ANALYSIS AND SIMULATION TOOLS FOR SOLAR ARRAY POWER SYSTEMS

by

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ABSTRACT

This dissertation presents simulation tools developed specifically for the design of solar array power systems. Contributions are made in several aspects of the system design phases, including solar source modeling, system simulation, and controller verification.

A tool to automate the study of solar array configurations using general purpose circuit simulators has been developed based on the modeling of individual solar cells. Hierarchical structure of solar cell elements, including semiconductor properties, allows simulation of electrical properties as well as the evaluation of the impact of environmental conditions.

A second developed tool provides a co-simulation platform with the capability to verify the performance of an actual digital controller implemented in programmable hardware such as a DSP processor, while the entire solar array including the DC-DC power converter is modeled in software algorithms running on a computer. This “virtual plant” allows developing and debugging code for the digital controller, and also to improve the control algorithm.

One important task in solar arrays is to track the maximum power point on the array in order to maximize the power that can be delivered. Digital controllers implemented with programmable processors are particularly attractive for this task because sophisticated tracking algorithms can be implemented and revised when needed

to optimize their performance. The proposed co-simulation tools are thus very valuable in developing and optimizing the control algorithm, before the system is built. Examples that demonstrate the effectiveness of the proposed methodologies are presented.

The proposed simulation tools are also valuable in the design of multi-channel arrays. In the specific system that we have designed and tested, the control algorithm is implemented on a single digital signal processor. In each of the channels the maximum power point is tracked individually. In the prototype we built, off-the-shelf commercial DC-DC converters were utilized. At the end, the overall performance of the entire system was evaluated using solar array simulators capable of simulating various I-V characteristics, and also by using an electronic load. Experimental results are presented.

To my parents

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I would like to thank my advisor Dr. Takis Kasparis for his guidance and encouragement throughout my study. I am grateful of his digital signal processing, electronics, and operational amplifier courses.

It would like to thank several individual who contribute to my research work. Dr. Issa Batarseh introduced me to power electronics and provided opportunities to gain various technical and non-technical experiences through various projects and discussion. Dr.Wenkai Wu developed the power stage used in this research and phase I of the Air Force project. Dr. Kasemsan Siri provided fruitful discussions on the subject of solar power system level and the simulation. I would like to extend my appreciation to my committee members for their help.

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LIST OF ABBREVIATIONS

A/D	Analog-to-digital
ADC	Analog-to-digital converter
BOL	Begin-of-life
CMC	Current-mode control
COTS	Commercial-off-the-shelf
D/A	Digital-to-analog
DAC	Digital-to-analog converter
DSP	Digital signal processing/processor
EOC	End of conversion
EOL	End-of-life
EVM	Evaluation module
GPIB	General Purpose Interface Bus
I-V	Current vs. voltage
IncCond	Incremental conductance
MPPT	Maximum power point tracking
OVR	Output voltage regulation
P&O	Purturb-and-observe
P-V	Power vs. voltage

PP	Parallel pin
PV	Photovoltaic
S/H	Sample-and-hold
SAS	Solar array simulator
SB	Shared-bus
SNR	Signal-to-noise ratio
SOC	Start-of-conversion
SPICE	Simulation program with integrated circuit emphasis

CHAPTER 1: INTRODUCTION

In recent years, the problem of energy crunch has become more and more aggravating, resulting in increased exploitation and research for new power energy resources around the world. In particular, the use of natural energy, especially the solar energy is increasingly emphasized and regarded as an important resource of power energy in the future.

As the power supplied by solar arrays depends upon the insolation, temperature and array voltage, it is necessary to implement a so-called maximum power point tracking (MPPT) technique to track the changes and extract the maximum power from the solar array. A MPPT for solar application is a control algorithm to force the impedance at the terminals of PV array to the value that produces maximum power out of the array. Some papers had proposed different maximum power point tracking control techniques in the past. The popularity of MPPT system was tempered to a large extent by operational problems, added complexity and unfavorable incremental costs.

1.1 Digital Control

The primary advantages of traditional analog controllers are high bandwidth, high resolution, are easy to understand and use, and they are relatively low in cost. Analog

controllers have some drawbacks such as component drift, they are hardwired and as a result they are not flexible. Large part count is also common for complex analog systems. Components age and change values over temperature and various environmental conditions. As far as predictability, one cannot obtain two components that are exactly alike. They have to be tweaked and trimmed. To modify a system one has to replace components. Board layouts become a consideration that we must take into account, and it is difficult, sometimes impossible, to implement some functions.

The innovation of DSP control into power electronic designs is an excellent example of the advantages provided by major technological advances. By replacing analog control with DSP control, the primary advantages are achieved by replacing hardware with flexible software.

A digital signal processing (DSP) controller is the combination of a high-speed mathematical core, memory, and a set of peripheral devices. With an appropriate set of peripherals for the application, it is possible to reach a single chip solution with minimum or even no external interface components. Today's DSP controllers created for complex motor speed and servo control are also ideally suited for renewable energy applications. The newly introduced low-cost, high performance DSPs, with features such as single-cycle multiplication and accumulation with on-chip pulse-width modulation (PWM) mechanism and analog to digital converters (ADCs), provide the Central Processing Unit (CPU) bandwidth and peripheral mix needed to implement sophisticated control techniques required for interfacing with various renewable energy sources.

There are many advantages to digital control. For example, digital controllers are less sensitive to the environment, they are highly reliable, and they are software programmable, which translates to greater flexibility. Digital controllers are precise, and offer more predictable behavior. Advanced control is also possible – enabling non-linear and multi-variable control. Designers can also perform multiple loops, and other unique functions.

A digital controller has many advantages over its analog counterpart. There are no hardware adjustments, fewer components, less aging effects, and smaller temperature drifts. With a digital controller, adjustment of control parameters for adapting to different electrical environments is easy and flexible. DSP provides other advantages such as full digital control, fewer components, high noise/EMI immunity, high reliability, reduced heating of power switches, lower harmonics, less filtering, faster fault response, no dc components, and higher efficiency. Additionally, it is easy to include other system level functions such as battery charging, power factor correction, reactive power compensation, fuzzy logic control, parallel operation, and on-the-fly frequency change to adapt to different environments and applications. Secure remote communication, data acquisition and display, device overload protection, maximum power tracking, and state control can all easily be implemented.

With the improvement in math-intensive functions and high execution speed, faster control response and correction to achieve desired parameters yields a better performing system. The DSP software allows for automation of the testing process, thus reducing the labor content of the technical staff. The software within the DSP can be

easily modified to optimize the application and provide diagnostic once in use in the field or if the application changes once the unit is installed. The application that the equipment addresses can be easily modified via software changes as opposed to hardware design changes. This also increases in-house design flexibility. Development time is reduced, since software is easier to revise than manufactured hardware. The same controller board can be used for different applications; thus economics are achieved by reducing the number of components in inventory across numerous product lines as well as the overhead associated with specifying and purchasing components.

With advanced DSP control, low frequency passive filter and high frequency filter damping circuits are not required. This results in a simple system configuration, high reliability, low cost, smaller footprint, and lighter weight. For example, the RFI (radio frequency interference) filter can be smaller and less costly. The controller will reduce the material cost of the customer's equipment, labor content, and overhead related to both materials and labor (purchasing transactions cost, accounting transactions costs, factory overhead). Technological advancements allow equipment to become smaller and lighter which translates into cost reduction, labor, transportation, and materials.

Digital controllers have drawbacks, however. Those include bandwidth limitations, numerical problems like quantization errors, data converter limitations, CPU performance limitations, and system cost concerns. More recently, many of the "traditional" negatives associated with digital controllers are disappearing. DSP controller technology is rapidly improving while prices are reaching levels where even cost-sensitive equipments benefit.

1.2 Scalable Power System

As the need for flexible, scalable space-based power requirements increases, and in an effort to avoid redesign of spacecraft and electric propulsion power systems, a number of concepts have emerged to provide expandable, parallel-connected power converters employing techniques such as maximum peak power tracking. Such approaches then allow a variety of options with the rest of the power system such as employing standard, modular, power converters that can be connected in parallel. The goal of such structures is to provide a single power system design that can meet a range of power requirements for spacecraft and/or electric propulsion power systems. For such a flexible and scalable power system, a need exists for control of such functionality. Depending on the concept, risks of power system failures exist due to a variety of circumstances. Under any circumstance that causes the output voltage of the power system to lose regulation, MPPT techniques ensure that the power delivered to the load is at the maximum available from the solar arrays. Hence, the control prevents the complete drop out of the system output voltage. Under normal sun insolation and healthy array source conditions, the control will not interfere with the regulation of the system output voltage because the load demand is below the maximum available power of the array source. The expansion capability of the system with such a control provides long-term cost/schedule benefits to the electric propulsion and spacecraft power systems of the next generations. In many cases, Commercial Off-the-Shelf (COTS) power converters can be employed with such control circuitry to meet space needs.

1.3 Outline

In this dissertation we present simulation tools and experimental work for solar power system. Chapter 2 gives a review of the modeling of solar cell sources and analysis of simple interconnection. An automated simulation tool is developed to ease the complexity of the analysis of solar cells characteristics. Simulation examples are presented. Chapter 3 describes methodologies for extracting maximum power from solar cell sources, and outlines existing techniques. A focus on dynamic tracking of maximum power point based on dither signal injection is discussed. Chapter 4 presents a flexible and scalable power system configuration under consideration. Details of the underlying components and their operation are explained for a single channel, and then for multi-channel arrangement. Chapter 5 describes a proposed co-simulation tool for system simulation. The tool is used to verify the digital-controlled implementation of the maximum power point tracking system, where a host computer simulates a modeled power stage and digital signal processor runs actual algorithms on-board. The communication and synchronization issues are discussed. Chapter 6 details the hardware and software implementation of the multi-channel power system. Various aspects of the embedded system implementation, such as timing and peripherals setup, are described. Descriptions of the power stage prototype and experimental results are shown. Chapter 7 provides conclusion and direction for future works.

CHAPTER 2: PHOTOVOLTAIC SOURCE MODEL

The understanding of solar cell source behavior is necessary to specify the size of solar array system or to study the stability of regulators. Placing the solar panels in an optimal way is an effective measure to take to maximize the energy yield from a photovoltaic-installation. Shading can rarely be completely avoided, certainly not in urban or suburban environments. At higher latitudes the sun is often close to the horizon, which makes the shading problem more severe than at low latitudes. Therefore, especially for high-latitude locations and urban/suburban sites, a shading-tolerant system should be chosen. Furthermore, the direction south/north (azimuth) and elevation angle should also be considered. Any shading of the solar panels will lead to considerable reduction in energy yield, even if just a small fraction of the panels is shaded. Consequently, the case in which the solar cells in the generation system do not operate under uniform generation conditions should be examined.

The connection of photovoltaic modules with different operating currents and/or voltages characteristic may result in the performance of the array being less than the sum of the potential performances of individual modules. When connected in series, the current flowing through the lowest productive cell limits the entire array output. The problem arises when modules have different sizes, which may be a result of individual modules not exposed to the same lighting conditions, such as is the case with differently

oriented modules or irregular shading of the array. Mismatch is more likely in large systems than in independent arrays, because individual modules may be oriented differently or they may be subject to varying degrees of shading and heating.

Taking into account that real operating conditions of a solar array are difficult to reproduce during tests, simulations to determine electrical characteristics will allow the researcher to gain more insight for better understanding and design. Performance gain is beneficial and can find applications in numerous areas such as the one described in reference [1]. As the fine modeling of a cell's behavior is the basis for any solar generator, the solar cell model needs to be properly determined. Methods for simulation of general solar array configuration have been proposed; however, these implementations are associated with special-purpose simulation tools, and detailed modeling has not been performed [2], [3], [4]. Utilizing a circuit-simulator such as Simulation Program with Integrated Circuit Emphasis (SPICE), one can run many component models.

2.1 Solar Cell Modeling

Solar cells are essentially a very large area p-n junction diode, where such a diode is created by forming a junction between the n-type and p-type regions. As sunlight strikes a solar cell, the incident energy is converted directly into electrical energy. Transmitted light is absorbed within the semiconductor by using the energy to excite free electrons from a low energy status to an unoccupied higher energy level. When a solar

cell is illuminated, excess electron-hold pairs are generated by light throughout the material; hence the p-n junction is electrically shorted and current will flow.

The equivalent circuit of a solar cell is represented by four components: a light-induced current source, a diode parallel to the source, a series resistor and a shunt resistor. The light-induced current is due to the separation and drift of the photon-generated electron–hole pairs under the influence of the built-in field.

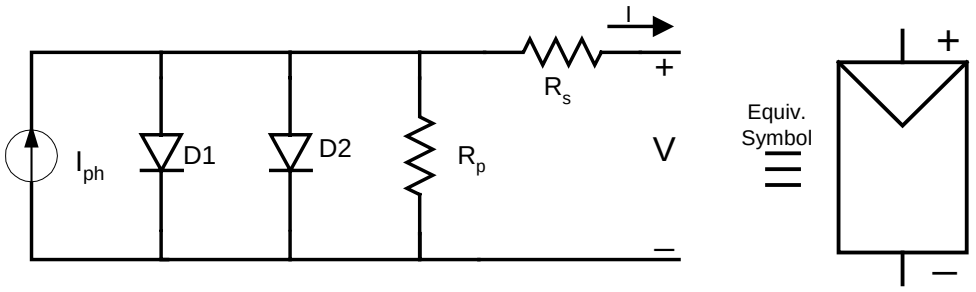


Figure 2.1: Two-diode solar cell model

The two-diode model of solar cell is shown in Figure 2.1. The corresponding current vs. voltage curves (I-V) equation is:

$$I = I_{ph} - I_{s_1}\left[e^{\frac{q(V+IR_s)}{n_1 kT}} - 1\right] - I_{s_2}\left[e^{\frac{q(V+IR_s)}{n_2 kT}} - 1\right] - \frac{V + IR_s}{R_p} \qquad (2.1)$$

where, I and V are the solar cell output current and voltage, I_{ph} is the generated photo-current, and I_{s1}, I_{s2} are the reverse saturation currents of each diode. The parameters n_1, n_2 are diode ideality factors, T is the absolute temperature in Kelvin, k is the Boltzmann's constant (1.380 x 10^{-23} J/K) and q is the elementary charge (1.602 x 10^{-19} C).

The two-diode model is derived from the physics of the p-n junction, especially those of poly crystalline silicon [5]. For amorphous silicon the single-diode model is more appropriate ($I_{s2} = 0$). The first saturation current, I_{s1}, is due to diffusion mechanism of the minority carriers into depletion layer, and the second, I_{s2}, is due to recombination in space-charge layer. Series resistance R_s is the effect of the path that photo-generated electrons have to traverse a surface semiconductor region to reach the nearest finger electrode. The value of R_s can also further increase for a thin finger electrode. A small fraction of the photo-generated carrier can also flow through the crystal surfaces or through grain boundaries in polycrystalline devices instead of flowing though the external load. This leakage can be represented by an effective internal parallel resistance R_p [6].

Consider a fixed environmental condition, a typical I-V characteristic of a solar cell is shown in Figure 2.2. The operating point on power vs. voltage curve (P-V curve) will depend on the solar array characteristic and the load. Assuming that initially there is no load, the operating point will be at the far right at the open-circuit voltage, Voc, of the solar array with zero current (V = Voc, I = 0). As the load increase, the operating point will move up and to the left, i.e. voltage at the solar array terminal decreased, while the power increases. As the load increases further, it will reach the maximum power point (MPP), where the power drawn from the solar cell is maximized. The voltage at this point is denoted by the maximum-power voltage (Vmp), and the current by maximum-power current (Imp). If the load increases beyond this point, the voltage decreases and

power drawn from the solar array decreases. Eventually, the operating point will reach the far left at the short-circuit current, Isc, with zero voltage output (V = 0, I = Isc).

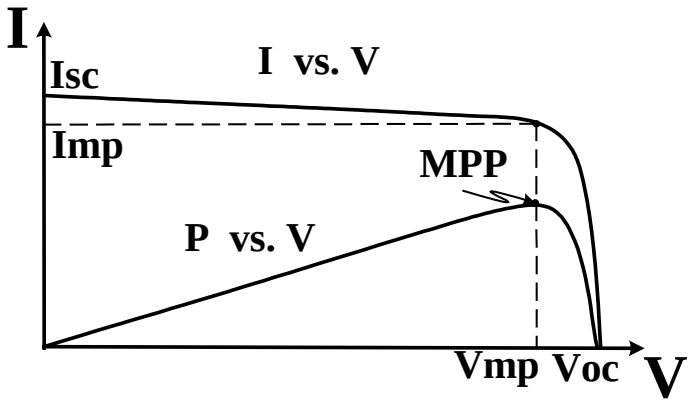


Figure 2.2: Typical I-V and P-V characteristics of a solar cell

Solar cell model parameters vary with environmental conditions, the two most important effects being temperature and irradiance. Solar cell open-circuit voltage decreases with increasing temperature, and the short circuit current is proportional to the amount of irradiance. The current vs. voltage curves (I-V curves) for various irradiance and temperature are shown in Figure 2.3 and Figure 2.4, respectively.

The equations showing modeling effects of irradiance and temperature on model parameters [5] are:

$$I_{ph} = I_{ph}\big|_{Tref} \left[1+K_0\left(T - T_{ref}\right)\right] \tag{2.2}$$

$$I_s = I_s\big|_{Tref} \left(\frac{T}{T_{ref}}\right)^3 \exp\left\{\frac{-qE_g}{nk}\left(\frac{1}{T_{ref}} - \frac{1}{T}\right)\right\} \tag{2.3}$$

$$R_s = R_s\big|_{Tref} \left[1 - K_3\left(T - T_{ref}\right)\right] \tag{2.4}$$

$$R_p = R_p\big|_{Tref} \exp\{-K_4 T\} \tag{2.5}$$

where T_{ref} is the cell reference temperature. E_g is the band gap energy of the semiconductor. K_0 is the short-circuit temperature coefficient, and K_3, K_4 are the resistance temperature coefficients. Each parameter value is varied relative to the value at the cell reference temperature.

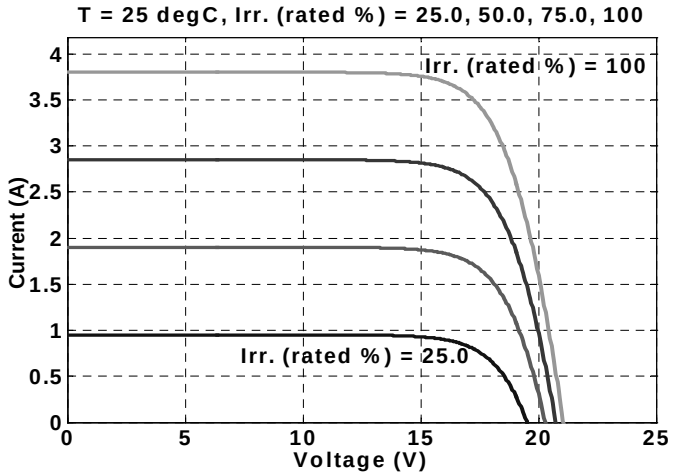


Figure 2.3: I-V curves for various irradiance

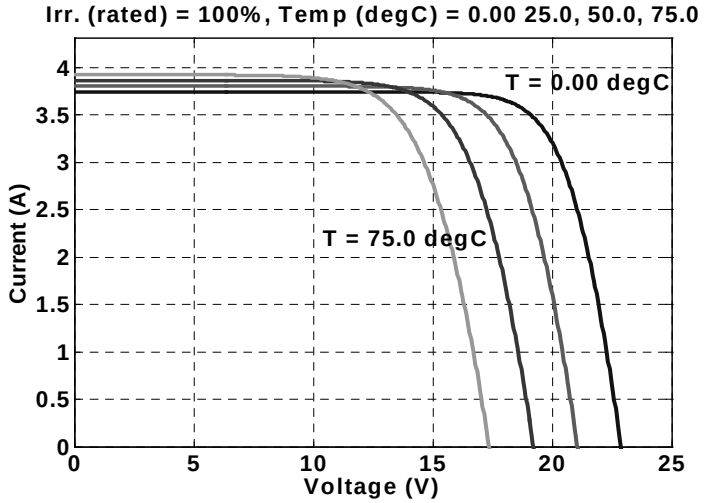


Figure 2.4: I-V curves for various temperature

2.2 Solar Array Structure

When solar cells are connected in parallel, the voltage is the uniform for each solar cell, and the current generated from each cell flows without restriction. In other words, the output voltage of the system becomes the voltage of a single cell, and the output current becomes the sum of the currents in each cell. In contrast, when solar cells are connected in series, the same current flows through each cell and the output voltage is the sum of the voltages across each of the cells. The voltage of each cell is determined according to the generation current, which depends on the generation conditions. Therefore, the optimal generation voltages are not always obtained for each cell. These behaviors can be generalized to the parallel/series connection of photovoltaic modules, provided the environmental condition is uniform on every cell in the modules.

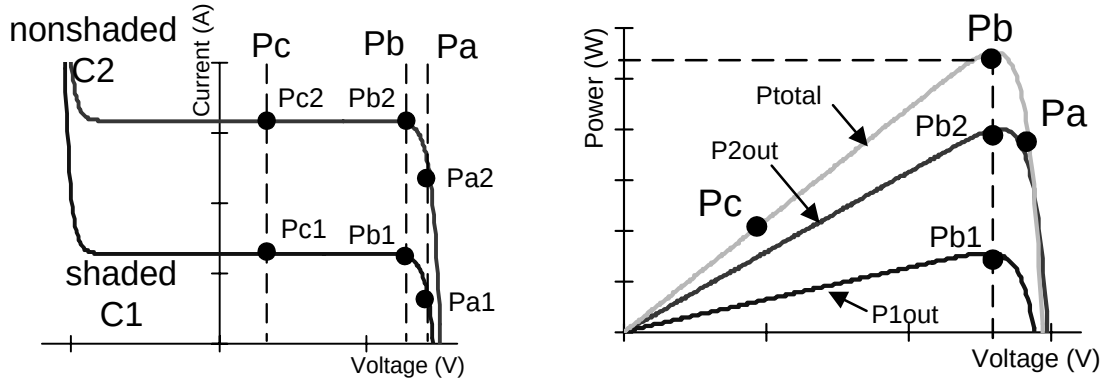


Figure 2.5: Generation characteristics for two parallel-connected cells.
(a) I–V characteristics. (b) P–V characteristics.

Figure 2.5(a) shows the typical generation characteristics and I-V curve for two parallel-connected cells that have different generation conditions, mainly in the amount

of irradiance. In this figure, C1 and C2 represent of a shaded and a nonshaded cell, respectively. In parallel connection, the operating point of each cell is given by the point of intersection of the vertical operating lines, $P_{a\text{-}c}$, i.e. uniform cells' voltage, and the I-V curve of each cell. As the output current of the system increases from zero to the maximum current, the operation point of each cell moves as indicated in Figure 2.5(b), $p_{a1} \rightarrow p_{b1} \rightarrow p_{c1}$ for C1 and $p_{a2} \rightarrow p_{b2} \rightarrow p_{c2}$ for C2. This operation characteristic reveals that both the nonshaded cells and the shaded ones can operate in the area where each cell can generate power. Hence, the total output P-V characteristics of these cells are obtained as shown in Figure 2.5(b). Then, the total output power, P_{total}, is given by Equation (2.6), where, the generation power on C1 is P_{1out}, and the generation power on C2 is P_{2out}.

$$P_{total} = P_{1out} + P_{2out} \tag{2.6}$$

In series connection, the operating point of each cell is given by the point of intersection of the horizontal operation line, i.e. uniform cells' current, and the I-V curve of each cell. As the output current of the system increases from zero to the maximum current, the operation point of each cell moves as indicated in Figure 2.6(a), $s_{a1} \rightarrow s_{b1} \rightarrow s_{c1}$ for C1 and $s_{a2} \rightarrow s_{b2} \rightarrow s_{c2}$ for C2. On operation line S_b, the shaded cell, C1, generates its maximum power, but the nonshaded cell, C2, does not generate its maximum power yet. When the operation line moves to Sc, the operation points of each cell C1 and C2 move to s_{c1} and s_{c2}, respectively, and the generation power on C2 increases. The unshaded cell, C2, will force the shaded cell, C1, to pass more current than its new short

circuit current. The shaded cell operates in reverse-bias region and causes a net voltage loss to the system. This is a point of breakthrough in the pn-junction when the externally applied electric field will overcome the intrinsic electric field, known as the avalanche effect. The product of the current and the negative voltage (avalanche voltage) gives the power dissipated by the shaded cell. In other words, the shaded cell will dissipate power as heat and cause "hot spots" [9]. Here the nonshaded cell, C2, generates power, P_{2out}, but the shaded cell, C1, causes a power loss, P_{1loss}. Hence, the output power, P_{out}, on this system is decreased to the following equation:

$$P_{total} = P_{2out} - P_{1loss} \tag{2.7}$$

The total output power characteristic of this system, the P-V curve, is obtained in the same manner and is shown in Figure 2.6(b). Two peaks in power exist, but the output powers at these peak points are much smaller than that of the parallel-connected condition shown in Figure 2.5(b). Although only a two-cell connection is described here, the mechanism by which power reduction occurs for multiple cells that are connected in series is similar to that for two-cell connection.

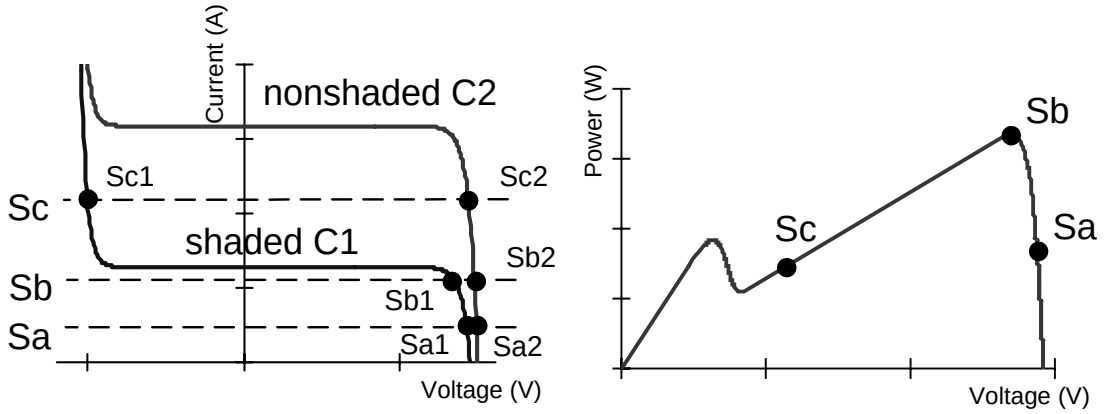


Figure 2.6: Generation characteristics for two series-connected cells.
(a) I–V characteristics. (b) P–V characteristics.

Solar cells are often connected together to form strings that produce a desirable voltage. In the string connection, the voltage is the sum of the device voltages and the string current is limited to the current of the least productive device in the string. Multiple strings are connected in parallel to form a panel. In practice, additional diodes are included for protection. Bypass diodes are depicted with black-filling, while gray-filled diode symbols represent blocking diodes. Diodes connected in series with cells perform a blocking function, preventing backflow of current back into the module string. When diodes are installed in parallel with cells/modules, they perform a bypass function allowing current to pass around a shaded area of a module. The configuration, including physical layout, will have impact on the system performance [7][8]. Figure 2.7 shows various solar cell interconnections. Figure 2.7(a) and (b) have blocking diode on every string before the positive array terminal. Bypass diode is connected across every cell in Figure 2.7(a), while across every 18 cells in Figure 2.7(b). Figure 2.7(c) has the same electrical configuration as in Figure 2.7(b), but each string is arranged as 2 columns with 9 cells per column.

To minimize the power loss and to prevent destruction of series-connected solar cells due to shading effect, we use bypass diodes over a group of cells. Bypass diodes allow current to pass around shaded cells and thereby reduce the voltage losses through the module. When a module becomes shaded its bypass diode becomes “forward biased” and begins to conduct current through itself. All the currents greater than the shaded cell’s new short circuit current are “bypassed” through the diode, thus reducing drastically the amount of local heating at the shaded area. The energy from the by-passed

substring is still lost, however. Bypass diodes should be connected across fewer solar cells to improve module's shade-tolerant.

Diodes placed in series with cells or modules can perform the function of blocking currents from flowing back to the modules; thus, preventing the modules from becoming loads. In battery charging systems, the module potential drops to zero at night, and the battery could discharge backwards through the module. Diodes placed in the circuit between the module and the battery can block any discharge flow. In the case that one string becomes severely shaded, or if there is a short circuit in one of the modules, the blocking diode prevents the other strings from loosing current backwards down the shaded or damaged string.

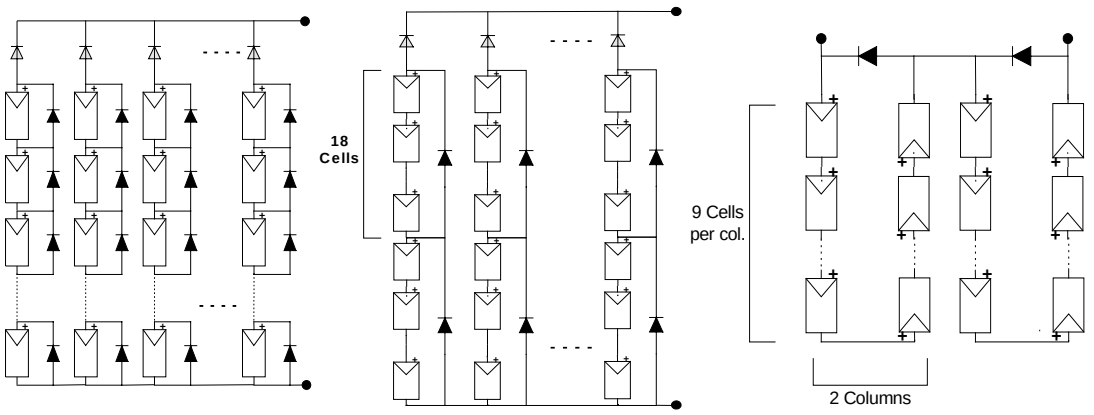


Figure 2.7: Various solar cells interconnection.
(a) Bypass diode across every cell, (b) Bypass diode across a group of cells, (c) Same as (b) with different physical layout

2.3 Implementation

Expression to describe solar cell characteristic is extremely nonlinear. The equation to describe their interconnection behavior is even more complex. Numerical techniques to solve for I-V curve have been proposed. To be able to obtain data for generalized solar cell structures under varying weather conditions, it is essential to have both programmability and circuit simulation capability. While circuit-oriented simulator, such as SPICE, is an excellent tool for solving circuit networks, existing schematic tools are not suitable for simulating photovoltaic system and data analysis functions for evaluating photovoltaic parameters are cumbersome. To this end, software with flexible coding feature will be utilized in addition to circuit simulator.

The implementation of the proposed tool is broadly consisted of four components. The first is an electrical configuration representing the interconnection of the elementary solar cells and protective diodes. Various models of photovoltaic devices and that of diodes can be applied to accommodate different types of solar cells. The second component is the environmental condition that account for climatic variation. These environmental conditions, such as short circuit current and temperature, can be incorporated into netlist as passing parameters to the solar cell elements via subcircuit parameterization. Circuit simulator solves the array circuit network, then a script file finally extracts data. A pictorial representation of the automated process is shown in Figure 2.8.

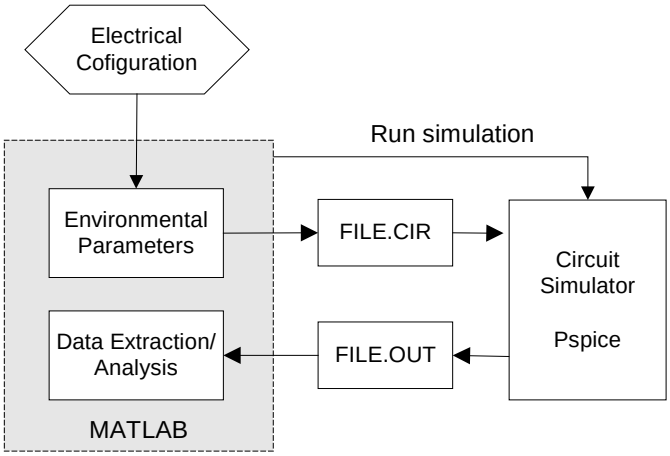
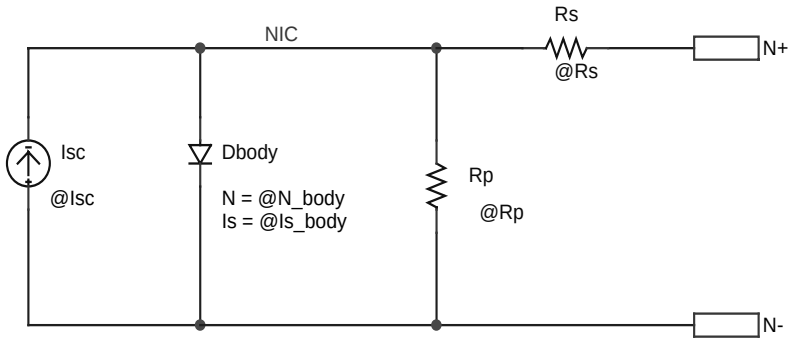


Figure 2.8: Implementation flow chart

PSPICE's sub-circuit [10] is used to model the individual cell and allow variable input parameters to fine-tune the model. With the sub-circuit of a single-diode model solar cell shown in Figure 2.9, short circuit current, saturation current and ideality factor of the body diode, and equivalent series and parallel resistances are variables. A call to the sub-circuit is also shown.

The proposed method has been implemented using two general-purpose software: a simulator to obtain electrical measurements given varying environmental condition and/or electrical structure, and a scriptor to update the netlist file **`FILE.CIR`**, start the simulator, read simulation results from the output file **`FILE.OUT`**, and perform data analysis. MATLAB script file is developed to create PSPICE netlist of a selected electrical configuration composing of solar cell PSPICE's sub-circuit. Node name is automatically updated to represent the electrical connections between solar cells for such structure. One of the advantage for this implementation is the ability to create batches of simulations, so for example, the performance of the solar array can be simulated with

varying illumination as it varies throughout a day. An important aspect of this batch mode is that the resulting I-V curves are automatically collected and analyzed, allowing large quantities of data to be handled with ease.

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************* Single diode solar cell model *************
*
.SUBCKT  CELL1D  N+  N-  PARAMS:
+ Isc=4  Is_Dbody1=1e-14  N_Dbody1=1  Rs=1u  Rp=1G

Isc     N-   NIC  DC    {Isc}
Dbody1  NIC  N-   _Dbody1
.MODEL      _Dbody1     D     Is={Is_Dbody1}    N={N_Dbody1}
Rs      NIC  N+   {Rs}
Rp      N-   NIC  {Rp}
.ENDS       CELL1D
*
******************
*
* Example of call to subcircuit
X_s01_c01     N_s01_c00_01  N_s01_c01_02  CELL1D
+  PARAMS: Isc=7.059E-001  Is_Dbody1=1.000E-010
+  N_Dbody1=1.000E+000  Rs=1.000E-003  Rp=5.000E+003
*******************************************************
```

Figure 2.9: PSPICE subcircuit model and schematic equivalent

2.4 Application Examples

To demonstrate the proposed method, some applications examples are presented. Comparison of shading effect on different panel configurations are considered, namely 1) panel with bypass diode across every solar cells, and 2) with bypass diode across every Nb cells with the same physical layout. The physical layout considered is strings of vertically-aligned solar cells with blocking diode at the output terminal of the panel and top most cells as shown in Figure 2.7(a) and b with 54 rows by 72 columns dimension. Variation of various parameters can be represented by two-dimensional matrix, such as an image file. The dimension of the image N rows x M columns corresponds to the physical layout of a solar panel with NxM solar cells. Illumination of each image pixel provides a mapping to the amount of short circuit current, i.e. white area corresponds to full short circuit current, while darker area has less. For an 8-bit grayscale image, a pixel value of 255 can corresponds to irradiance that produces the full short circuit current. By analogy, mapping of solar cells' temperature by a two-dimension image is also possible. For example, a high pixel value can correspond to high temperature. For a partially shaded cell, the parameter value is assumed constant and is equal to the corresponding averaged value [12]. For instance, cell illumination is set to the average solar irradiance over the entire cell.

In Figure 2.10(a) and (b), a gradual shadow is casted across the diagonal and along the vertical of the panel as represented with intensity levels shown. For simplicity, other parameters are kept constant in this case. A variable load across each solar array

configuration obtains I-V characteristic, and P-V is calculated and displayed. As it can be noticed, certain shading patterns produce local maxima in the power curve, and the proposed method provides a tool to study the severity of such shading effects.

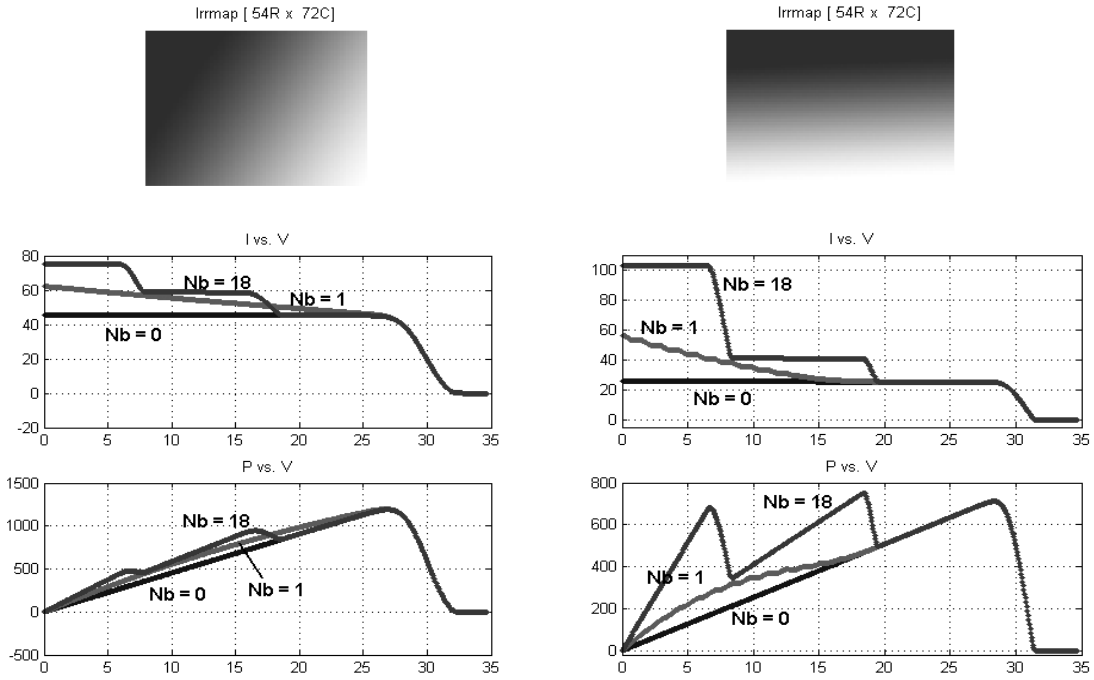


Figure 2.10: I-V and P-V curve of partially shaded panel
(a) Diagonal shade (b) Vertical shade

Even though, it is possible to assume that each cell in a module has the same semiconductor characteristic, another potential feature of the proposed method is that it allows distribution of the parameters statistically to account for manufacturing tolerances. As a result, all solar cells can be simulated together as a module, allowing the effects of cell mismatching to be evaluated. Example showing effects of resistances variation is shown in Figure 2.11.

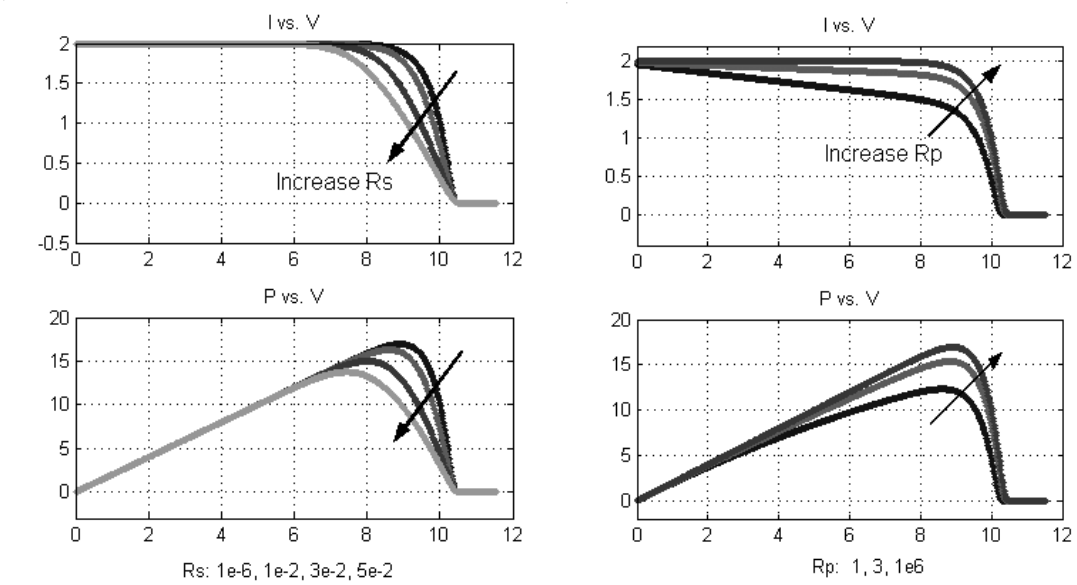


Figure 2.11: Parameter variation (a) Rs (b) Rp

2.5 System Consideration

Unlike ideal voltage or current sources, solar arrays produce a limited electrical energy which related to the amount of sunlight they receive. As describe earlier, other environmental, such as temperature, also affects the solar array's electrical characteristics. For stand-alone application, it is necessary to incorporate backup battery to provide extra energy when load-demand energy exceeds that provided by the solar array sources, and both battery and arrays must be properly sized. Since the arrays also requires a large area for installation, then for optimal cost benefit it is desirable to extract the maximum power available from solar array sources, with minimum number of arrays installed.

CHAPTER 3: MPPT ALGORITHMS

The environmental condition under which a solar power system operates can be wide, as shown in I-V curves in Figure 3.1. The current-voltage relation of a solar array is variable throughout the day, as it varies with environmental conditions such as irradiance and temperature. In terrestrial applications, Low Irradiance, Low Temperature (LILT) condition reflects morning condition where the sun just rises. A High Irradiance, High Temperature (HIHT) condition might represent a condition near high noon in a humid area. High Irradiance, Low Temperature (HILT) condition can represent a condition with healthy sunlight in the winter. Finally, condition near sunset can be described by Low Irradiance, High Temperature (LIHT) condition. For space application, LILT characterizes a deep space mission or aphelion period, while HIHT condition is when satellite orbits near the sun (perihelion).

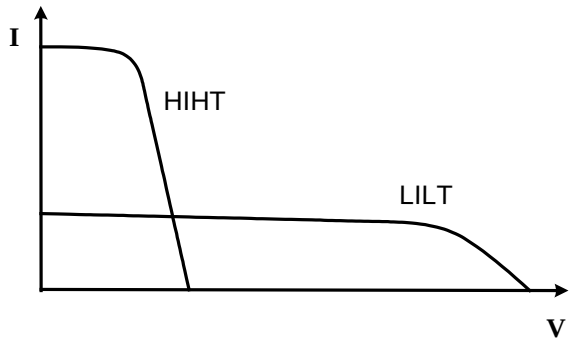


Figure 3.1: I-V characteristics under wide operating conditions

For a uniformly illuminated array, there is only one single point of operation that will extract maximum power from the array. In a battery charging system where the load seen by the solar modules is a battery connected directly across the solar array terminals, the operating point is determined by the battery's potential. This operating point is typically not the ideal operating voltage at which the modules are able to produce their maximum available power.

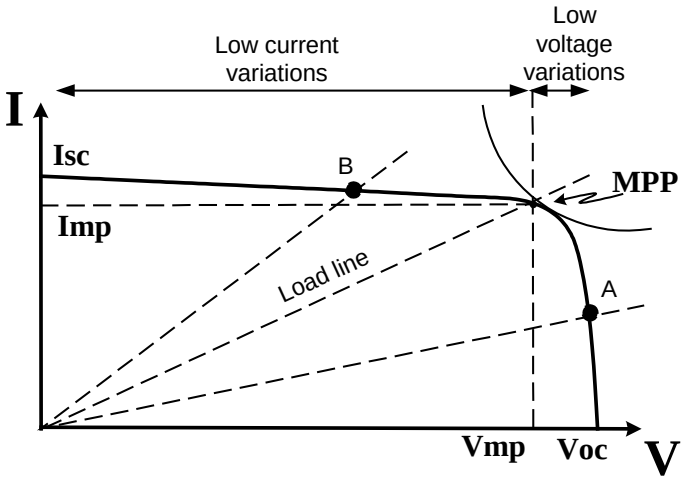


Figure 3.2: Direct coupled method

In the direct coupled method [13], in which the solar array output power is delivered directly to the loads, as shown in Figure 3.2. To match the MPPs of the solar array as closely as possible, it is important to choose the solar array I-V characteristic according to the I-V characteristics of the load. A general approach for the power feedback control is to measure and maximize the power at the load terminal, and it assumes that the solar array maximum power is equal to the maximum load power. However, this maximizes the power to the load not the power from the solar array. The direct-coupled method cannot automatically track the MPPs of the solar array when the

insolation or temperature changes. The load parameters or solar array parameters must be carefully selected for the direct coupled method

To be able to extract the maximum power from the solar array and to track the changes due to environment, therefore, a maximum power point tracking should be implemented. Devices that perform the desired function are known as Maximum Power Point Trackers, also called MPPTs or trackers. A tracker consists of two basic components, as shown in Figure 3.3: a switch-mode converter and a control with tracking capability. The switch-mode converter is the core of the entire supply. The converter allows energy at one potential to be drawn, stores as magnetic energy in an inductor, and then releases at a different potential. By setting up the switch-mode section in various topologies, either high-to-low (buck converter) or low-to-high (boost) voltage converters can be constructed. The goal of a switch-mode power supply is to provide a constant output voltage or current. In power trackers, the goal is to provide a fixed input voltage and/or current, such that the array is held at the maximum power point, while allowing the output to match the load voltage.

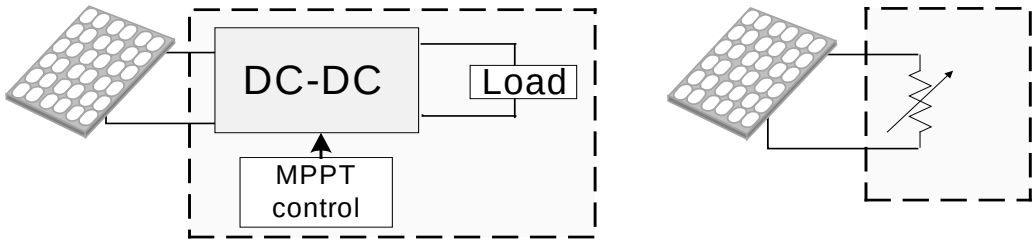


Figure 3.3: Basic components of a maximum power pointer tracker

When properly applied, a maximum power point tracking control can prevent the collapse of the array voltage under excessive load demand, particularly when supplying a

constant-power type of load. One of the proper approaches is to operate the system in a solar array voltage regulation mode where the array voltage is clamped to a commanding set point, Vmp, which is dynamically updated by the MPPT control circuit. The control processes feedback signals, such as the array current and voltage, to determine a proper direction to move the operating point. Eventually, this continuously updated set point will fluctuate around the voltage corresponding to the array peak power point. By adjusting the operating point of the array to the point Vmp, power output of the array is maximized, and the most efficient use of the solar array may be realized.

For a system without MPPT, the voltage will quickly collapse to zero. This phenomenon can be understood from the I-V characteristic of a solar array. The flatness of the I-V curve on the left of the MPP implies that a small incremental increase in current demand leads to large voltage change. A system with MPPT avoids the voltage collapse by keeping the operating point near the MPP. On the I-V curve, the operating point corresponding to the maximum-power point is around the "knee" region. Therefore, unlike other power systems with stiff voltage sources, power conversion from solar array sources with MPPT requires more robust design due to risks of an array voltage collapse under peak load demand or severe changes in the array characteristics.

The location of the MPP of an I-V characteristic is not known a priori, and must be located. A number of MPPT control algorithms / methods have been proposed. In the subsequent sections, the algorithms will be reviewed. The MPPT method based on dither signal injection will be emphasized, and later applied in this dissertation.

3.1 Constant Voltage and Current

The constant voltage algorithm is based on the observation from I–V curves that the ratio of the array's maximum power voltage, Vmp, to its open-circuit voltage, Voc, is approximately constant:

$$Vmp / Voc = K \quad < 1 \tag{3.1}$$

The constant voltage algorithm can be implemented using the flowchart shown in Figure 3.4. The solar array is temporarily isolated from the MPPT, and a Voc measurement is taken. Next, the MPPT calculates the correct operating point using Equation (3.1) and the preset value of K, and adjusts the array's voltage until the calculated Vmp is reached. This operation is repeated periodically to track the position of the MPP. Although this method is extremely simple, it is difficult to choose the optimal value of the constant K. The literature reports success with K values ranging from 73 to 80%.[14]. Constant voltage control can be easily implemented with analog hardware. However, its MPPT tracking efficiency is low relative to those of other algorithms. Reasons for this include the aforementioned error in the value of K, and the fact that measuring the open-circuit voltage requires a momentary interruption of PV power.

It is also possible to use a constant current MPPT algorithm that approximates the MPP current as a constant percentage of the short-circuit current [15]. To implement this algorithm, a switch is placed across the input terminals of the converter and switched on momentarily. The short-circuit current is measured and the MPP current is calculated, and the PV array output current is then adjusted by the MPPT until the calculated MPP

current is reached. This operation is repeated periodically. However, constant voltage control is normally favored because of the relative ease of measuring voltages, and because open-circuiting the array is simple to accomplish, but it is not practically possible to short-circuit the array (i.e., to establish zero resistance across the array terminals) and still make a current measurement.

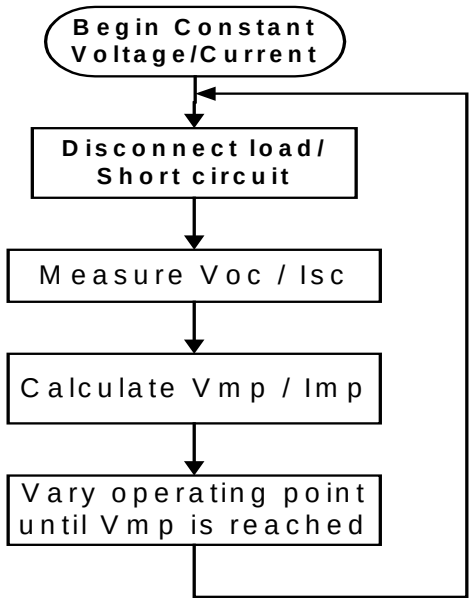


Figure 3.4: Constant voltage/current algorithm flowchart

3.2 Pilot Cell/Reference Array Measurement Approach

In the pilot cell MPPT algorithm, the constant voltage or current method is used, but the open-circuit voltage or short-circuit current measurements are made on a small solar cell, called a pilot cell, that has the same characteristics as the cells in the larger

solar array. Alternative improvement can be achieved with I-V characteristics curve measurement by scanning reference solar cells located at strategic points on the array, but do not constitute a part of the array itself. The pilot cell measurements can be used by the MPPT to operate the main solar array at its MPP, eliminating the loss of PV power during the Voc or Isc measurement. However, the problem of a lack of a constant K value is still present. Also, this method has a logistical drawback in that the solar cell parameters of the pilot cell must be carefully matched to those of the PV array it represents. Thus, each pilot cell/solar array pair must be calibrated, increasing the cost of the system.

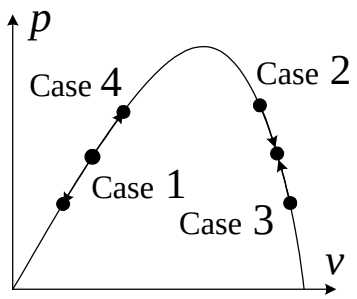
3.3 Model-Based MPPT Algorithms

If the values of the parameters in the solar array I-V equation are known for a given solar cell, the solar cell current and voltage could be calculated from measurements of the light incident on and temperature of the solar cell. The maximum power voltage could then be calculated directly, and the PV array operating voltage could be simply set equal to Vmp. Such an algorithm is commonly called a model-based MPPT algorithm. Although appealing, model based MPPT is usually not practical because the values of the cell parameters are not known with certainty, and in fact can vary significantly between cells from the same production run. In addition, the cost of an accurate light sensor (pyranometer) can by itself make this MPPT scheme unfeasible.

3.4 Perturb-and-Observe

As the name of the perturb-and-observe (P&O) states, this process works by perturbing the system by increasing or decreasing the array operating voltage and observing its impact on the array output power. The operating voltage is perturbed with every MPPT cycle. As soon as the MPP is reached, V will oscillate around the ideal operating voltage Vmp. Figure 3.5 summarized the control action of the P&O method. The value of the reference voltage, Vref, will be changed according to the current operating point. For example, for when the controller senses that the power from solar array increases ($dP > 0$) and voltage decreases ($dV < 0$), it will decrease (-) Vref by a step size C1, so Vref is closer to the MPP. The MPP represents the point where Vref and scaled down Vsa become equal.

The oscillation around a maximum power point causes a power loss that depends on the step width of a single perturbation. The value for the ideal step width is system dependent and needs to be determined experimentally to pursue the tradeoff of increased losses under stable or slowly changing conditions. In fact, since the AC component of the output power signal is much smaller than the DC component and will contain a high noise level due to the switching DC-DC converter, an increase in the amplitude of the modulating signal had to be implemented to improve the signal to noise ratio (SNR), however, this will lead to higher oscillations at the MPP and therefore increase power losses even under stable environmental conditions.



Case	dP	dV	Action
1	< 0	< 0	+
2	< 0	> 0	-
3	> 0	< 0	-
4	> 0	> 0	+

Figure 3.5: Perturb & Observe (P&O) control action

Several improvements of the P&O algorithm have been proposed. One of the simplest entails the addition of a 'waiting' function that causes a momentary cessation of perturbations if the algebraic sign of the perturbation is reversed several times in a row, indicating that the MPP has been reached. This reduces the oscillation about the MPP in the steady state and improves the algorithm's efficiency under constant irradiance conditions. However, it also makes the MPPT slower to respond to changing atmospheric conditions, worsening the erratic behavior on partly cloudy days. Another modification involves measuring the array's power P1 at array voltage V1, perturbing the voltage and again measuring the array's power, P2, at the new array voltage V2, and then changing the voltage back to its previous value and remeasuring the array's power, P1, at V1. From the two measurements at V1, the algorithm can determine whether the irradiance is changing. Again, as with the previous modifications, increasing the number of samples of the array's power slows the algorithm down. Also, it is possible to use the two measurements at V1 to make an estimate of how much the irradiance has changed between sampling periods, and to use this estimate in deciding how to perturb the

operating point. This, however, increases the complexity of the algorithm, and also slows the operation of the MPPT.

3.5 Incremental Conductance

The incremental conductance (IncCond) method [16] is based on comparing the instantaneous panel conductance with the incremental panel conductance. The input impedance of the DC-DC converter is matched with optimum impedance of PV panel. As noted in literatures, this method has a good performance under rapidly changing conditions. The algorithm uses the fact that the derivative of the output power P with respect to the panel voltage V is equal to zero at the maximum power point:

$$\frac{dP}{dV} = I\frac{dV}{dV} + V\frac{dI}{dV} = I + V\frac{dI}{dV} = 0 \tag{3.2}$$

One of the advantages of the IncCond algorithm is that it does not oscillate around the MPP. The check of condition (1) and dI = 0 allows it to bypass the perturbation step and therefore maintain a constant operating voltage V once the MPP is found. Furthermore, conditions $\left|\frac{dI}{dV} + \frac{I}{V}\right| > 0$ and $dI > 0$ make it possible to determine the relative location of the MPP. This leads to the advantage that an initial adjustment in the wrong direction, as with the "trial and error" P&O method, does not occur. A fast and correct system response to changing operating conditions should be the result – yielding high system efficiency. A small marginal error could be added to the maximum power

condition (1) such that the MPP is assumed to be found if $\left|\frac{dI}{dV}+\frac{I}{V}\right|<\varepsilon_2$. The value of ε_2 was determined with consideration of the tradeoff between the problem of not operating exactly at the MPP and the possibility of oscillating around it. It will also depend on the chosen perturbation step size C1.

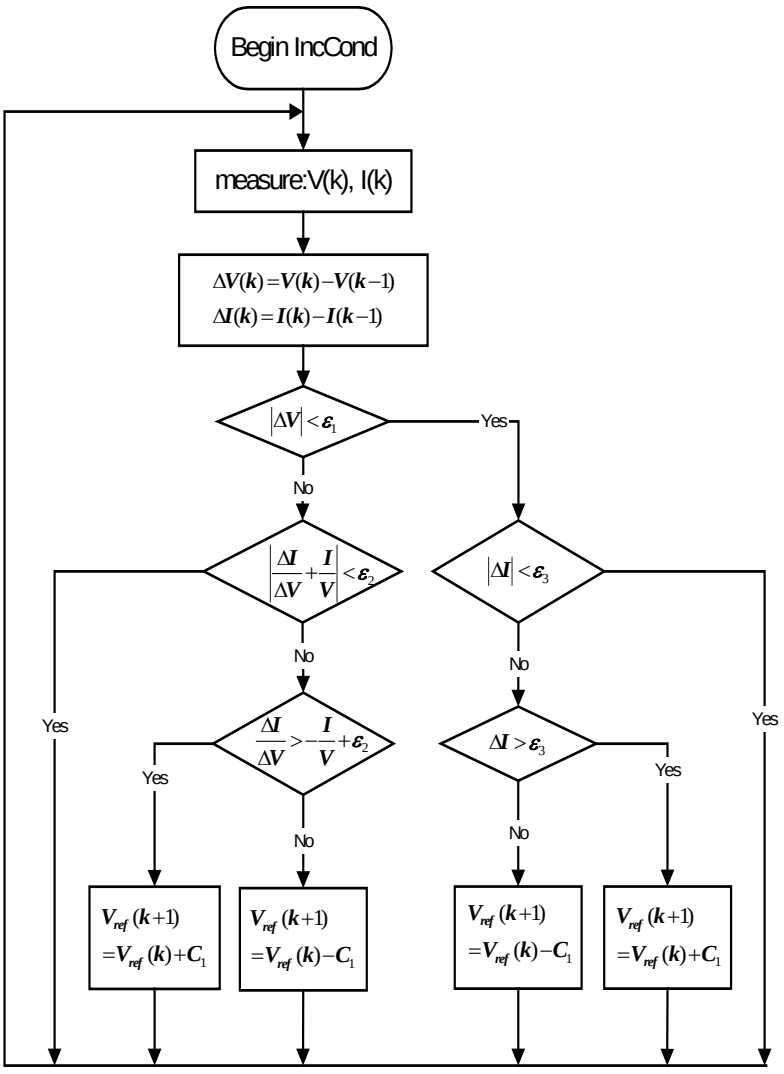


Figure 3.6: Incremental conductance algorithm flow chart

3.6 Parasitic Capacitance

The parasitic capacitance algorithm [17] is similar to incremental conductance, except that the effect of the solar cells' parasitic junction capacitance Cp, which models charge storage in the p–n junctions of the solar cells, is included. By adding this capacitance to the lighted diode equation, and representing the capacitance using i(t) =CdV/dt, Equation (3.3) is obtained.

$$I = I_{ph} - I_{s_1}\left[e^{\frac{q\left(V_p + IR_s\right)}{n_1 kT}} - 1 \right] + C_p \frac{dv_p}{dt} = F(v_p) + C_p \frac{dv_p}{dt} \tag{3.3}$$

On the far right of Equation (3.3), the equation is rewritten to show the two components of I, a function of voltage $F(v_p)$ and the current in the parasitic capacitance. Using this notation, the incremental conductance of the array g_p can be defined as $dF(v_p)/dv_p$ and the instantaneous conductance of the array, g_L can be defined as $-F(v_p)/v_p$. The MPP is located at the point where $dP / dv_p = 0$. Multiplying Equation (3.3) by the array voltage V_p to obtain array power and differentiating the result, the equation for the array power at the MPP is obtained:

$$\frac{dF(v_p)}{dt} + C_p\left(\frac{\dot{V}}{V} + \frac{\ddot{V}}{\dot{V}}\right) + \frac{F(v_p)}{v_p} = 0 \tag{3.4}$$

The three terms in Equation (3.4) represent the instantaneous conductance, the incremental conductance, and the induced ripple from the parasitic capacitance. The first and second derivatives of the array voltage take into account the AC ripple components generated by the converter. The reader will note that if C_P is equal to zero, this equation

simplifies to that used for the incremental conductance algorithm. Since the parasitic capacitance is modeled as a capacitor connected in parallel with the individual solar cells, connecting the cells in parallel will increase the effective capacitance seen by the MPPT. From this, the difference in MPPT efficiency between the parasitic capacitance and incremental conductance algorithms should be at a maximum in a high-power solar array with many parallel modules.

The array conductance is just the ratio of the instantaneous array current to the instantaneous array voltage. Obtaining the array differential conductance is more difficult, but it can be done using Equation (3.5):

$$g_P = \frac{P_{GP}}{V_0^2} = \frac{\frac{1}{2}\sum_{n=1}^{\infty}\left[a_n^i \cdot a_n^v + b_n^i \cdot b_n^v\right]}{\frac{1}{2}\sum_{n=1}^{\infty}\left[\left(a_n^v\right)^2 + \left(b_n^v\right)^2\right]} \tag{3.5}$$

where P_{GP} is the average ripple power, V_O is the magnitude of the voltage ripple, and a_n^i; a_n^v; b_n^i; b_n^v are the coefficients of the Fourier series of the PV array voltage and current ripples. The values of P_{GP} and V_O^2 may be obtained from a circuit configuration like that seen in Figure 3.7. The inputs to the circuit are the measured array current and voltage. The high-pass filters remove the DC component of V_{PV}. The two multipliers generate the AC V_O^2 and AC P_{gP}, which are then filtered by the low-pass filters, leaving behind the DC components of V_O^2 and P_{gP}. From Equation (3.5), the ratio of these two values is equal to the array conductance, which can then be used in conjunction with Equations (3.2) until the array differential conductance and the array conductance are equal.

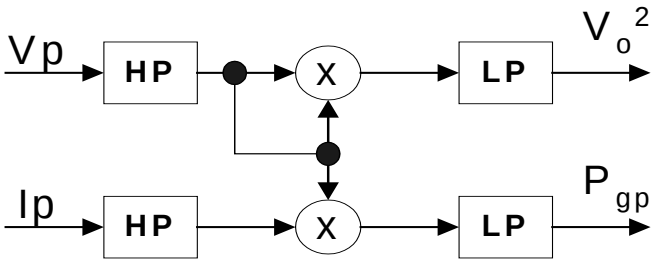


Figure 3.7: Circuitry used to implement the parasitic capacitance method

3.7 Dither Signal Injection

The MPPT control usually operates in a limiting cycle oscillation in which the array voltage contains an AC ripple component, while continually tracking the array peak power that varies with changes in environmental conditions. Several MPPT approaches rarely achieve stability in both amplitude and frequency of the oscillatory array voltage ripple. These MPPT controllers can lose their peak power tracking ability and lock up in a "trapped" state far from the array peak power point due to the insufficient strength of the feedback signal used for determining the proper control direction toward the maximum power point. Therefore, an improved MPPT control approach should take into account all the severe circumstances of solar source to achieve sufficient stability margin.

An MPPT approach employing a dither signal superimposed on the updated set point provides the controllability of the amplitude and frequency of the array voltage ripple with respect to the amplitude and frequency of the dither signal. Using the dither signal to properly perturb the MPPT control loop, the power system can operate without a

trapped state in which the array voltage is settled far above or below the peak power voltage. In contrast, several other MPPT approaches, without dither signal injection, experience two major difficulties: The first is a trapped state in which the array voltage is undesirably settled down (far from the peak power point condition), and the second is that the operating amplitude and frequency of the array voltage ripple around the peak power point are not fixed and difficult to analyze because of their load dependency. Consequently, the improved MPPT controllers (for different array sources not connected in parallel) can be set to operate synchronously by sharing the same dither signal for which the frequency of the ac voltage ripple in steady-state is the same for all the DC-DC converters being controlled in tandem.

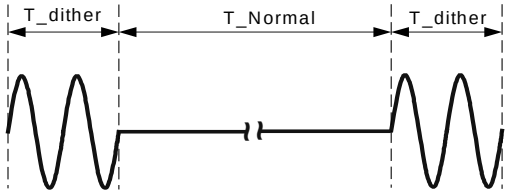


Figure 3.8: Modified dither-based MPPT scheme

Another approach is to vary the amplitude of the dither signal over time, as shown in Figure 3.8. In such an arrangement, a higher efficiency could be expected since the solar arrays primarily operate in near peak power point. Such operation could adopt larger modulation amplitude to increase the SNR and system dynamic performance. Furthermore, multiple local maxima problems could be overcome by finding the global maximum through scanning a wide control range MPPT operation. Since the percentage of large ripple is much smaller, the overall system efficiency will be improved.

Dither signal in MPPT method and proposed hybrid MPPT method helps to increase the system stability; however, it also by-produces one drawback namely the output ripple. For multiple channel solar array power system, this issue could be mitigated by inversing the dither signal for the complimentary solar array source.

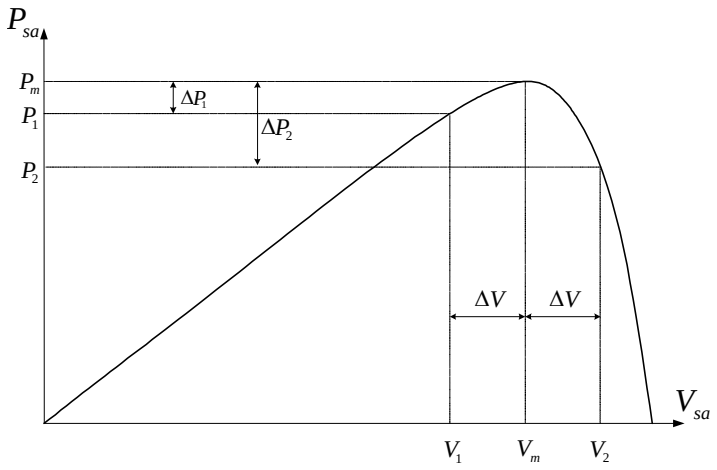


Figure 3.9: Solar array power change vs. voltage change

For a system with dither signal added to the setting voltage to generate the reference signal for solar array voltage compensator, the setting voltage is change slowly to keep the system stable. So the reference signal will include the dither signal. Since the solar array voltage will follow the reference signal, the solar array voltage will follow the dither signal changing. Here sinusoidal signal is chosen as dither signal. Figure 3.9 shows the power change according to the voltage change. We can find the power change is not symmetric even if the voltage change is symmetric around the maximum power point. For example, solar array voltage changes from maximum power point V_m to V_1, the power change from P_m to P_1. The solar array output power will change from P_m to P_2,

if the changes from maximum power point V_m to V_2. Although V_m-V_1 is equal to V_2-V_m (=ΔV), the power change is not the same, i.e. ΔP_1 is not equal to ΔP_2. The simulation results of system with dither signal are shown in Figure 3.10.

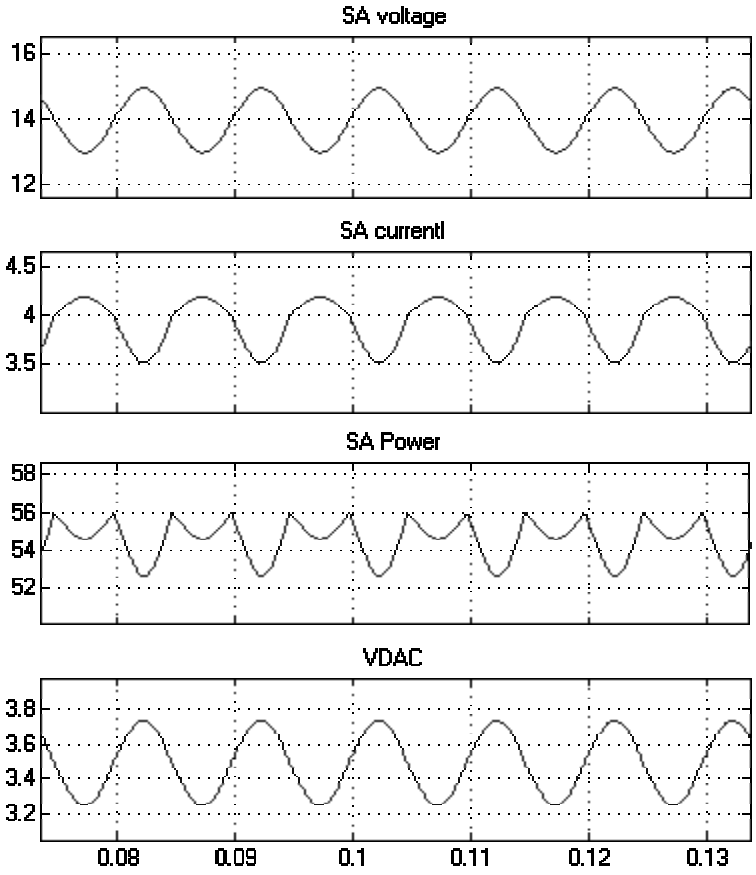


Figure 3.10: Simulation results with dither signal added

3.8 Analog Implementation

Figure 3.11 shows the detailed block diagram for the maximum power tracking system using discrete components. The description of how the maximum power tracking system automatically adjusts operation conditions of the converter to maximum power

point of the solar array is as follows. The maximum power point tracker receives i_{in}, V_{in} sense signals, and the dither signal to calculate the control signal. The array voltage passes through a low pass filter (LPF) and scalar to provide appropriate signals to the two samples and hold (S/H) circuits. At the output of the sample and hold circuits the present state voltage signal V(n) and the previous state V(n-1) will be generated by sampling V_{in} at two adjacent sampling times with one sampling period apart. Likewise, the product of i_{in} and V_{in} will be processed to provide P(n) and P(n-1) since scaling the current will be correlated with the average output power change and consequently with the average change in the solar array power due to the slow varying output voltage. The sampling intervals are controlled by a sampling signal. The four signals V(n), V(n-1), P(n), and P(n-1) will provide the MPPT control algorithm with enough indications on the direction of voltage and power movements. At the output of the MPPT control circuit the increment INCR and decrement DECR signals will define two operation states; an increment and decrement in the array voltage, respectively.

In Figure 3.12 we can notice that during maximum power point tracking process the operation point on the P-V curve can fall in two distinct regions. In region I the operation point will be to the left of the maximum power point and the voltage of the solar array should be increased to move this point up towards MPP. On the other hand when the operation point is to the right of the MPP the solar array voltage should be decreased.

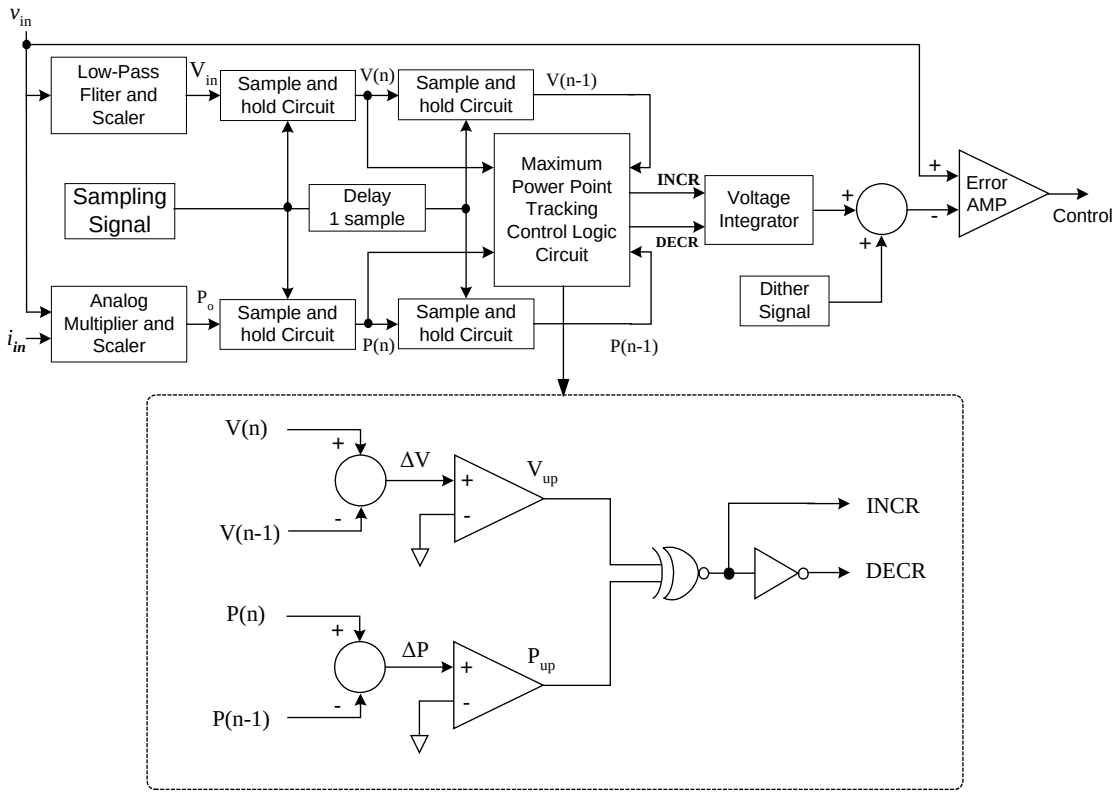


Figure 3.11: Control mechanism of MPPT

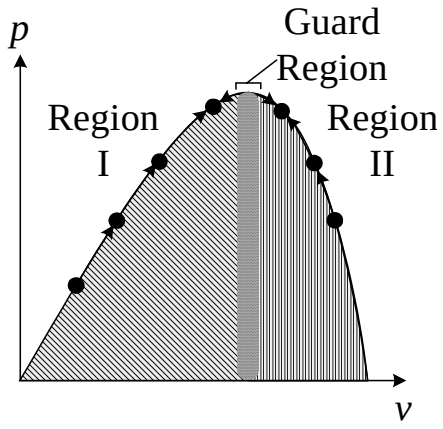


Figure 3.12: Regions of MPPT

In order to trace the operation point to its related region, the algebraic difference between V(n) and V(n-1) is generated to produce true logic V_{up} when the input voltage is

increasing and false V_{up} other wise. The same process will be applied to P(n) and P(n-1) to produce the logic P_{up}. Figure 3.13 shows all the logic combinations that may occur and the associated movement of the operation point. When V_{up} and P_{up} are either high or low the action should be increasing the array voltage to move the point to a higher position on the curve other. When V_{up} and P_{up} have different logic the array voltage should be decreased. Connecting V_{up} and Pup to an exclusive NOR gate with the direct output to INCR and inverted output to DECR with provide the described functionality.

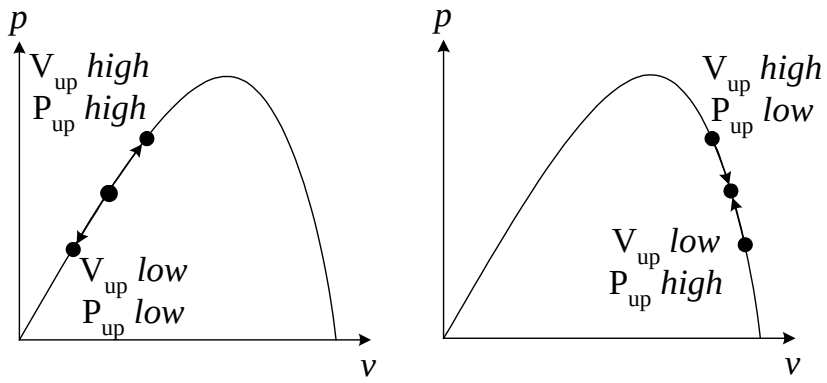


Figure 3.13: Logic combinations that may occur and its associated movement

The voltage integrator at the output of this logic circuit will provide a linearly changing tracking signal that is clamped between minimum and maximum levels to a summer. This signal will be linearly increasing if only INCR is high and linearly decreasing if only DECR is high. The summer will sum up the tracking signal with the dither signal and provide a set point signal that is AC dithered above the DC level of the tracking signal and feed it to an error amplifier as shown in Figure 3.11. The difference between the summer signal and the input voltage will be amplified through the error amplifier to generate the output control signal that provides the negative feedback closed loop operation and controls the solar array voltage and power.

3.9 Applications

The MPPT techniques have much wider application than just photovoltaic alone, since similar functionality of power output versus loading can be seen in the I-V curves of other sustainable energy sources. Such sources are small water turbines and wind-power turbines; however, the actual physics behind the I-V curves for the various sources are different. The voltage, current, and power produced by such sources is variable in response to environmental conditions (insolation, pressure, or wind speed) and dependent on the electrical impedance of the load. Under any combination of environmental conditions, each of these sources is characterized by exactly one ideal load impedance, which will result in operation at V_{MPPT} and maximum power transfer.

CHAPTER 4: SYSTEM CONFIGURATION

Unlike other power systems with stiff voltage sources, power conversion from solar array sources with MPPT requires more robust design due to risks of an array voltage collapse under peak load demand or severe changes in the array characteristics. One of the two control approaches may be used for preventing the total collapse of array voltage: array current regulation or array voltage regulation. Array current regulation is a means of controlling the array current so that it does not exceed a pre-determined set point when load demand is heavy. However, under conditions where the array characteristics change significantly such that the array short-circuit current is close to or below the set point, the array voltage can still collapse. Array voltage regulation is a more robust method of preventing the voltage collapse since it regulates the array voltage to the voltage set point when the load demand exceeds the array peak power. Normally, to achieve near optimum End of Life (EOL) performance, the array voltage set point remains fixed near or at the array voltage corresponding to the array peak power at EOL. During periods of low sun intensity or severe degradation of the array characteristics, the clamped array voltage enables reliable power transfer to the load without requiring unnecessary power drain from standby batteries to fulfill the load demand. In this case, it is best to apply an MPPT approach to continuously clamp the array voltage at the array peak power.

For a solar array source power system, DC-DC converters operate in output voltage regulation mode when system-load demand is less than array peak power. In this case the operating point on the I-V array characteristic curve is on the right side of the array peak power point where the array source behaves similar to a voltage source of low internal impedance. As the load increases, the solar array operating point moves up to the left along the array I-V characteristics until it reaches the maximum power point while the system output voltage remains regulated. Without MPPT control, when the load current is above the level corresponding to the array maximum power, the array I-V operating point will move to the left of the maximum power point, causing the system output voltage to lose regulation. Without a proper controller design, the array voltage can collapse toward zero when load demand is above the maximum power of the array, particularly when supplying a constant-power type of load.

4.1 System Architecture Under Consideration

The overall system architecture [19] under consideration can be decomposed into 4 parts as shown in Figure 4.1: solar array, power module, maximum power point tracking (MPPT) controller, and load. The solar array acts as the source of energy, and the load dissipates energy. The characteristic of the solar array varies depending on environmental factors, while the load can be changing. The power module contains parallel-connected DC-DC converters with outer loop voltage-mode regulation and inner loop current-mode control (CMC) that regulate energy from solar array into a constant

voltage output. The input and output terminals of the DC-DCs are tied together. Parallel pin (PP) is used to achieve current sharing between converters and control of current-mode loop. The MPPT controller senses the voltage and current from the solar array, determine proper action, and change reference voltage, Vref, for the power module to maximize the energy drawn from solar array under a given condition.

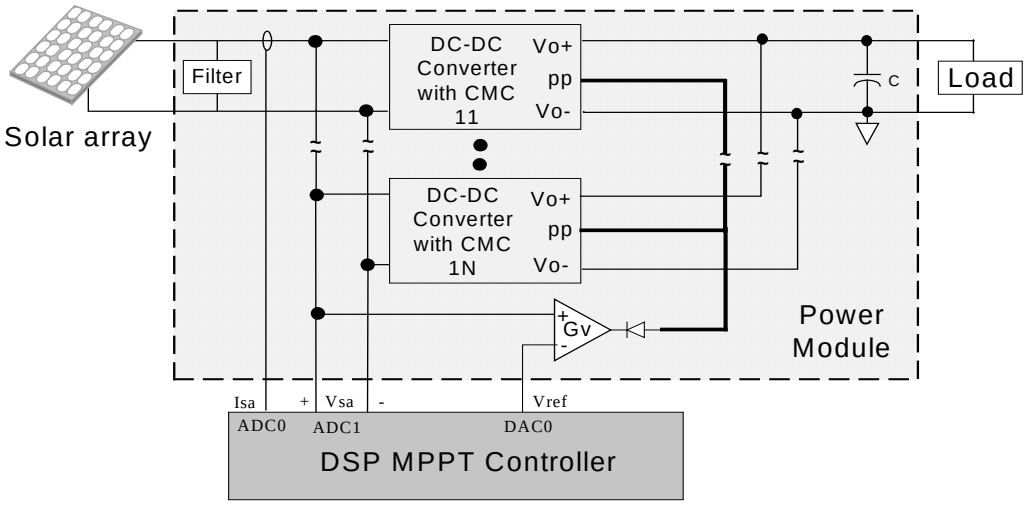


Figure 4.1: Configuration of paralleled converters with MPPT control for a single solar channel

4.2 Parallel Current-mode-controlled DC-DC with Current Sharing

Current-mode control [18] is a two-loop control strategy for switching regulators that is used to enhance the stability of the voltage output of the switching regulator. An inner high speed current loop provides control of the inductor current, while a slower outer loop regulates the output voltage by providing an error signal input to the inner

current loop. This error signal is related to the difference between the actual output voltage and the desired output voltage. The error signal from the error amplifier in the slower outer loop is the current command signal for the high-speed inner loop. This increases the bandwidth of the inductor current so that the voltage regulation loop is essentially changed into a controlled current source for frequencies well below the switching frequency of the switching element.

Connecting converters in parallel also presents several new challenges. The main issue for the parallel-connected converters is how to distribute the current uniformly among the converters. Currently, most of the approaches were mainly intended for uses in large classes of power converters that usually do not exploit current mode control as the innermost basic control loops. When considering a much simpler current sharing control approach, current mode controlled converters become very attractive. Although some approaches adopted current mode control as the innermost control loop, the added complexity makes it unsuitable for expandable power system applications.

Current mode converters connected in parallel with automatic-master current sharing bus are shown in Figure 4.2. The controlling voltage to all current-mode power stages is created by tying together all the outputs of the converter voltage error amplifiers, Hv's, via additional diodes connected to the error amplifier output. It can be found after current sharing bus is inserted inside the voltage regulation loop that it becomes the inner loop regulation structure for current sharing. The benefit is that the current sharing loop and current feedback loop can be combined together as one current loop, and the total control structure becomes simple. Also the current sharing response

can be much faster because now the current sharing loop is inside and its bandwidth will not be limited by the outside voltage loop. In addition, the automatic master current sharing method for inner loop regulation structure are based on each module's output of voltage compensator rather than the shared current, so there will be no "chattering" or fault tolerance issue as demonstrated in the other structures with current sharing bus being outside of the voltage regulation loop. The current sharing bus actually carries a common reference for the current loops in all modules based on the current reference each module provides through their voltage compensators. From the orientation of the diodes in Figure 4.2, the common reference voltage on the shared bus is the minimum command voltage from the module's voltage compensators. This common reference voltage will be given by the compensator of the DC-DC module with the lowest internal output reference voltage $V_{ref[i]}$. The current sharing accuracy is then decided by the current control accuracy of each module. Shared bus with the fault tolerance makes the power system a real scalable system just through adding/removing the power modules and without conflict with the running modules. Such arrangement also has the benefit of eliminating the non-uniform output characteristics caused by different reference voltage among the converters. Besides, the shared bus can also be implemented to track the maximum power point, and thereafter to further simplify the system and make it possible to carry out MPPT control with the standalone Commercial Off the Shelf (COTS) power modules. Therefore, such a current sharing techniques is suitable for solar-based expandable parallel-connected power system.

The application of paralleling modules actually brings benefits in the following aspects: 1) lowering the current stress on each single power semiconductor devices, therefore improves the thermal management and increase the current output capability, 2) achieving so-called N+1 redundant and greatly improves the reliability of the power supply; 3) providing more flexibility for customization, eases the maintenance and repair, and reduce the cycling time.

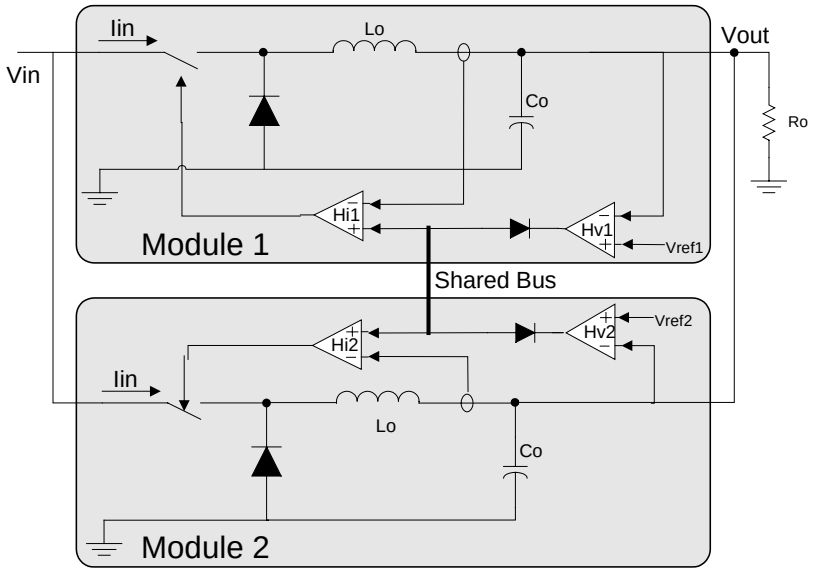


Figure 4.2: Paralleled converters with current sharing bus

4.3 Single-channel Configuration

The MPPT algorithm under consideration is the dither signal based algorithm, and care must be taken for system design. The frequency of the dither signal is selected to be significantly below the resonant frequency formed by the net capacitance across the solar

array(s) and the inductance(s) within the line-filter(s) of the DC-DC converter(s) [20]. The power input port of the paralleled dc-dc converter modules requires a bus stabilizer (BS) terminated across the solar array source but located as close to the system input as possible to damp out ac energy, thus ensuring system stability during maximum power tracking.

Figure 4.3 shows the internal configuration of current-mode DC-DC(s) with an additional solar array voltage compensator, Gv, for Maximum Power Point Tracking (MPPT) mode. The DC-DC(s) have to internal compensators: Hi is the inner current-loop compensator, and Hv is the output voltage compensator. Depending on the power demand of the load and the maximum available power from solar array, there are two operation modes in this system. When the power demanded by the load is less than the maximum available power of solar array, converters will operate under output voltage regulation (OVR) mode to keep output voltage constant, and MPPT controller will not take effect. Otherwise it operates under MPPT mode. Under MPPT mode, the MPPT controller will take over the control to let converters draw a current that will achieve maximum power from solar array.

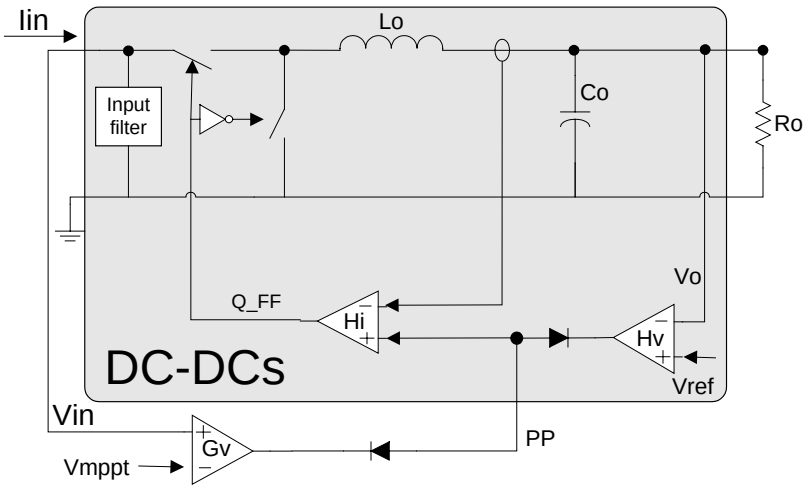


Figure 4.3: Two operating modes

Under light load condition, the voltage regulation takes effect, while the current regulation is activated when the operating point of the solar array is near the maximum power point. For light load, the voltage of the solar array is greater than the reference voltage. The output of the comparator is high; thus turning off the diode, and the parallel pins are unaffected. Near the MPP, the reference voltage is greater than solar array voltage. The parallel pins voltage will be pull down; thus limiting the current output from converters. System with backup batteries to provide the extra energy, the output voltage can be maintained, but without the batteries, the output voltage will drop. We can also say that operating point on the right side of the MPP corresponds to voltage-mode controlled, and current-mode controlled for the left side of the MPP.

Figure 4.4 to Figure 4.8 shows waveforms for the system operating under two modes. The load for the system is of resistive type undergoes a repetitive transient. From 0-6ms and 160-165ms, the load demand is less than that from the solar source (light load), and the system operates in OVR mode. From 6-160ms and 165-250ms, the

demand exceeds the maximum power available from solar array (heavy load), and the system operates in MPPT mode.

Figure 4.4 shows the resulting command to the inner current-loop compensator, Hi. The command is the lower quantity of 1) command from output voltage compensator, Hv (OVR command) and 2) command from solar array voltage compensator, Gv (MPPT command). The outputs of the compensators take turn moving toward a maximum saturation voltage when it does not affect the parallel pin. In other words, the output of Gv moves toward the maximum saturation in OVR mode, and the output of Hv in MPPT mode. The outputs that move toward saturation will have no influence over the operation of the current loop.

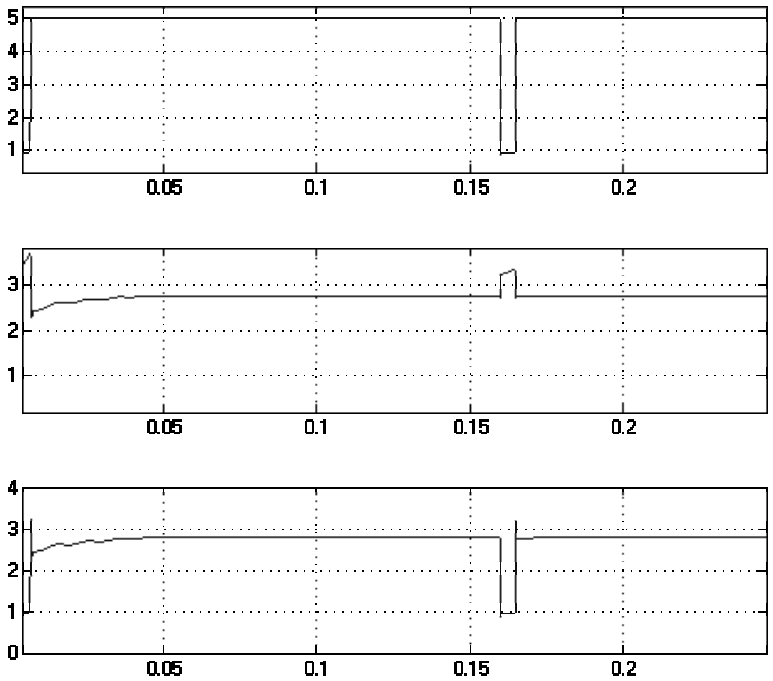


Figure 4.4: Command to the current-loop compensator
(a) OVR command, (b) MPPT command, (c) Resulting current-loop command - PP

Figure 4.5 presents the climbing and the steady state characteristics of the set point voltage, when the MPPT controller is seeking the maximum power point then oscillates around it, once it is reached. The reference voltage is the set point voltage with a 100Hz sinusoidal dither signal superimposed.

Figure 4.6 displays the voltage and current waveforms of the solar array. In OVR mode the waveforms are nearly constant reflecting a constant light load. In MPPT mode, the initial drop in solar array voltage represents the operating point set by the MPPT controller that is lower than the actual solar array MPP. After MPPT controller increases the reference voltage point and MPP is reached, the average solar array voltage then becomes constant. The ripple shown in the solar array voltage and current waveforms is due to the dither signal injection seen at the current command compensator.

Figure 4.7 shows the effect of the transient load on the system output voltage (without backup batteries). In OVR mode the output is maintained constant by the output voltage compensator. When the load demand power becomes greater than the maximum available from the source, the output voltage initially drops. This initial output voltage reduction is resulted from the initial decrease in the input power. The output voltage compensator over-demanded the input current, so the operating point moves quickly to the left of the maximum power. The MPPT controller takes control, but has not reached the MPP. As the MPPT controller seeks for the location of maximum power, the input power increases, and so do the output power and the output voltage. Once the operating point oscillates around the MPP, the average output voltage will be constant with inherent superimposed ripple caused by the dither signal. As the load demand switches to a

lighter one, the system changes from MPPT to OVR mode. The output voltage will increase briefly until the fast-action of the output voltage compensator regulates to the output reference voltage. Figure 4.8 shows the load transient effect on the output current: a different viewpoint of the same phenomenon. The output current is low when the system is in OVR mode, and is high in MPPT mode. The frequency current ripple is the same as that of the dither signal. For a system with backup batteries at the system output, a constant output voltage equal to the batteries' voltage will be maintained. However, the batteries will be required to provide the extra energy approximately equal to the difference between the load demand energy and the supplied energy from the solar sources.

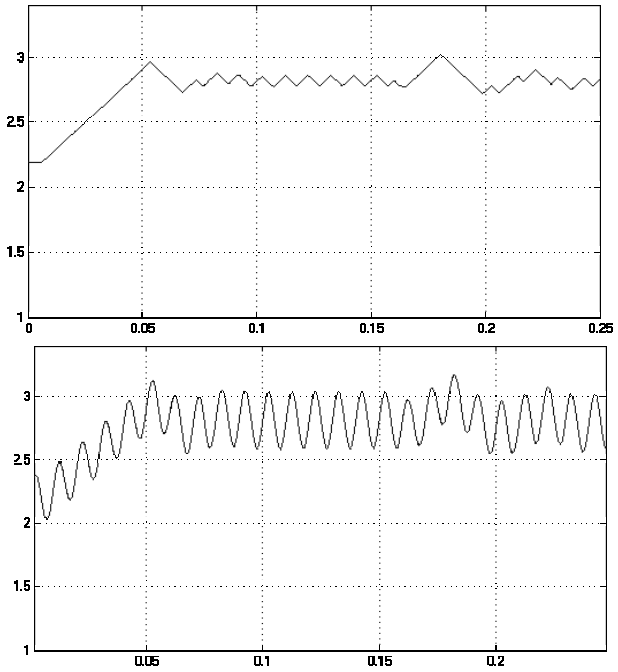


Figure 4.5: (a) Set point voltage and (b) Reference voltage from MPPT controller

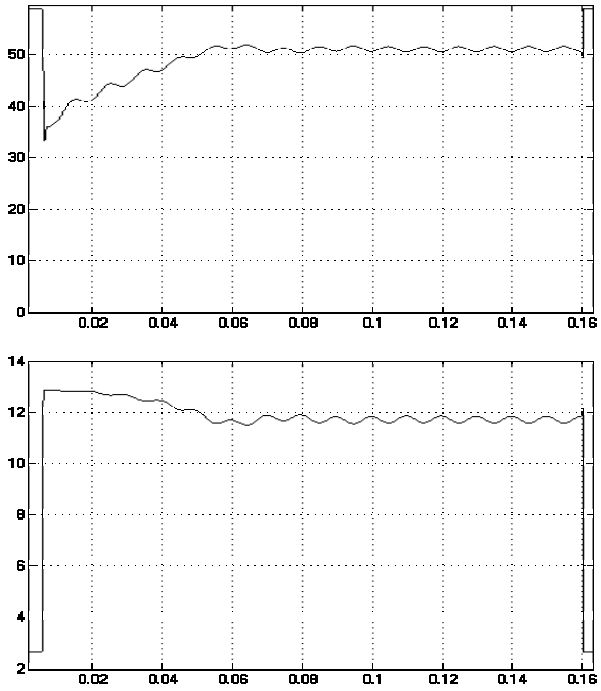
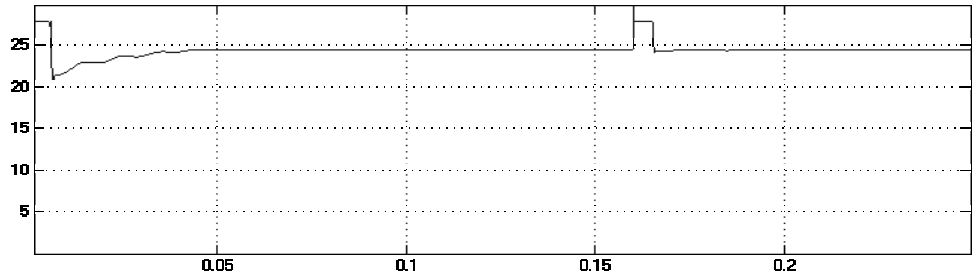
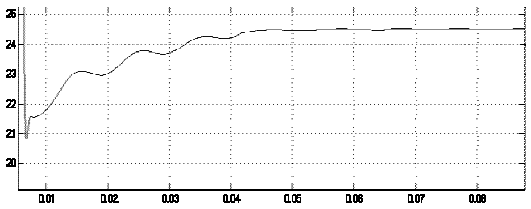


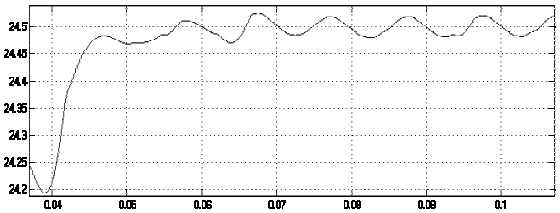
Figure 4.6: Solar array (a) voltage and (b) current under transient load



(a)



(b)



(c)

Figure 4.7: Output voltage under transient load
(a) overall waveform, (b) near the transient, (c) when MPP is reached

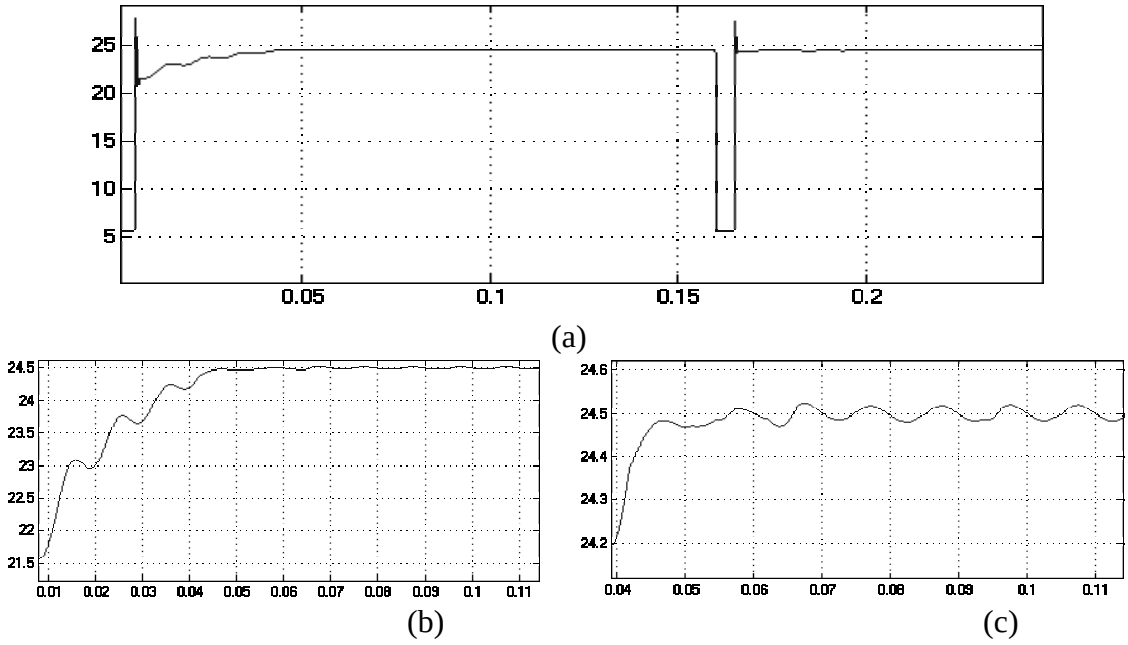


Figure 4.8: Transient load current
(a) overall waveform, (b) near the transient, (c) when MPP is reached

4.4 Multi-channel Configuration

The power system with the multiple solar array voltage regulation and MPPT control is shown in Figure 4.9, the configuration is output-paralleled DC-DC converters system with distributed solar sources, each of which is connected to the input of respective set of DC-DC converters. A simple DSP-based controller dedicated to all the solar array sources is implemented to control their respective set of DC-DC converters, therefore track the multiple peak power points of the distributed solar arrays. The MPPT controller processes the array output voltage Vin and current signals Iin, then deliver the proper reference signals to the solar array compensators. The compensators regulate one

or more converter modules through the Shared Bus (SB). Shared Bus and parallel pin (PP) pins are interfaced by PNP transistor(s) that provide a distributed current-sink to its respective voltage-error amplifier within each converter. When transistor(s) become active during the MPPT mode of operation, the driving impedance across the PP and return terminals is much lower as compared to that without the transistor, resulting more effective noise attenuation.

All the solar array output voltage and current are fed into the DSP controller for tracking their respective array peak power. Each channel either automatically adjusts its operating condition to be near or at the maximum power point of its solar array source(s) or regulates its system output voltage when the net load demand is below the peak power. At the same time, nearly uniform current sharing among DC-DC converter modules connected in parallel is also achieved by the concept of shared-buses. In this distributed MPPT approach, each current mode DC-DC converter module has an additional control port for the purpose of MPPT.

It is possible that while many converter modules are operating in their output voltage regulation mode, the remaining modules may operate in MPPT mode individually, depending on the characteristics of their respective solar array sources. Three modes of operation exist for the multi-channel system depending on the relative power between the solar channels available power and the load demand: 1) the load demand can be handled by a single channel, 2) the load demand is met with more than one channel, 3) the load demand power exceeds the total power available from all channels.

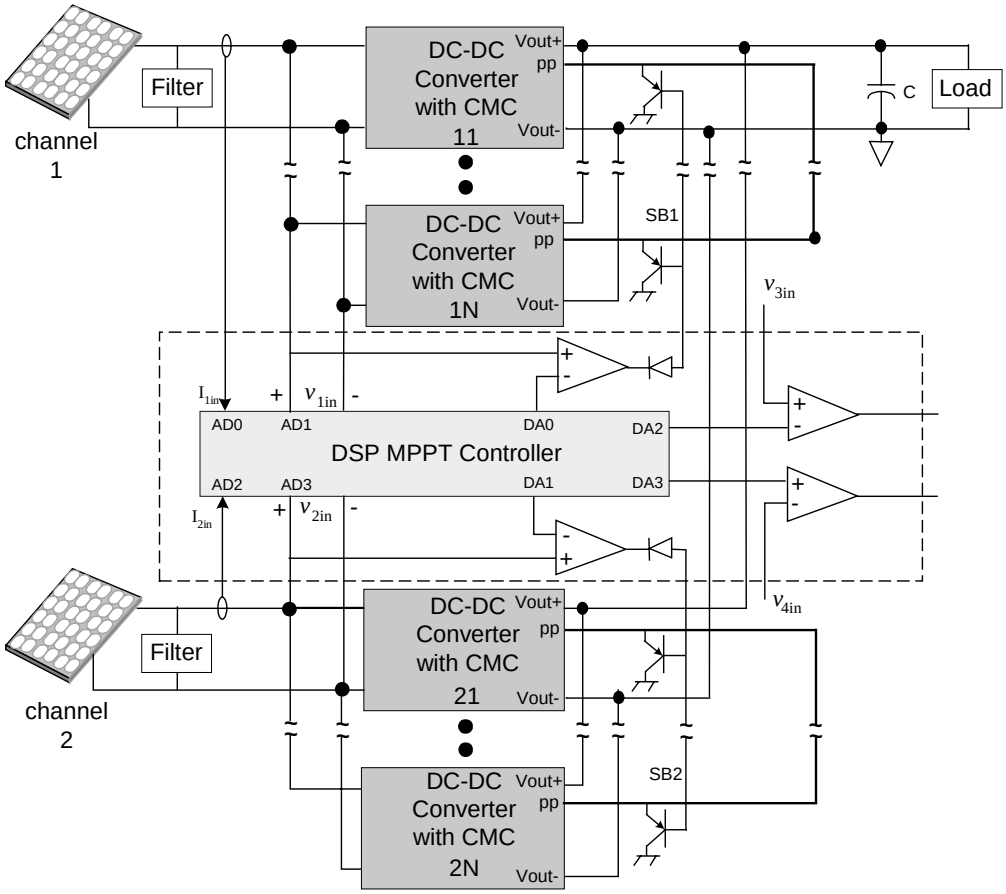


Figure 4.9: Basic Configuration of Paralleled Converters with Multiple Peak Power Tracking Control

When the load demand is light enough, one of the channels will regulate the output bus, while the remaining channels are idle. The relative output reference voltage among the channels determines the channel will regulate the bus voltage. As mentioned earlier for DC-DC within a solar channel, the effective output reference voltage of DC-DCs with shared-bus tied is given by the DC-DC with the minimum reference voltage. For across the solar channels, the shared-bus lines are not common. However, the output voltage compensators of all the channels sense the same output voltage from the common

output bus. In this case, the channel that will regulate the bus is the one whose effective output reference voltage is the highest among the channels. It will attempt to raise the output voltage to meet its inner output reference voltage; thus it causes the DC-DCs of the other channels to shut down.

As the load demand increases and exceeds the available power from the first channel that to regulate the bus, that channel will enter MPPT mode of operation. Subsequently, the channel with the next highest effective output reference voltage will regulate the output bus. As we have seen previously, the channel operates in MPPT mode will have as output current with ripple due to the effect of the dither injection. The channel that just regulates the output bus will compensate for the output ripple from the channel under MPPT by providing an output current with ripple opposite in phase. As a result, the channel under OVR will have a ripple superimposed on the operating point (voltage and current ripple) at the solar source terminal.

In the case that the load demand power exceeds the total power available from all channels, all channels operate in MPPT mode. The individual channels will work independently to properly track the maximum power point of its corresponding PV array. For a decrease in the load demand, each solar channel leaves MPPT mode and enters OVR mode in the reverse order.

4.5 Advantages of a MPPT Controller Per Channel Approach

A controller-per-channel approach has many advantages. Specific application examples for PV applications are given to help illustrate each case. 1) It has a better utilization on a per channel basis. Each converter module can independently control and so optimize the power flow to or from its source. For a battery charging system, each converter can independently and optimally charge its connected battery, reducing equalization time and increasing charge efficiency. In a solar power application, each converter can independently perform MPPT for its solar source. In an otherwise ideal installation, this will compensate for mismatches in panels of similar manufacture. It offers the further advantage of allowing panels to be given different orientations and so allow new possibilities in architectural applications. The greater tolerance to localized shading of panels is achieved. These reasons taken together are the most important advantage of per-channel distributed converters in PV applications. 2) A hybrid system with different sources becomes possible. Independent and intelligent power flow control can decouple each source from the others. Existing PV channels could be expanded by adding new higher output panels without compromising overall string reliability or performance. 3) Protection of power sources can be applied on a per source basis. For example, a weak battery can be protected from permanent damage during deep discharge. A single shaded PV panel can deliver its reduced power rather than being bypassed by a diode for its own protection. 4) An intelligent converter module can bypass a failed source or indeed a failed converter if appropriately designed, allowing the complete

installation to continue operation at a reduced capacity. 5) Each power source/power converter module will have an inherent data collection capability and most likely a control network connection, so that data gathering and reporting will add minimal additional complexity or cost. PV panels or batteries requiring inspection or replacement can be individually identified. 6) Greater safety during installation and maintenance is realized. Depending on design, each converter module may be able to isolate its connected power source, so that the wiring of series or parallel connections of these modules can be performed safely. The power source-to-converter connection is a safe low voltage connection.

4.6 Advantages of DSP-based MPPT Controller

The benefits of a DSP-based MPPT controller can be numerated as follows: 1) Improved Signal to Noise Ratio (SNR); 2) Inter-modal system stability since operating points are very repeatable and free from life and environmental drift; 3) Easier for control laws optimization; 4) Minimum system complexity since multi solar array sources share one DSP with different internal A/D and D/A conversion channels.

CHAPTER 5: SYSTEM SIMULATION AND VERIFICATION OF DIGITAL CONTROLLER

Digital controllers offer many advantages over their analogue counterparts, such as improved system reliability, flexibility, ease of integration and optimization, and communication capability. A system based on a digital controller will require fewer components, which will increase the reliability of the system. For example, all the components for the feedback loop can be eliminated and are replaced by software programming. The added capability of monitoring protection and prevention will also increase the system reliability. The use of software to change the controller functionality makes a system based on a digital controller very flexible. The digital controller offers the ability to change any parameters on the system in order to meet new requirements, or to optimize and calibrate the system. In this respect, tools used to verify correct behavior of the software code become essential to the design and development process.

Even though conventional methods of simulating of the process and digital control algorithm are beneficial in the initial state of development, verification of implementation on actual hardware will increase the confidence in the success of the system hardware prototype. Digital control brings about numerous benefits; nevertheless, it also brings additional complexity to system analysis, simulation, and design. Furthermore, effects of delays and the data converters' characteristics in the signal path sometimes cannot be ignored.

As one of the first steps, off-line simulation is performed. Several software tools exist, and they can readily represent power electronic apparatus and power systems. Even though existing tools do not allow complete simulation of all schematic components, critical portions can be simulated to verify the circuit operation. Circuit-level simulation is used to obtain performance information such as transient response, cross regulation, and stability. Such tools also provide facilities to represent basic control logics and algorithms for digital controllers. Various choices of processors for digital control systems are available; including general-purpose processors, microcontrollers, field programmable gate arrays (FPGAs), digital signal processors (DSPs), reduced-instruction-set computing (RISC) processors, and parallel processors. The development of a comprehensive representation of all instruction sets and/or functions of a digital controller for simulation studies is a challenging task, and is prone to skepticism with respect to the accuracy of the results.

Detjen et al. [21] describes a method to interface a plant simulator, PSPICE, and use C-source code for algorithm calculation. We can take a step further by implementing it in a real digital controller hardware environment. We can utilize the readily available communication capability of the controller as a data link path. Once hybrid simulation is performed satisfactorily, our approach leads to selection of system parameters and peripheral devices, such as clock frequency and data converters. Minimizing the clock frequency in a high-speed system will help reduce induced-noise in the system. In addition, the timing information is a good approximation for digital controllers in the same family or in those with similar core processors. In analog implementation the

output from the controller is available almost instantaneously after receiving an input signal. Furthermore, the output from an analog "circuit" has continuous signal resolution. However, for digital implementation various timing delays and quantization effects should be analyzed, since they have effects on stability [22].

This section presents a method to co-simulate a plant model on a computer with algorithms running on actual hardware. The effects of discrete sampling times and calculation delays caused by the processor can be accurately analyzed. Source codes for the final application can be developed and verified with the "virtual plant" in the co-simulation environment prior to testing with a real power stage prototype.

5.1 System Modeling

5.1.1 Behavioral Modeling of Analog Power Stage

The issue of synchronization between the output signals for firing power electronic switches and the timing for digital controller operation is important. The lack of such synchronization can lead to inaccuracies in the simulation results. Our approach is to use a variable time step for a power stage system level to accommodate analog circuit simulation, while we manually model events that will trigger operation of digital control sections. The variable time step nature allows for small time step simulation of highly nonlinear nature of the circuit, while it allows relatively large time step in some

other cases. For accuracy we can also specify the maximum step size for the transient analysis. Fixed time step can also be used, but care should be taken. Inaccuracy can arise from mismatch between the simulation points and switching instants [23].

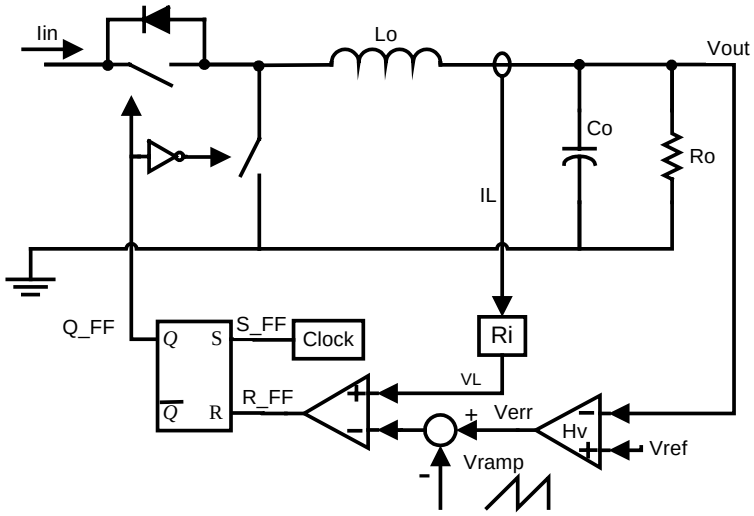


Figure 5.1: Example of behavioral modeling

With the understanding of the basic power circuit operation, often it is sufficient to model its behavior. This approach is suitable for concept verification and system level study. Behavioral model has different levels of detail, such as ideal-model and average model, with trade-off between them. For the ideal-model method, power switches are modeled as ideal, and circuit parasitics are neglected. Figure 5.2 shows an example of key waveforms of the peak-current mode control in Figure 5.1 using an ideal switched-circuit, for example. The converter model is simulated in the time-domain and its operation is verified. At the beginning of every cycle, the signal of the high-side switch turns on with the flip-flop output, Q_FF, which is set high by the signal S_FF. The inductor current, i_L, starts to charge. This measured inductor current through a sensing

resistor, R_i, is continuously compared with the difference of a ramp signal, Vramp, from the error signal, Verr. Once the two quantities become equal, the signal, R_FF, output of the comparator changes to high; it thus resets the output of the flip-flop, and subsequently turns off the high-side switch. The inductor current then discharges, and starts to charge again at the beginning of the next cycle. The low-side switch operates in complement with the high-side switch.

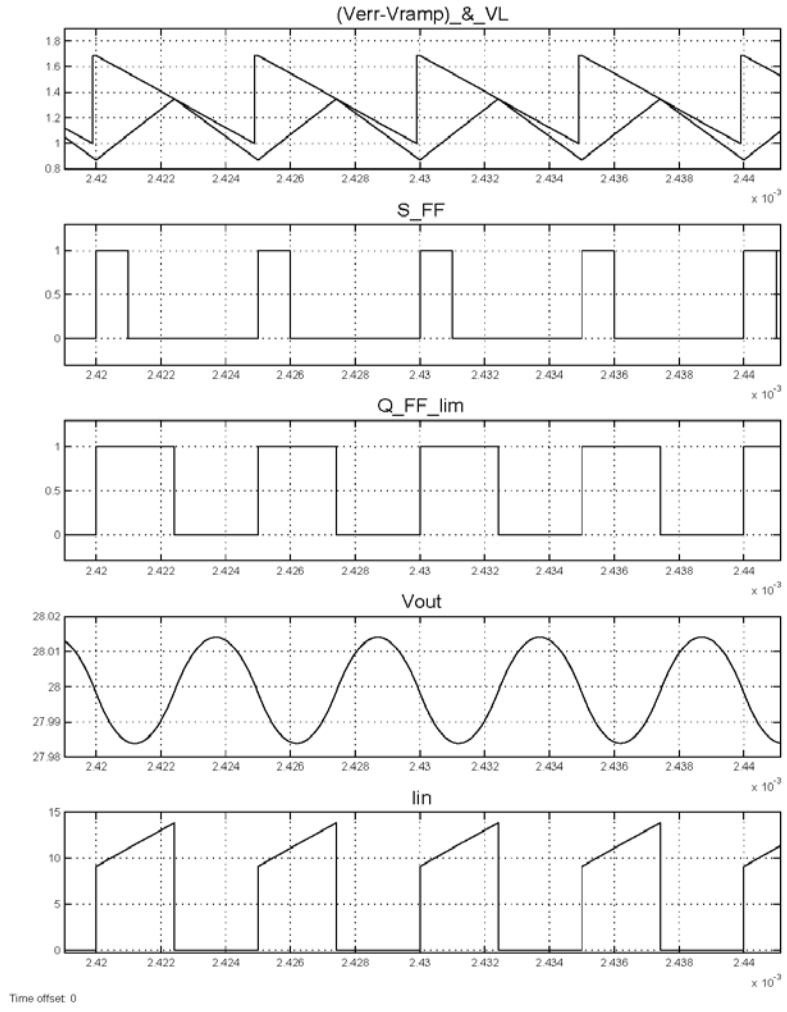


Figure 5.2: Power stage peak-current controlled steady-state waveforms (a) (Verr-Vramp) & VL, (b) S_FF, (c) Q_FF, (d) Vout, and (e) Iin.

5.1.2 Digital Control Portion

A general structure to incorporate digital control for a plant, such as a power stage, is shown in Figure 5.3. Data converters are necessary to transfer a signal from analog to digital domain, and vice versa. The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) perform those functions, respectively. Calculation is done inside the digital controller, which can be a DSP, FPGA [24], etc.

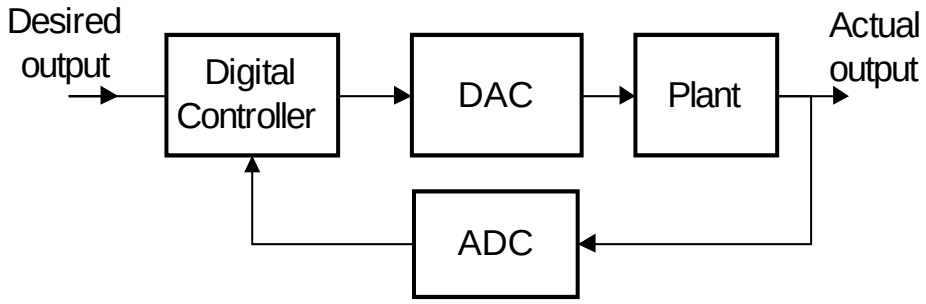


Figure 5.3: Typical digital control configuration

Initial modeling of the data converters' characteristics can include effects, such as static performance, delay effect, sample-and-hold, quantization, and input impedance, and etc. [25]. To achieve better modeling of the data converter, experimental data can be incorporated into the simulation. Dynamic characteristics, such as frequency response, can be performed experimentally and then modeled on the computer for ease of further analysis.

To test ADC frequency response, we can use sweep the frequency of sinusoidal from a known source VADC_input, take the converted value as the output VADC_output, and then compute the response [VADC_output / VADC_input]. For the

DAC, we can test by applying “white noise” as the source, and we can measure the output. The source of white noise can easily be generated by digital algorithms.

5.2 Proposed Co-simulators’ Data and Time Synchronization

In a typical real-time system, the controller reads system variables (voltages or currents), usually via an A/D, and issues control signals to the system. All this operation follows a master clock. In creating a co-simulation environment, we must take into account that a general-purpose computer is not designed for real-time processing. Therefore, we must develop a plan to coordinate the data flow between the computer and the digital hardware so that it will match the timing of the actual system. Furthermore, since the computer cannot produce analog signals, the A/D readings must be placed in the controller memory and point the controller to read from that location. The computer must also provide a signal to the digital signal processor (DSP) to initiate the data processing. In the more general case where multiple interrupts are needed, then a vector type interrupt can be used.

A general guideline for computer-DSP data synchronization follows a memory-mapped concept. General-purpose digital controller will have memory section mapped to specific external peripherals, and its content corresponds to its state. For the purpose of computer-DSP communication, additional user-defined variables will substitute those memory-mapped section and is read from/write to.

To synchronize the interaction between the plant simulator and DSP, co-simulation requires customization. The timing of each section at times is not directly compatible. The most critical tasks are coordinating "time" and passing control back-and-forth between them. Plant simulator with variable time step will take control of the overall operation: running the simulation, and requesting information from the DSP on an interrupt based approach. As the DSP operation is expected to be much faster than the pace of plant simulator, the DSP is usually idle and is only excited for small periods of time. This configuration should force the DSP chip operation to follow the pace of the plant simulation. This section describes typical timing for real-time system, which is based on regular interval interrupt. However, multi-event-based timing can also be modeled. In DSP one can identify the source of interrupt via interrupt control register(s), for example, by reading certain bit of the register. Extending the idea to multi-source interrupt, the computer can send extra information to the DSP to indicate the interrupt source.

A block diagram of the co-simulator is shown in Figure 5.4. The "plant real-time clock" represents the base-time (the plant's time reference) in the plant (power system). The "synchronized master clock" is derived from the real-time clock and it synchronizes the timing of operations taking place in the plant simulator (computer) and in the controller (DSP processor). The user can provide a set of input parameters to the plant simulator. In the case of the power system, such a parameter could be temperature, loading, etc.

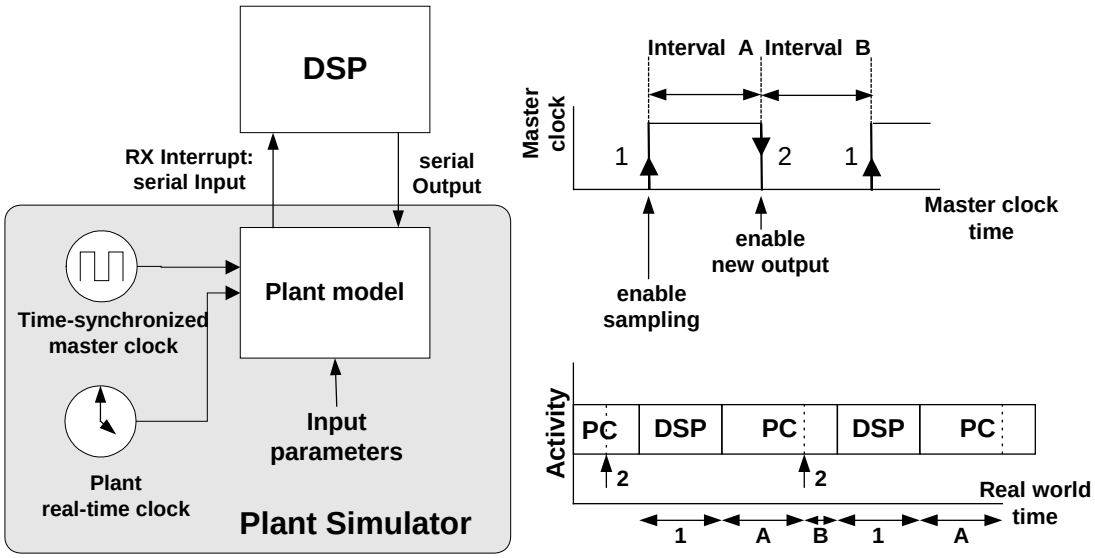


Figure 5.4: Timing details for co-simulation

The computer communicates with the DSP hardware via a bus, for example, via a serial port operating in asynchronous mode, transmitting 8-bits at a time at a baud rate of 115,200 bps. The input data frame to the DSP is preformatted to have voltage and current values sent by the computer, 16 bits for each value for convenience. Since a typical ADC used in these applications has less than 16-bits of resolution, then a set of bits out of the 16 transmitted bits are used in a way to match the bit format of the actual ADC on the DSP board. The plant simulator transmits data to the DSP to be processed and it then pauses the simulation and awaits data from the DSP. The DSP is programmed to read ADC data sent by the simulator, instead of from the actual ADC register. During simulation the DSP is idle and upon receiving the first byte, a serial port-received interrupt (RX) signal the DSP to enter the receive data routine and begin computing new control parameters. When the computation is completed, the DSP transmits back to the plant simulator which is awaiting for the data to arrive. As illustrated in Figure 5.4, the

DSP portion of the co-simulation begins with the rising edge 1 of the master clock that marks the actual sampling instance of the ADC. On the falling edge of the master clock (instance 2), the control variables from the DSP will be transferred to the simulator in a fashion that emulate the DAC update. Therefore, the master clock high time (interval A) represents the calculation delay of the digital controller, and the low portion (interval B) represents the idle time between DSP updates. The next sampling instance will be again the rising edge 1 of the master clock.

The co-simulation events as described above occur sequentially, i.e. the DSP and the host computer take turns in computing variables. However, in the real system the digital controller (DSP) and the plant operate in parallel, i.e. the plant never stops. It is therefore necessary to model the computation time of the DSP in the simulator so it can be taken into account.

In master clock time reference, the sampling and calculation is done "instantaneously", but the new output will be used after an interval of time later. With respect to the real world time, calculation activity on the host computer and the DSP occurs successively. The DSP takes time to calculate algorithms on-board in the interval 1, and the new output is sent back to the host computer. The host computer runs the simulation using the previous output from the DSP for an interval of time, A. At instance 2, the host computer uses new output received at the end of interval 1, and continues to run the simulation using the new output for an interval of time, B. The process repeats until the simulation final time is reached. The DSP is inactive during the interval A and B, and the host computer is idle during the interval 1.

In general, depending on the control process, the DSP execution time may vary. For the simulator to account for the DSP calculation time a timer on-board the DSP can keeps track of the number of execution cycles, and then passes this information to the simulator. Typically more than one timer is available for real-time operation. We can set one up to time the algorithm execution from start to finish. Upon exiting the algorithm, the timer's counter can be read to obtain the number of execution cycles used. The execution time then can be found from the product of the number of execution cycles and the clock period. In order to use the delay simulation, the customized DAC interface receiving and transmitting code must be modified. The host computer can subsequently use this information to determine the proper update time for DAC, the rising edge instance.

The operation of digital control portion is set to be trigger by a master digital clock, and is updated only on the rising/falling edges events. The continuous time system and the discrete time are guaranteed to solve at the same time instance of edges events. In other words, the continuous and discrete models will simultaneously generate simulation results on these events, and at other time the output of the digital system remains constant. In between two sampling times, only the simulation of the plant model (an analog system) is active. The solver is free to use a variable time step of any step size during this time.

5.3 Implementation and Results

The plant simulator is realized using SIMULINK with S-function as the communication link with the digital control hardware, TMS320LF24xx. Physical data link is via serial port, which is readily available on computer and general microcontroller.

Figure 5.5 shows the SIMULINK system block diagram operating in solar array voltage regulation mode, consisting of a solar array source, input filter, current mode DC-DC converter, load circuit, MPPT controller, and solar array voltage error amplifier. The solar array is modeled as voltage-controlled current source feeding by an IV characteristic look-up table. The load is of constant resistive type.

5.3.1 Power Stage Modeling

The behavioral power stage model shown in Figure 5.6 and Figure 5.7 is implemented using SIMULINK Power System Blockset [26], and run using variable-step integration method. Power switches are modeled as ideal and operating in complementary.

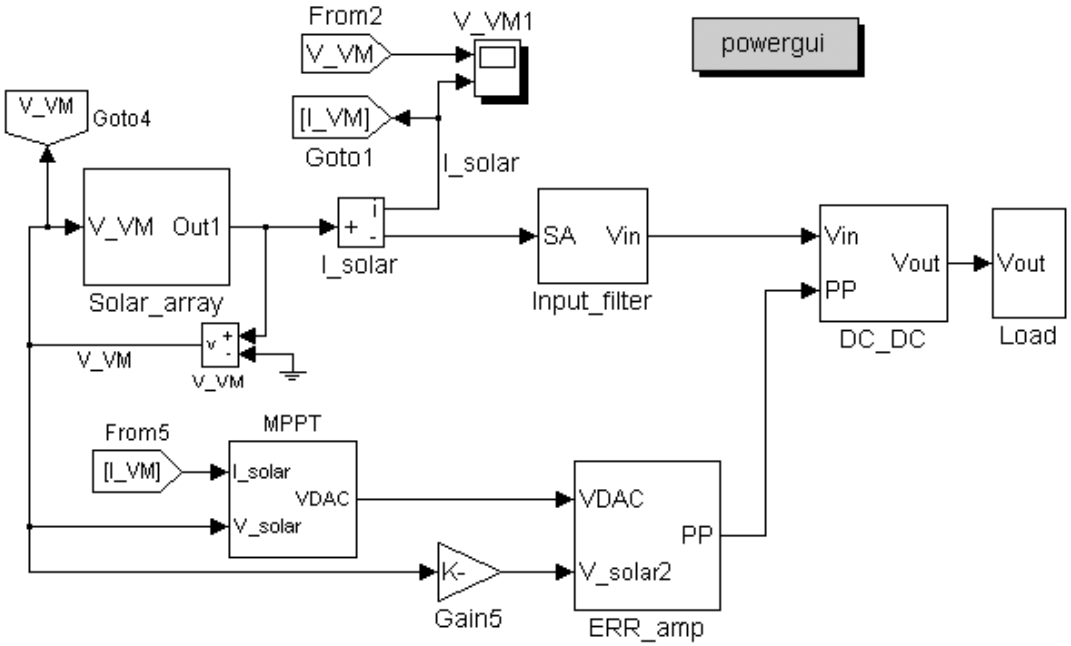


Figure 5.5: SIMULINK system block diagram

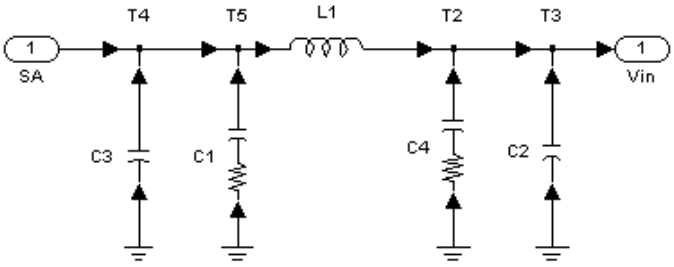


Figure 5.6: Power stage modeling – input filter

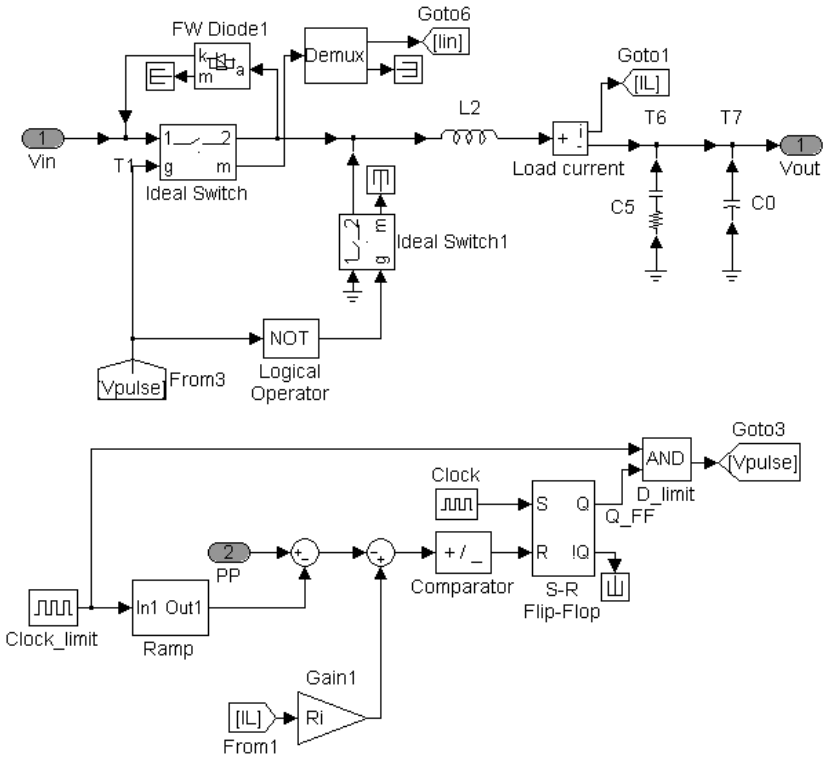


Figure 5.7: Power stage modeling – DC-DC

5.3.2 DSP Controller and Hardware

Digital control algorithm is executing on TMS320LF2407A EVM evaluation board from Texas Instruments. User-defined variables mapped to the peripherals (ADC/DAC) are RESULT[i_ADC]_sci and DAC[i_DAC]_sci, where i_ADC = 0 …15 and i_DAC = 0 … 3.

The TMS320LF2407A [27] is a 16-bit 40MHz processor with fixed point calculation capability.. The DSP chip has a 16 channels multiplexed 10-bit ADC with a built-in sample-and-hold (S/H) circuit. The minimum conversion time is 500ns. Each

ADC Conversion result is located in the 10 most-significant bits of the result buffer register, RESULTn [28]. A DAC7625 quad-output 12-bit double-buffered DAC is located on the evaluation board followed by a buffer [29]. The 12 least-significant-bit of a 16-bits must be written to the I/O space, and an extra data to transfer-register to transfer to output conversion. In addition to converting data to binary representation, those data alignment of ADC and DAC is performed inside S-function before data transfer.

5.3.3 Data Converters and Event Timing

Analog-to-digital converter is modeled with a zero-order-hold (ZOH), followed by a gain, and a rounding function. ADC input values has the voltage range of power supply of the DSP board (0 – Vcc_DSP). ZOH has the same sampling frequency as that of the interrupt frequency. The gain translates the sampled voltage into a number that can fill the entire ADC range corresponding to the resolution of the ADC, e.g. $(2^{10} - 1)$ / Vcc_DSP for 10 bits ADC. Rounding function can be {floor, ceil, round, fix}; thus allowing theoretical investigation of quantization effects. Digital-to-analog converter model consists of a gain followed by a saturation function. The gain translates the numerical value calculated from the digital signal processor to the voltage range of the DAC, and the saturation helps guarantee that correct range. Data converter implementations are shown in Figure 5.8.

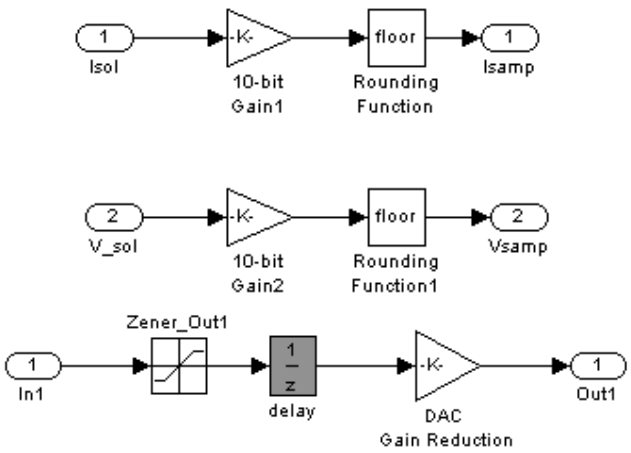


Figure 5.8: Data converters modeling

In actual DSP controller execution, the analog-to-digital conversion process can be triggered by different sources for start-of-conversion (SOC) sequence, such as software, event signals, and external signals. The EVA timer is used to trigger the SOC in our system, and the events are shown in Figure 5.9. Every sampling period time, Ts, ADC starts to convert the inputs according to the sequencer configuration. When the conversion is completed, ADC gives an end-of-conversion (EOC) signal and trigger the interrupt. The interrupt is responded and in the interrupt service routine DSP program begins to read the converted signal(s) in the result registers and do the calculation. During this time, we also setup the ADC registers for the next cycle, then wait for the next SOC.

For the proposed method, the ADC interrupt is replaced by event resulting from receiving data from the plant simulator, with the algorithm remains the same. The time between SOC and EOC represents delay in the AD conversion process, and the time between return and EOC as calculation delay. Source code is modified to have an I/O

signal XF as an indicator of the calculation delay. The signal XF turns low as the DSP enters the interrupt service routine, and toggle upon exit.

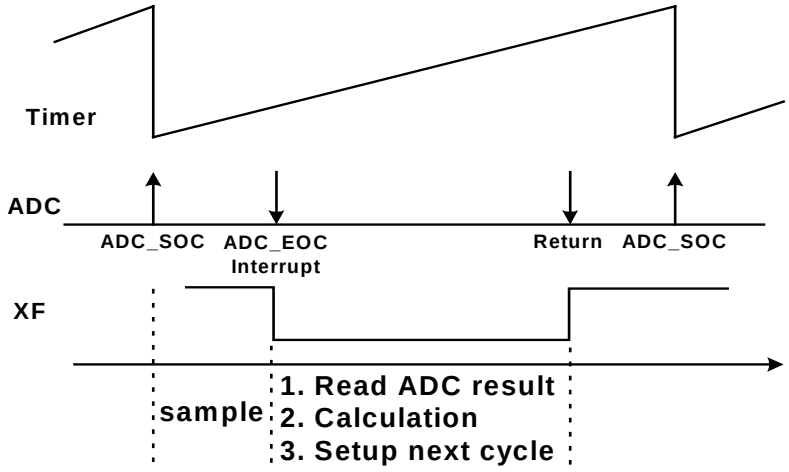


Figure 5.9: ADC timing inside DSP

5.3.4 Data Pre/Post Processing and Communication

S-function enables interaction with SIMULINK's equation solvers, and provides general-purpose block that can accommodate continuous, discrete, and hybrid systems [30]. SIMULINK passes arguments to an S-function, which includes the current time (t), the state vector (x), the input vector (u), and the flag (flag). During simulation of a model, SIMULINK repeatedly invokes an S-function, using the flag argument to indicate the task (or tasks) to be performed for a particular invocation. Each time the S-function performs the task and results are returned in an output vector (y). The list of possible

tasks are initialization, update state variables via integration, calculating the output of the S-function, calculating the next processing time, and termination.

```
switch flag,

    case 0        % Initialization
        Open_communication();
        Initialize_DSP ();

    case 3        % Calculate outputs

        Read_input_vector();
        Format_data_for_DSP();
        Send_data_to_DSP();
        Wait_for_DSP_data();
        Format_data_for_SIMULINK();
        Return_output();

    case 9        % Termination
        Close_communication();

End
```

Key functions example necessary for the proposed method are summarized, and The SIMULINK pseudo-code is shown above. In the initialization process, communication link is established, and DSP is initialized into proper state with initial conditions of data converter and variables given. Once SIMULINK invokes the S-function to calculate its output, the input is read from the input vector (u), and passed to the DSP with proper format. The DSP interrupts upon receiving data, performs the calculation using on-board algorithm, and returns the result back to the simulator. These are done while SIMULINK is waiting for the result. Upon receiving the calculation results, necessary data formatting is performed, then is returned as an output vector (y). When an end-of-simulation signal is detected, communication link is terminated.

The number in binary format for the communication can be adapted to the DSP hardware under consideration. For our case a 16-bit fixed-point number system is used in accordance to the TMS320LF24xx. The number of variables, their types, and number of bit representation are assumed known a priori to the user. Once the user decides the input/output data characteristics, the user can customize proper interface code for ADC data-receiving and the DAC data-transmitting on the DSP hardware, and ADC data-transmitting and DAC data-receiving on the host computer. The different resolutions for the data converters can be accommodated in their modeling on the host computer.

5.3.5 Key Waveforms

Figure 5.10 shows waveforms which are saved to workspace, and is re-ploted using MATLAB script file. Vref_scale is the scaled command signal from DAC. V_VM is the solar array voltage, which can be seen to follow Vref. Verr is the error signal from the solar array voltage error amplifier, and Vload is the load voltage. Tracing the solar array voltage and current to the I vs. V and P vs. V characteristics yield tracking near the maximum power point, as shown in Figure 5.11.

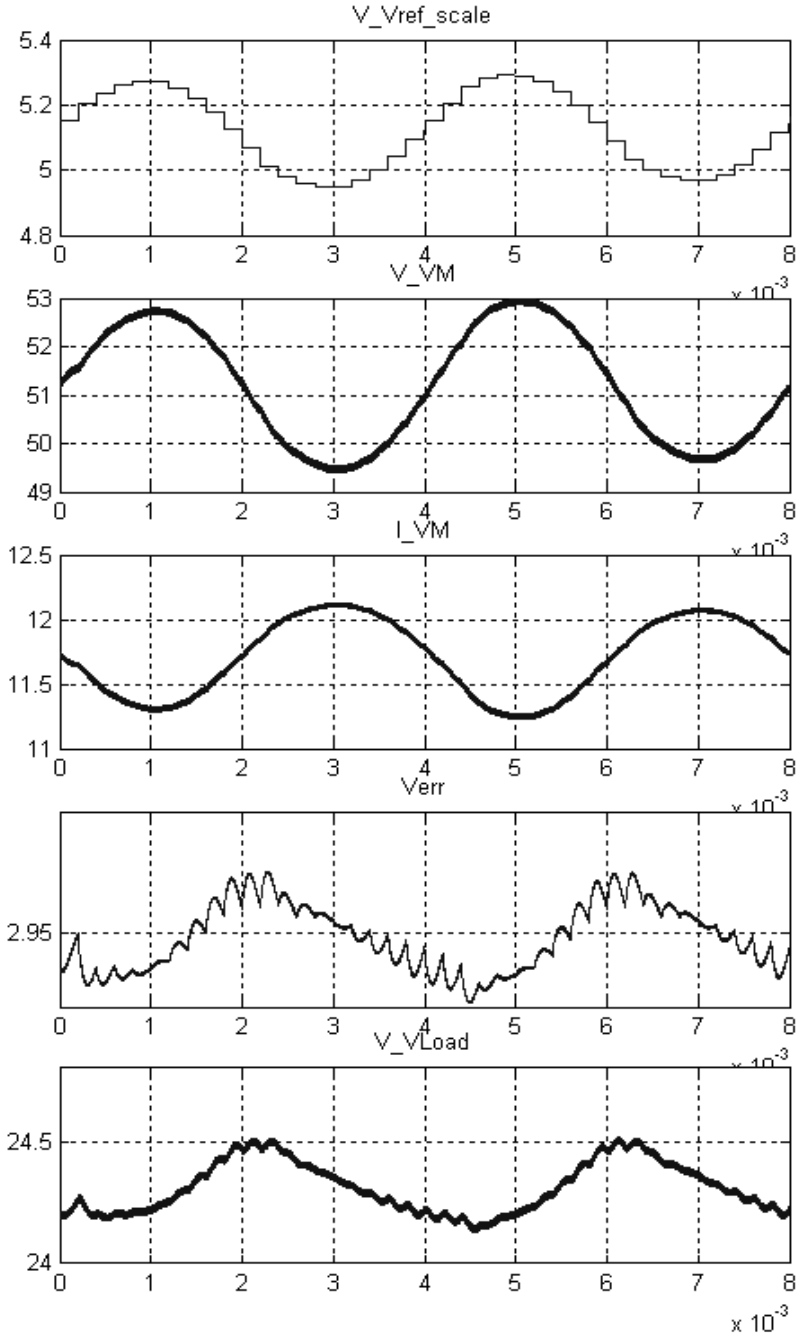


Figure 5.10: Co-simulation resulting waveforms

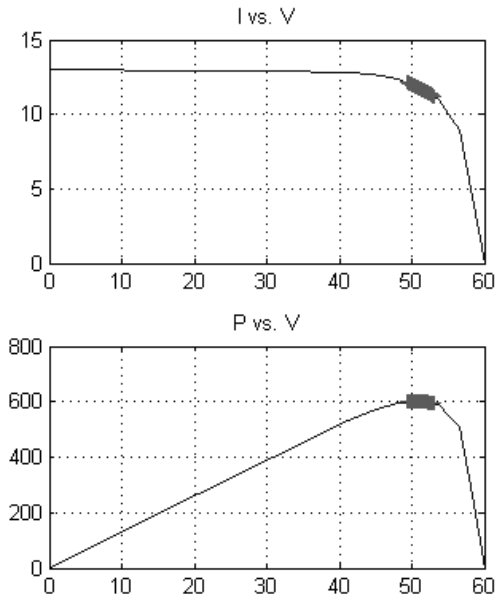


Figure 5.11: Co-simulation resulting I-V and P-V traces

5.4 Towards Experimentation

The co-simulation methodology presented in this chapter provides a valuable tool to evaluate the control behavior of a mixed signal system, such as the MPPT control. It allows verification of initial development of the embedded control coding. Modeling of the analog portion is done in a host computer. The methodology allows works between hardware and software development units to be performed in parallel, since some software debugging does not rely on actual hardware. The next steps are to build the required power stage prototype, to integrate various the power stage with embedded hardware, and to perform final tuning to the algorithm.

CHAPTER 6: IMPLEMENTATION AND EXPERIMENTS

A DSP-based controller dedicated to all the solar array sources is implemented to control their respective DC-DC converter modules. A single DSP hardware is used to track multiple peak power points of the distributed solar arrays. All the solar arrays' output voltage and current are fed into the DSP controller for tracking their respective array peak power. Each channel either automatically adjusts its operating condition to be near or at the maximum power point of its solar array source(s), or regulates its system output voltage when the net load demand is below the peak power. At the same time, nearly uniform current sharing among DC-DC converter modules connected in parallel is also achieved by the concept of shared-buses. In this distributed MPPT approach, each current mode DC-DC converter module has an additional control port for the purpose of MPPT. It is possible that, while many converter modules are operating in their output voltage regulation mode, the remaining modules may operate in MPPT mode individually, depending on the characteristics of their respective solar array sources. The benefit of single DSP-based MPPT controller reduces system complexity since multiple solar array sources share one DSP with different internal ADC and DAC conversion channels. The following sections describe the prototype hardware implementation of the outer solar array voltage loop, the inner current loop, and additional interface circuitry that connects the digital controller and the power electronics.

6.1 DSP Hardware Implementation

The TMS320x2xx family is optimized for digital motor/motion control applications. The DSP controllers combine the enhanced TMS320 architectural design of the 'C2xLP core CPU for low-cost, high-performance processing capabilities and several advanced peripherals optimized for motor/motion control applications. Notable features that are related to the current and future works are as follows:

- 20 MHz clock speed (50-ns Instruction Cycle Time)
- 16K Words × 16 Bits of On-Chip Program Flash EEPROM ('F240)
- 12 Compare/Pulse-Width Modulation (PWM) Channels
- Three 16-Bit General-Purpose Timers With Six Modes
- Three 16-Bit Full-Compare Units With Deadband
- Dual 10-Bit Analog-to-Digital Conversion Module (ADC) with 6.1us conversion time
- 28 Individually Programmable, Multiplexed I/O Pins
- Serial Communications Interface (SCI) Module
- Serial Peripheral Interface (SPI) Module
- Six External Interrupts (Power Drive Protect, Reset, NMI, and Three Maskable Interrupts)
- Four Power-Down Modes for Low-Power Operation

Texas Instruments introduced TMS320F240 in 1996, and this chip has successfully demonstrated its power in many applications since then. A military version of the TMS320F240 is also available as SMJ320F240, which is compliant with the MIL-PRF-38535 (QML) standard. TI provides extensive technical support on this chip and its related software, as we can see from the number of application notes and updated datasheets and user manuals.

The multiply-accumulate is common in signal processing, and is optimized for a digital signal processor. DSP can perform such function in a single clock cycle. Data

move (DMOV) for time delay is also efficient if we organize the memory next to each other. The 8 Auxiliary Registers (ARs) can be used as pointer to data memory, allowing fast access to memory location without taking any additional clock cycle. For example, we can load the register and at the same time select the pointer to point to a location.

Evaluation module (EVM), as shown in Figure 6.1, containing the TMS320F240 chip with external peripherals is available from Texas Instruments. The EVM includes 4 channels 12 bits DAC, external memory, 8 LEDs, DIP switches, etc. Multiple channels DAC allow control of multiple power modules corresponds to multiple solar sources. The resolution of the DAC relates directly to the step size C1. Extra components on the evaluation board and the accompany software, Code Composer, facilitate in the debugging process.

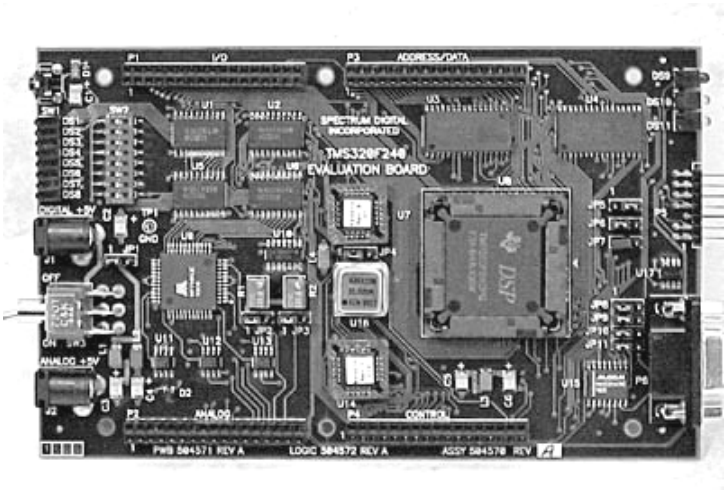


Figure 6.1: DSP TMS320F24xxEVM evaluation board

The 16-bit TMS320LF240 from Texas Instrument was chosen as the microprocessor for our prototype. This embedded device provides sufficient processing power for this application. To achieve high level of performance and to explore the

various control schemes and features made possible by operating in discrete time with a digital controller, including adaptive control techniques, a reasonably capable microprocessor is required. The components of the TMS320LF24xx control board employed in the system are described next.

In a digital control system, tasks such as sampling and command generation need to be synchronized to specific points in time. Others are event generated, such as shutdown or other precautionary measures taken when a certain condition is detected. Still other tasks, such as communication, system operation services, or computations carried out during intervals free of other processing tasks, have no time restriction.

The DSP chip has a 16-channels multiplexed 10-bit analog-to-digital converter with a built-in sample-and-hold (S/H) circuit. The minimum conversion time is 6.1us for a system using 20MHz clock. As is the case with other peripherals, the ADC is controlled by dedicate registers. Each ADC Conversion result is located in the 10 most-significant bits of the result buffer register, RESULTn.

A precision timer is used in the prototype to coordinate periodic sampling for the sampled data MPPT control. The TMS320LF240 contains two 16-bit timers that are capable of stepping every clock cycles, providing a maximum timing resolution of 50 ns. As preprogrammed times are reached by the timer, a software timer interrupt can be generated. When the interrupt is generated, time specific tasks, such as starting A/D conversion of analog inputs, are carried out.

The output of the MPPT controller computation provides the reference for the solar array voltage regulation error amplifier. One approach for interfacing the digital

and analog control loops would be to compute the command voltage inside the microprocessor and then convert it to an analog signal for the error amplifier. This approach would require the microprocessor to deliver samples to the voltage loop at a sufficient rate to provide the desired voltage set point.

DSP speed and memory size determines the possible degree of complication of the control algorithm. The resolution of the ADC relates directly to the sample value on the inputs (Vsa and Isa). It will determine the accuracy of the tracked operating point. The speed of the ADC will be the limiting factor of the control action. A 6.1us conversion time of the Texas Instruments TMS320F240 DSP chip limits the sampling frequency to about 160kHz.

Consider a processing time for a single channel is shown in Figure 6.2(a). Every sampling period time, Ts, ADC starts to convert the inputs according to the sequencer configuration. When the conversion is completed, ADC gives an end-of-conversion (EOC) signal and trigger the interrupt. The interrupt is responded and in the interrupt service routine DSP program begins to read the converted signal(s) in the result registers and do the calculation. During this time, we also setup the ADC registers for the next cycle, then wait for the next start of conversion (SOC). The time between SOC and EOC represents delay in the AD conversion process, and the time between return and EOC as calculation delay. Source code is modified to have an I/O signal XF as an indicator of the calculation delay. The signal XF turns low as the DSP enters the interrupt service routine, and toggle upon exit.

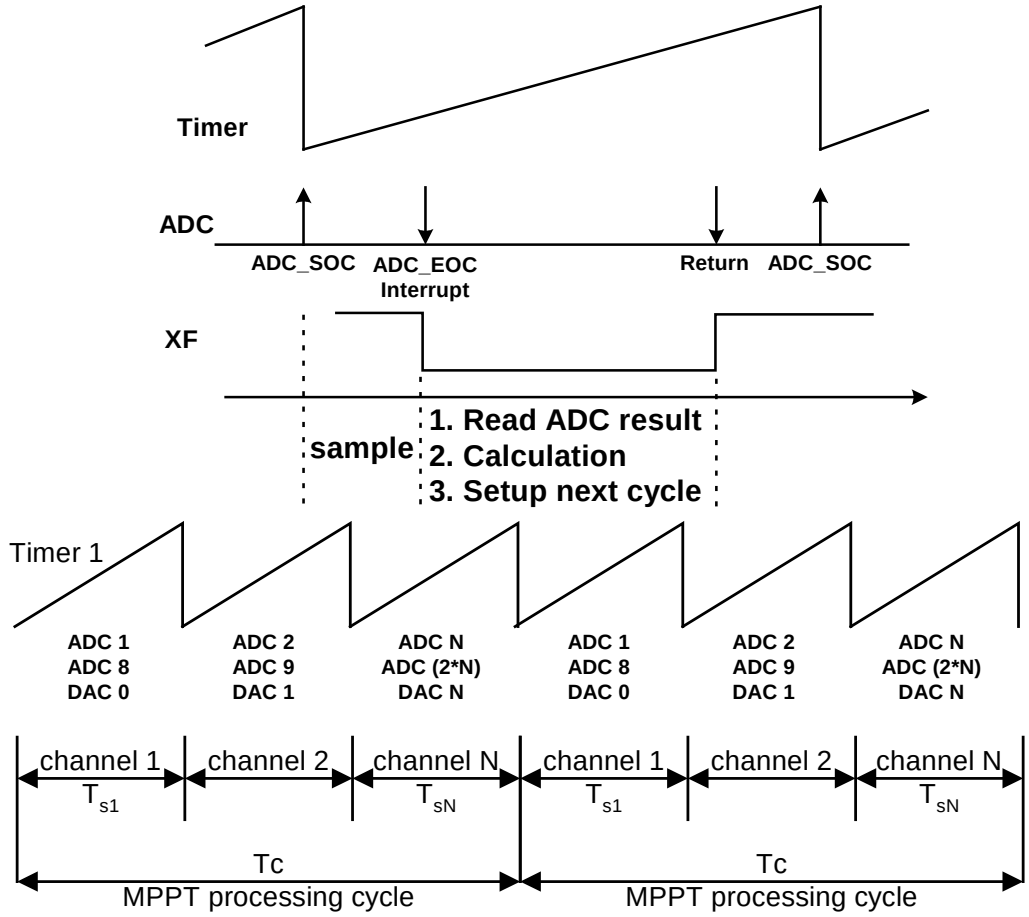


Figure 6.2: Timing (a) Single channel and (b) Time-multiplexed multi-channel

From the MPPT operation, we need 2 ADCs and a DAC per channel operation. Therefore, for an N-channel system, we needs 2*N ADC channels with N DAC. For design purpose, we must ensure that sufficient processing time is available for each channel. Thus, there is an upper limit on the maximum sampling frequency achievable. As an example, consider a N-channel system with an MPPT algorithm with processing time Ts. The maximum effective sampling period is Tc = N * TsN. The time multiplexing for multi-channel is shown in Figure 6.2(b).

For an efficient implementation, ADC interrupt is generated after it finishes conversion. A timer is set up to be in continuous up counting mode, and provide SOC signal for the analog-to-digital converter every period match. At the end of conversion, the ADC generates an interrupt signal. For the dual ADC, two feedback signals (voltage and current) from multiple solar sources can alternately be read by connecting the one of the two feedback signals to one of the lower 8 channels (ADC0-ADC7), and the other to the upper channels (ADC8-ADC15). In addition, proper bits in the ADC register need to be modified to select proper solar source channel. Referring to Figure 6.3, solar source channel selection must be done before the subsequent timer period match occurs. Auxiliary registers are used to facilitate memory address calculation to minimize the processing time. The guard time is intentionally left so that DSP can perform other functions. The fastest processing time occurs when this guard time is zero, and the ADC interrupt of for the consecutive channel arrives right after finishing with the previous channel. Possible interaction arises when at least one of the channels operates in output voltage regulation (OVR) mode, while the rest in MPPT mode. Channel(s) operate in current limit mode, providing output current according to a command voltage at its parallel pin. The channel under OVR will sense the combined current ripple and tries to provide an out-of-phase output current to maintain a constant output voltage. Effectively, reflected current will appear at the input of the DC-DC, which is the solar array terminal of the respective channel. During this time, we must ensure that the MPPT control is stop or set point voltage slowly moving to the left.

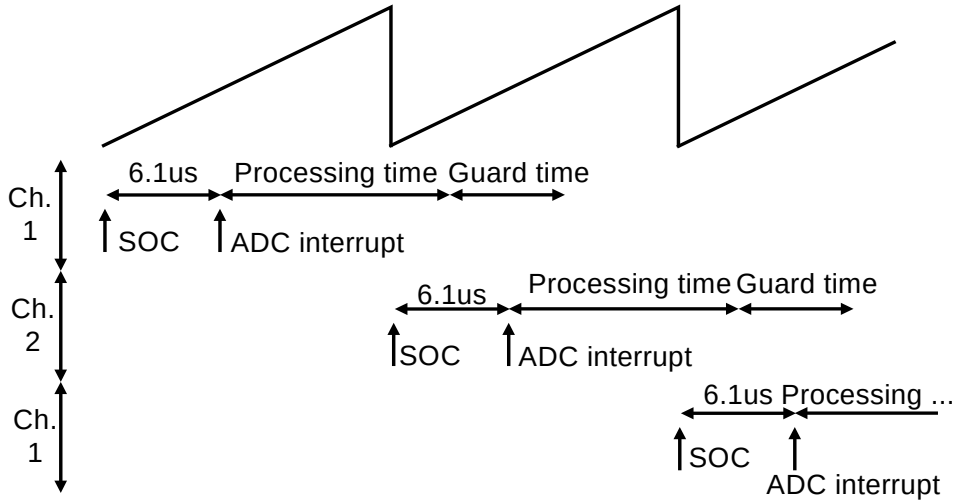


Figure 6.3: Detail timing of interrupt service routine for 2 solar sources case

6.2 MPPT Algorithm Implementation

Figure 6.4 shows a flow chart diagram of the P&O algorithm as it was implemented in the controlling microprocessor [31]. Small thresholds ε_1 and ε_2 are used when we test for change in the power and voltage, respectively. The value of the thresholds was determined with consideration of the tradeoff between the problem of not operating exactly at the MPP and the possibility of oscillating around it. It also depends on the chosen perturbation step width C_1.

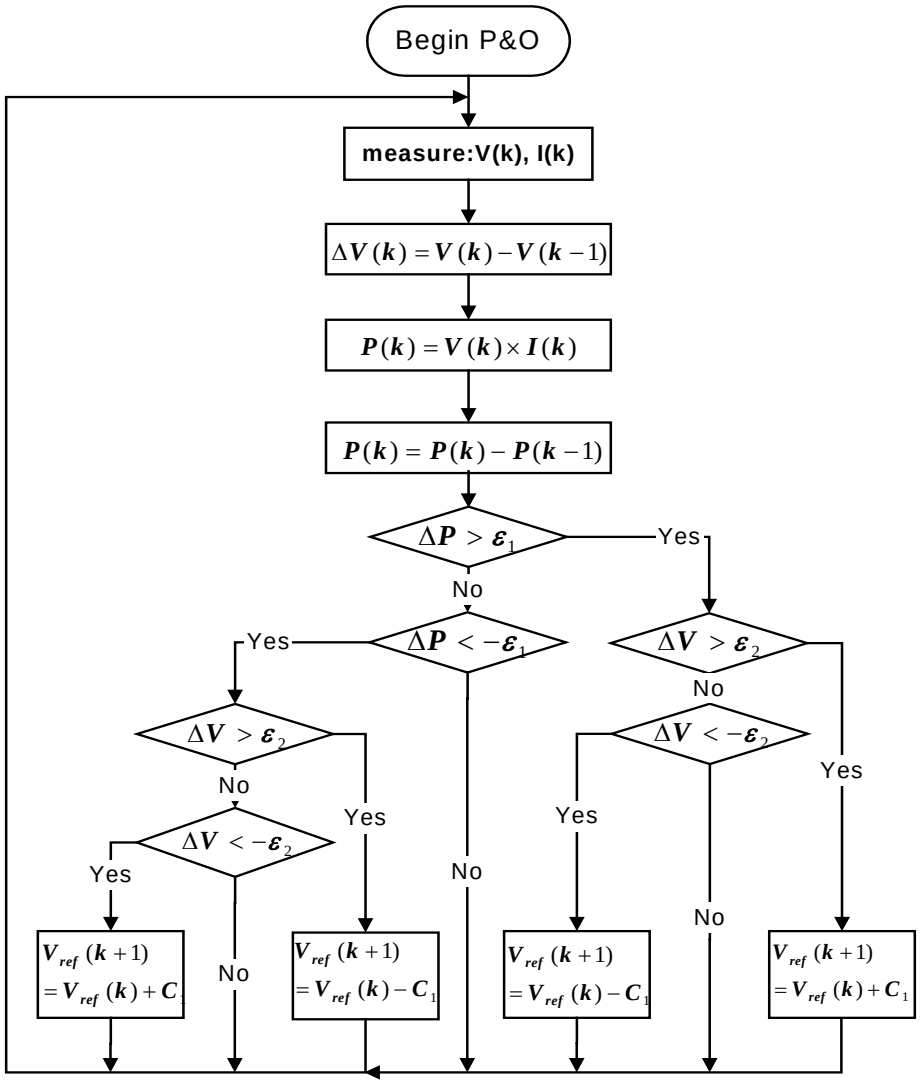


Figure 6.4: Perturb-and-observe implementation

6.3 Dither Signal Generation

The generation of the sine wave is performed using a look up table. To be able to control the frequency of the modulation with some accuracy, a method based on the modulo mathematical operation is used. The modulo mathematical operation is used

when there is overflow in the accumulator from the lower word to the upper word. When an overflow occurs, only the remainder (lower word) is stored. A 16-bit counter is used to determine the location of the next value. A step value is added to the counter every time a new value from the sine table is to be loaded. By changing the value of the step, one can control the frequency of the sine wave. The routine to load a new value in the compare register will be accessed at the same frequency as the timer signal, will be implemented inside an interrupt service routine. Phase shift can be realized by specifying the starting point for the counter. The frequency of the sine wave is proportional to the step size and inversely proportional to the size of the counter register and the period at which the routine is accessed and can be calculated by

$$f(step) = \frac{step}{T_s \times 2^n} \tag{6.1}$$

where f(step) is the desired frequency, Ts is the time period between each update, n is the number of bits in the counter register, and step is the step size used. A separate timer is used to vary the amplitude of the dither signal periodically, when desired.

6.4 Power Stage Hardware Prototype

Each power module, as shown in Figure 6.5, consists of parallel-connected DC-DC converters with conditioning circuitry. The conditioning circuit consists of circuit that scaled down the solar array voltage, Vsa, and a voltage from hall sensor for measuring solar array current, Isa. The scaled down voltages are in the range that satisfy

the specification of the analog-to-digital of DSP (0-5V). The biasing of the transistor is controlled by comparator with compensation. The input voltages to the comparator are that of the solar array, Vsa and from DSP board's digital-to-analog converter, Vdac. They are in the range of 0-5V corresponding to 36-60V. The Vsa signal from solar array and Vdac from DSP are isolated using opto-isolator. A current sensing path is also provided for measuring current output from one of the module. The solar array voltage-loop controller is implemented via analog compensation. The reference input command used by this loop is updated from the DSP

The HDM-45 DC-DC converters are COTS from Rantec Power System, Inc. The HDM-45 has 28V output voltage, 9A, 252W maximum output power, and it is a military-qualified product (MIL-STD-810C). The current-loop controller in the prototype is internal to the current mode parallelable COTS DC-DC using the Unitrode UC3843. The current reference is the output of the solar array voltage error amplifier. The input current is controlled to follow this reference value through a peak current mode control scheme. The output terminals of the DC-DC converters are tied together. The DC-DC converters have common current sharing pin, which is also tied to a transistor, which will be activate in the current-controlled mode.

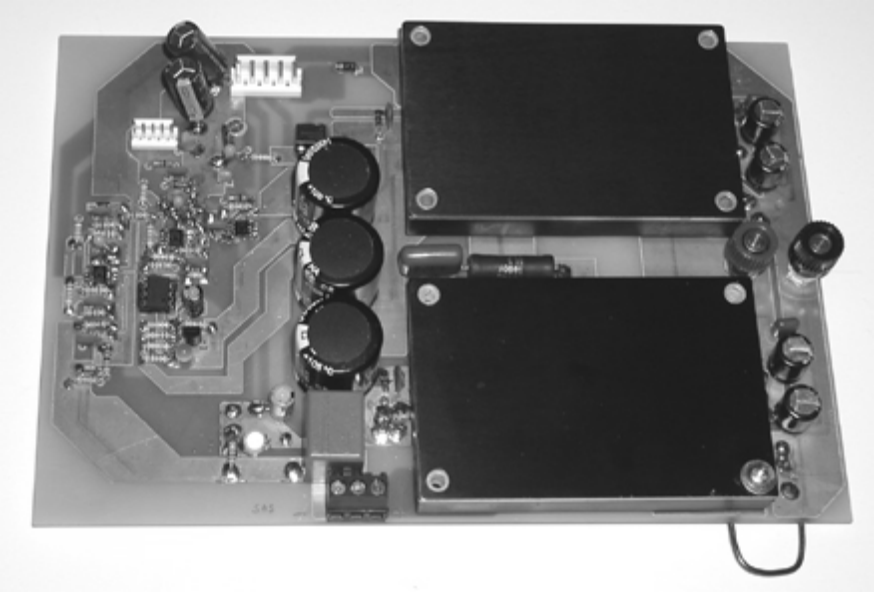


Figure 6.5: Power modules and conditioning circuit

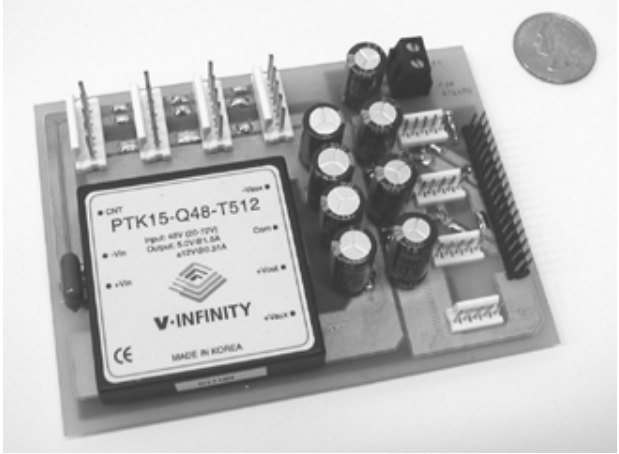


Figure 6.6: Auxiliary board

The auxiliary board, shown in Figure 6.6, serves two purposes: 1) Act as the central point where information is exchanged with the DSP. The solar arrays voltage and current information are collected and sent to DSP board. The control signal from DSP's digital-to-analog converter is distributed to the corresponding power modules. 2) Supply power for the DSP board and power modules conditioning circuit. DSP board utilized

+5V, and the conditioning circuit uses both +5V and ±12V. The auxiliary supply is connected to an external power supply (simulating backup battery) with output voltage lower than that of the power module. In MPPT operation mode, the input of the auxiliary board will come from this external power supply in lieu of the output of the paralleled power modules.

6.5 Solar Array Simulator

The E4350B maximum rating is 60V at 8A (480W). It is a DC power source that simulates the output characteristics of a solar array. The SAS is primarily a current source with very low output capacitance and is capable of simulating the I-V curve of arrays under different conditions (i.e., temperature, age etc.). The I-V curve is programmable over the IEEE-488.2 (GPIB) bus and is generated within the SAS. The SAS provides three current operating modes. In Fixed Mode, The SAS acts as a constant DC voltage source. In Simulator Mode, an internal algorithm is used to approximate a SAS I-V curve. In this mode, we need to specify four input parameters: Voc (open circuit voltage), Isc (short circuit current), Imp and Vmp (current and voltage at the peak power point on the curve). Figure 6.7 show an experiment scanning of the I-V curve using, Isc = 4.0, Imp = 3.6, Vmp = 48, and Voc = 60. The simulator is set to this mode for the experiment. In Table Mode, The I-V curve is set by a user-defined table of points. A table can have any length up to 4000 points (a point corresponds to a specific value of I and V). In Table Mode, current and voltage offsets can be applied to the selected table to

simulate a change in the operating conditions of the solar array. Using table mode, we can investigate the issue of local maxima. Figure 6.8 shows an experimental scanning of solar array characteristic with multiple maxima; thus demonstrate the feasibility of using the SAS to simulate such condition.

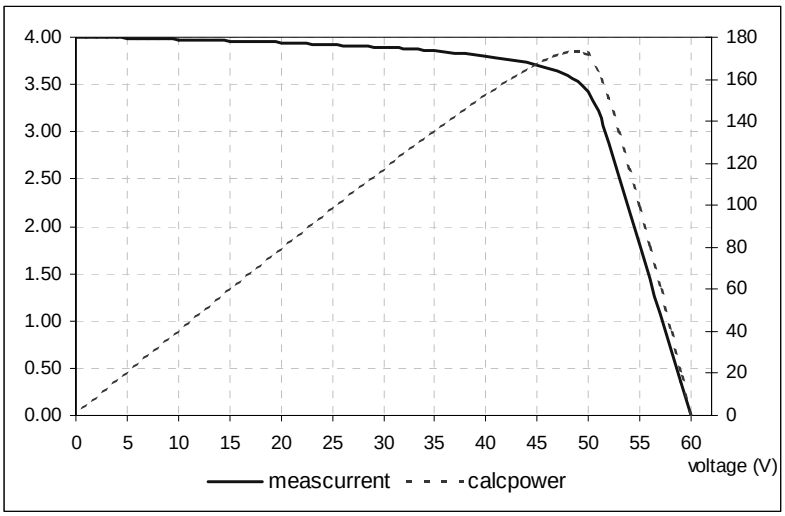


Figure 6.7: I-V curve from Simulator mode

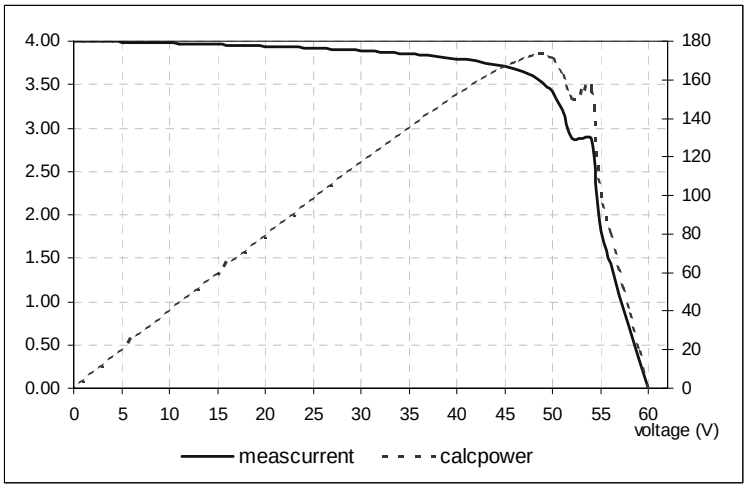


Figure 6.8: I-V curve from Table mode

A graphic user interface (GUI) was developed using Visual Basic for the communication with the solar array simulator, as shown in Figure 6.9. Through GPIB port, the computer controller can also communicate with the electronic load Agilent E3300A.

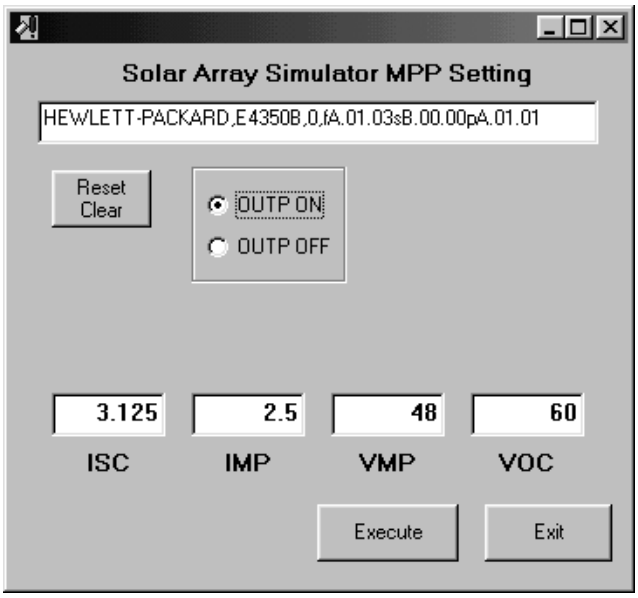


Figure 6.9: GUI for SAS control in Simulator mode

6.6 System Setup and Experimental Results

Figure 6.10 shows the overall system setup. The SAS is set to operate in Simulator mode, and the electronic load in current-mode. Figure 6.11-Figure 6.14 give the experimental results of power system with single solar array and two parallel-connected DC-DC converters. Figure 6.11 shows the dither signals from the DAC of the DSP board. This command signal is connected to the solar array voltage compensator.

The current sharing pin of the DC-DC converters takes control when the operating point is near the maximum power point. Figure 6.12 indicates the active current sharing method can achieve near uniform current among the paralleled DC-DC converters. The output current of DC-DC converter #1 is about half of the total output current. The innermost current mode regulation plus automatic master current sharing solution could be implemented to expand the power in distributed power system.

Figure 6.13 illustrated the dynamic response of the array voltage and array current, revealing transitions between the maximum power point tracking and output voltage regulation modes of operation. Figure 6.14 shows the trajectories of array P-V and I-V under MPPT operation. The P-V trajectory reveals the array output moving around its peak value resulted from added dither signal, which indicates the MPPT control, achieved expected performance. From the figures, 240W of the array peak power is transferred to the power system during the MPPT mode and 120 W of the array power is transferred during the OVR mode in which the system output voltage is regulated at 28V. During the MPPT mode, the output voltage loses its regulation and settles below 28 for this particular load condition without backup battery.

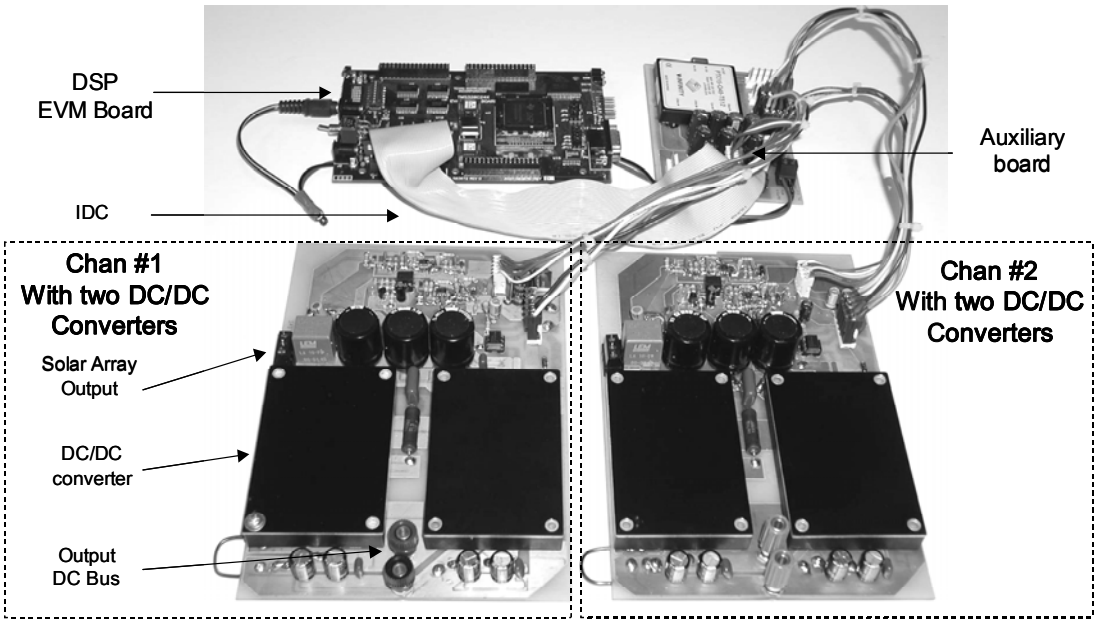


Figure 6.10: 500W Two solar arrays power system with DSP-based MPPT control

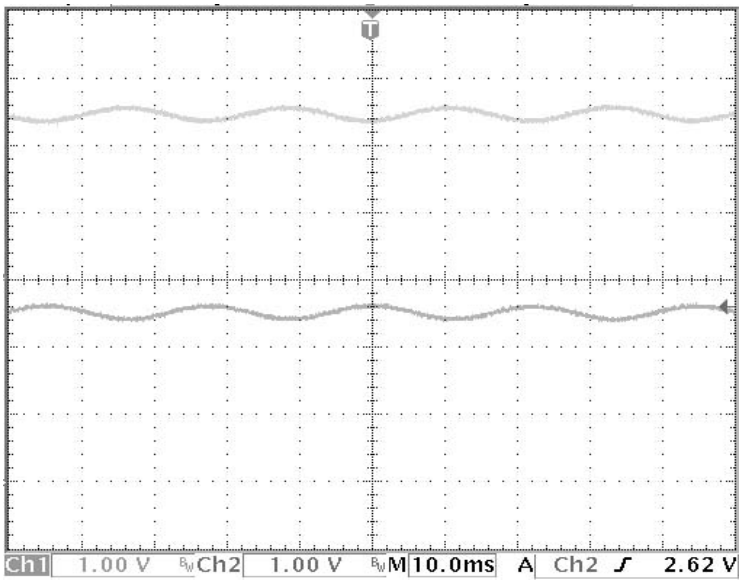


Figure 6.11: Dither signals

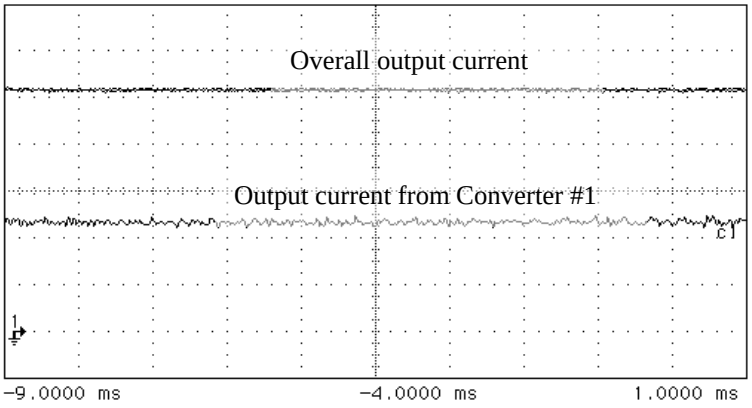


Figure 6.12: Current sharing among the paralleled DC-DC converters (2A/Div)

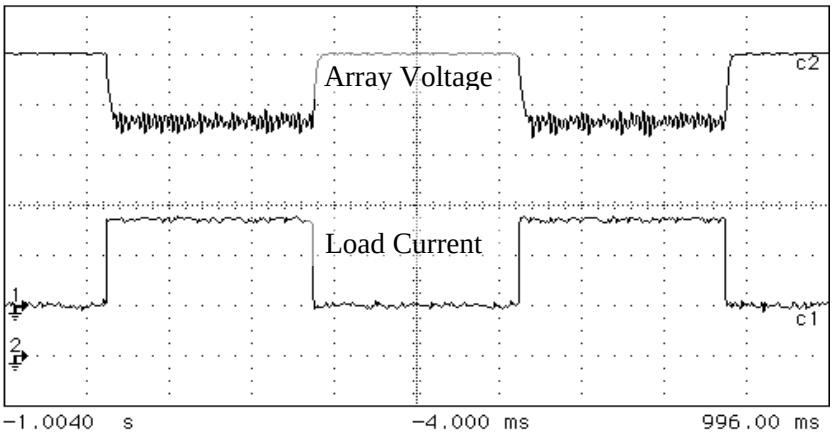


Figure 6.13: Dynamic response of array voltage and current
(Upper trace: 10V/div, Lower trace: 2A/div)

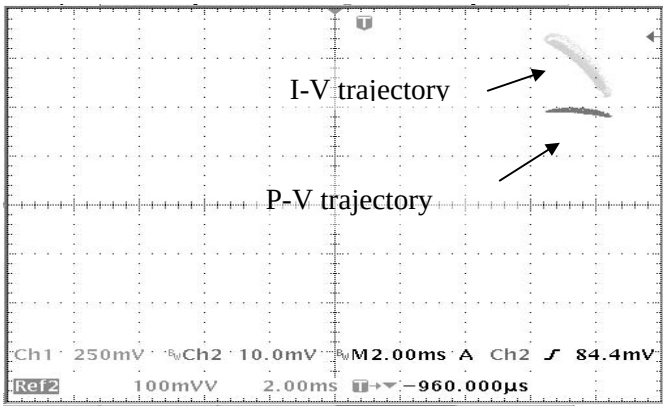


Figure 6.14: Trajectories of array P-V and I-V

Figure 6.15 and Figure 6.16 present the experimental results of power system with two solar arrays. Figure 6.15 indicates the commanding set point waveform for two solar arrays, where two periodical dither signals are superimposed upon the operating points of two solar arrays with the same amplitude and 180° phase shift. As afore-mentioned, the periodical dither signal with higher amplitude was implemented in the system to overcome solar array local maxima. Phase-shifted dither signal in different solar arrays, therefore, can deliver improved output performance since the output ripple caused by the dither signal could be cancelled by the counterpart unit.

In the scalable power system with distributed solar arrays, it is possible to have mixed-mode operations: simultaneous MPPT and OVR modes. To evaluate such a performance of developed power system, two solar arrays were deliberately set with different characteristics. Figure 6.16(a) shows the light load case. It can be found that for the solar array with less power rating, its output moving around its peak value resulted from added dither signal, while in the other solar array the two-converter modules are operating in their output voltage regulation mode. With the load increases, the operating point of another solar array also climbs up to its maximum power point, while the other one stays in its peak power point, as shown in Figure 6.16(b).

The experimental results validated the behavior of the constructed scalable power system with parallel-connected DC-DC converters and distributed solar arrays with multiple maximum power points tracking.

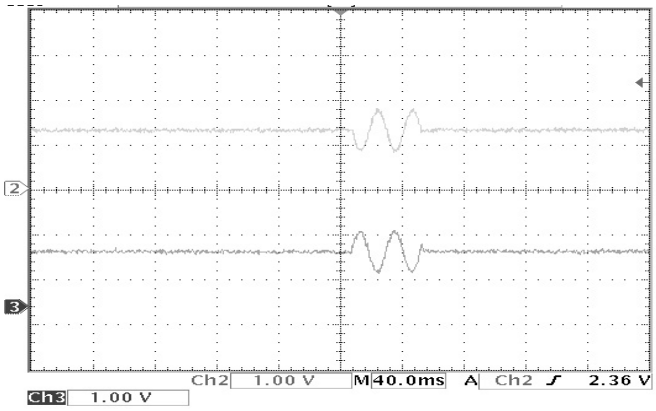


Figure 6.15: Operating point for two solar arrays

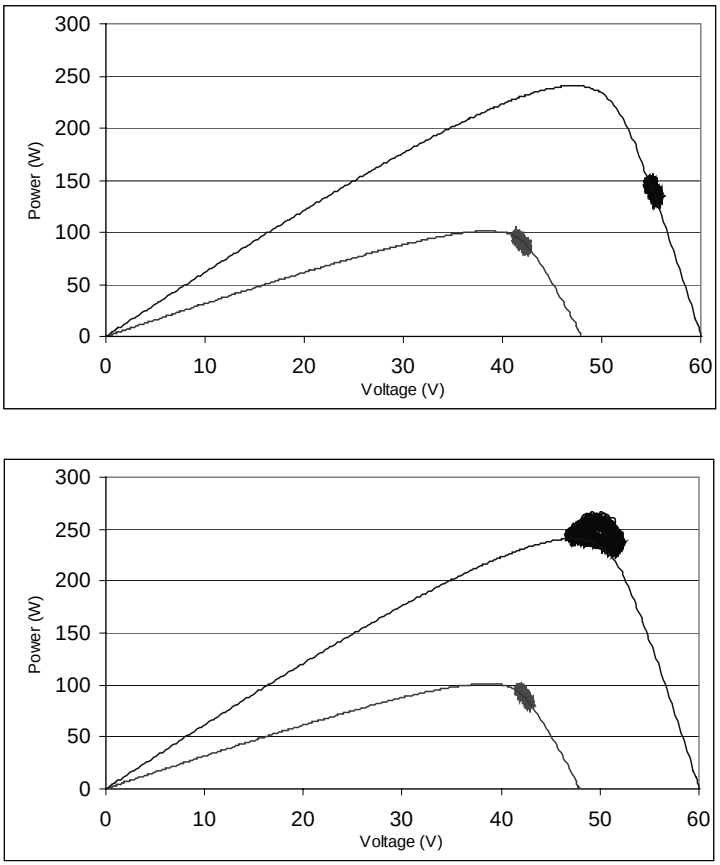


Figure 6.16: Two solar array's P-V trajectory under different loads
(a) Light Load and (b) Heavy load

CHAPTER 7: CONCLUSIONS AND FUTURE DIRECTIONS

A simulation methodology for automating the simulation of solar arrays is presented. Each cell in the array is individually modeled, thus permitting evaluating the effects of electrical mismatches between individual cells. An advantage of the proposed methodology is that it is based on commercially available software packages, and therefore it does not require extensive software development. In our implementation we have used MATLAB and SPICE. MATLAB is used to program various operational scenarios that are automatically transferred to SPICE for simulation. The results of the simulation are automatically returned to MATLAB for further analysis. Another advantage of the method is that various panel configurations as well as environmental conditions can be effectively modeled as two-dimensional matrices or as images. The presented examples demonstrate the versatility of the method. The proposed methodology can be an effective tool in designing and evaluating the performance of large panels.

A method for co-simulation between plant model running in a computer environment and digital control algorithm executing on actual hardware has been presented. Data exchanged between the two simulators is via any data communication link commonly available, and is done based on event-synchronized request. Data-logging enables system analysis at later time. The approach is demonstrated with digital

control based maximum power point tracking for a photovoltaic system. Applications and benefits of our approach can be summarized as follows. It provides freedom to debug and improve the algorithm without depending on the "real" power board and in-the-loop test and debugging capability. It facilitates the selection of data interfaces and can employ empirical characteristic in modeling. It is applicable to general digital signal processors.

A DSP-based multiple peak power tracking for expandable power system is implemented. In the system, multiple solar arrays are connected to individual peak power tracker units, which composed of paralleled COTS DC-DC converters. Each of the solar arrays is individually peak power tracked with an improved MPPT algorithm. The outputs of each of the individual tracker units are connected in parallel. In such a power system, new solar arrays may be added to the system in a modular fashion simply by adding additional tracker units and adjusting a control routine to account for the additional units.

With the developed automation tools for solar array simulation, there are numerous applications toward manufacturing, system study, and advanced MPPT method. One extension is to apply automated solar array simulation tool in the design of real-life panel configurations. Semiconductor details of protection diodes and model of solar cells obtained from panel datasheet or via direct measurements can give a close representation of the I-V characteristics.

From interconnecting solar cell models we have seen that multiple maxima on the P-V curve can exist when illumination is not constant for all the cells. Tracking of the

global maximum is desire, but is challenging. With known or slowly changing illumination patterns on solar panels, the use of simulated shading test data is beneficial for training of learning controllers, such as neural networks. In such networks, data set composing of input(s) and desired output(s) is presented for the training algorithm to adjust the coefficients internal to the network. The training is completed when the network can produce results closely represent the desired output(s). We may use illumination patterns on individual cells and the maximum power point voltage as the input(s) and desired output, respectively.

Monte Carlo simulations can be performed for analysis of performance of solar panels based on solar cells manufacturing tolerance. A Monte Carlo simulation uses random numbers to model process distribution. In manufacturing samples are taken to compare actual products performance with the specification that it has been designed for. From the measurements, distribution of parameters value is found, for example, equivalent parallel and series resistances. Integration of our automated tools with the parameter distributions allows study of worst-case performance of manufactured solar panels.

In co-simulation the calculations in the digital signal processing hardware is real-time; however, that is not the case for the simulation time of the plant model on a host computer. Power system with switching devices required small time step near the switching transition, so the total simulation time is lengthened as a result. Development of a simplified power stage and control laws is sufficient for a first step in control system design to evaluate performance parameters, such as stability. The control laws of the

power stage, voltage or current-mode, can be described in simple form using mathematical equations. Simulation time will be significantly reduced. The trade-off between mathematical complexity and simulation accuracy should be considered.

LIST OF REFERENCES

[1] N.D. Kaushika and N.K. Gautam, "Energy yield simulations of interconnected solar PV arrays," IEEE Transactions on Energy Conversion, Vol.18, No. 1, Mar 2003, pp.127-134.

[2] A. Abete, "Analysis of photovoltaic modules with protection diodes in presence of mismatching," in Photovoltaic Specialists Conference, 1990, Conference Record of the Twenty First IEEE, 21-25 May 1990, Vol.2, pp.1005 –1010.

[3] Slonim, M.A.; Shavit, D.S., "Linearization of the output characteristics of a solar cell and its application for the design and analysis of solar cell arrays," Energy Conversion Engineering Conference, 1997. IECEC-97. Proceedings of the 32nd Intersociety, Vol.3, pp.1934 –1938.

[4] V. Quaschning, R. Hanitsch, "Numerical simulation of current voltage characteristics of photovoltaic systems with shaded solar cells," *Solar Energy*, Vol.56, No.6, 1996, pp. 513-520.

[5] J.A. Gow and C.D. Manning, "Development of a photovoltaic array model for use in power-electronics simulation studies," *IEE Proceedings of Electric Power Applications*, Vol. 146, No. 2, March 1999, pp. 193 –200.

[6] Kasap, S.O. *Optoelectronics and Photonics, Principles and Practices.* Prentice-Hall, 2001.

[7] V. Quaschning, R. Piske, and R. Hanitsch, "Cost Effectiveness of Shadow Tolerant Photovoltaic Systems," EuroSun'96, pp.819-824.

[8] V. Quaschning and R. Hanitsch, "Increased energy yield of 50% at flat roof and field installations with optimized module structures," 2nd World Conference and Exhibition on Photovoltaic Solar Energy Conversion, Vienna, Austria, 6-10 July 1998, pp. 1993 – 1996.

[9] W. Herrmann, W. Wiesner, and W. Vaassen, "Hot spot investigations on PV modules-new concepts for a test standard and consequences for module design with respect to bypass diodes," in Photovoltaic Specialists Conference, 1997, Conference Record of the Twenty-Sixth IEEE, 29 Sept.-3 Oct. 1997, pp.1129 –1132.

[10] *Orcad PSPICE A/D – Reference Guide*, 1999.

[11] A.K. Sharma, R. Dwivedi, S.K. Srivastava, "Performance Analysis of a Solar Array Under Shadow Condition," *IEE Proceedings-G*, Vol 138, No. 3, June 1991.

[12] V. Quaschning and R. Hanitsch, "Influence of shading on electrical parameters of solar cells," in Photovoltaic Specialists Conference, 1996, Conference Record of the Twenty-Fifth IEEE, 13-17 May, pp.1287-1290.

[13] K.Y. Khouzam, Optimum load matching in direct-coupled photovoltaic power systems-application to resistive loads, *IEEE Transactions on Energy Conversion*, vol. 5, no. 2, June 1990, pp.265 – 271.

[14] J. H. R. Enslin, et al., "Integrated photovoltaic maximum power point tracking converter", *IEEE Transactions on Industrial Electronics*, vol. 44, no. 6, Dec. 1997, pp. 769-773.

[15] T. Noguchi, S. Togashi, and R. Nakamoto, "Short-current pulse-based maximum-power-point tracking method for multiple photovoltaic-and-converter module system", *IEEE Transactions on Industrial Electronics*, vol. 49, no. 1, Feb. 2002, pp. 217-223.

[16] K. Hussein, et al., "Maximum photovoltaic power tracking: an algorithm for rapidly changing atmospheric conditions", *IEE Proceedings of Generation, Transmission and Distribution*, vol. 142, no. 1, Jan. 1995, pp. 59 –64.

[17] A. Brambilla, et al., "New approach to photovoltaic arrays maximum power point tracking", in *IEEE Power Electronics Specialists Conference*, 1999, pp. 632–637.

[18] C. W. Deisch, "Simple switching control method changes power converter into a current source", in *IEEE Power Electronics Specialists Conference* 1978, pp. 300-306.

[19] K. Siri and K.A. Conner, "Parallel-connected converters with maximum power tracking," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2002, vol. 1, Mar. 2002, pp. 419 –425.

[20] K. Siri, "Study of system instability in solar-array-based power systems", *IEEE Transactions on Aerospace and Electronic Systems*, vol. 36, no. 3, July 2000, pp. 957-964.

[21] D. Detjen, S. Schroder and R.W. De Doncker, "Embedding DSP control algorithms in PSpice," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 294 –300, Jan. 2003.

[22] J. T. Tou. *Digital and sampled-data control systems*. New York, McGraw-Hill, 1959.

[23] H. Jin, "Behavior-mode simulation of power electronic circuits," *IEEE Transactions on Power Electronics*, vol.12, no. 3, pp. 443 –452, May 1997.

[24] A. Prodic and D. Maksimovic, "Mixed-signal simulation of digitally controlled switching converters," in *IEEE Workshop on Computers in Power Electronics*, 2002, pp.100-105.

[25] P. G. Jespers. *Integrated converters: D to A and A to D architectures, analysis and simulation*. New York: Oxford University Press, 2001.

[26] *Power System Blockset*. MathWorks, Natick, MA, 2001.

[27] *SPRS145I TMS320LF240xA DSP Controllers datasheet*. Texas Instruments, Houston, TX, 2003.

[28] *SPRU357B TMS320LF/LC240xA DSP Controllers Reference Guide- System and Peripherals*. Texas Instruments, Houston, TX, 2001.

[29] *TMS320LF2407A Evaluation Module Technical Reference*. Spectrum Digital, Stafford, TX, 2003.

[30] *Writing S*-function. MathWorks, Natick, MA, 2001.

[31] W. Wu et al., "DSP-Based Multiple Peak Power Tracking for Expandable Power System," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Feb. 2003.vol. 1, pp. 525 –530.