# SURFACE CHARACTERIZATION OF THIN FILM ZnO CAPACITORS BY CAPACITANCE-VOLTAGE MEASUREMENTS

by

LINDA BONITA SMITH
B.S. Florida A & M University, 1999

A thesis submitted in partial fulfillment of the requirements
for the degree of Master of Science
in the Department of Physics
in the College of Sciences
at the University of Central Florida
Orlando, Florida

Spring Term
2007

Major Professor: Enrique del Barco

# ABSTRACT

The main objective of the research was the fabrication and characterization of MOS/MIS capacitors with ZnO as the insulating layer. Comparison with the already well known behavior of MOS/MIS capacitors with $SiO_2$ as insulator was used to facilitate determination of the ZnO characteristics. Moreover, thermal annealing of the samples led to increased understanding of the role of defects on the dielectric properties of the ZnO layers in the MOS/MIS devices. Hall-effect transport measurements and x-ray diffraction (XRD) spectroscopy are used to analyze the structure and electronic surface characteristics of the ZnO insulator. Capacitance-voltage (C-V) measurements are used to understand the effect of surface interface charges and fixed oxide charges in the MOS/MIS (metal-oxide (insulator)-semiconductor) capacitor. The results of the Hall-effect measurement will reveal several things; the sheet resistance, carrier concentration, and mobility as well as confirm the type of silicon used. The optical spectrophotometry measurement confirmed the band gap of 3.2 eV for ZnO. The x-ray diffraction data confirmed a (002) orientation polycrystalline wurtzite ZnO structure. Initial capacitance-voltage measurement of $SiO_2$ and ZnO revealed that the capacitance was larger for $SiO_2$ than for ZnO.

This study also explores the impact of thermal annealing on the performance of the ZnO capacitors. Hall-effect measurements are used to evaluate the influence of thermal annealing on the resistivity, carrier concentration and mobility as a function of annealing temperature. ZnO is an n-type semiconductor; this n-type conductivity is due to deviations from the stoichiometry as a result of oxygen vacancies and interstitial zinc. After ZnO samples were annealed at different temperatures, the Hall-effect measurements were performed. After thermal annealing, the mobility increased significantly by two orders of magnitude, but both the carrier concentration and the sheet

density decreased. A threshold voltage (turn-on) of –1V was observed for the ZnO sample annealed at 980°C.

ZnO is very versatile material with the potential for use in field effect transistors, solar cells, sensors, surface acoustic wave devices and photodiodes due to the high conductivity and high transmittance in the visible part of the spectrum.

ZnO as an insulator works through analytical solutions, but not necessarily through this investigation. The difference in oxide thickness during rf magentron sputtering change the capacitance for ZnO making it lower. For n-type substrates it appears that the capacitance after annealing was higher than the capacitance before annealing. After annealing, a stretched out capacitance-voltage curve indicates the presence of trapped oxide charges and an unsmoothed surface. A high resistivity material could be used for some devices. However, typically low resistivity materials are used.

After ZnO samples were annealed (unetched) at different temperatures, the Hall-effect were performed and the mobility increased significantly by two orders of magnitude, but the sheet density decreased along with the carrier concentration. The only sample that appears to come to a high frequency C-V in equilibrium is the ZnO sample annealed at 980°C. The depletion region was distinguishable and the transition point (threshold voltage) was found to be at -1 V.

# ACKNOWLEDGMENTS

First, I wanted to thank my God and Savior Jesus Christ who not only allowed me to be here at this time and place, but God kept the dream in my heart alive even though I tried to smother it out with mediocrity. I decided to take my road less traveled because living without knowing what my fullest potential could be is like not living at all. This part of my journey is over, now onto the next.

I wanted to thank my mother Lillian Smith, my beloved Grace, and my other family and friends who have cheered me on, encouraged me to keep my eyes looking straight ahead, and to remember the promises of God. There were many times when I had to stay put because of my work and I am grateful for their understanding and their continued love and support.

I also wanted to thank my graduate thesis committee members: Dr. Enrique del Barco, Dr. Robert Peale and Dr. Helge Heinrich for their patience and help with getting to the end of this part of my journey.

I want to thank my mentors: Dr. Jacqueline Smith, Dean Melvin Rogers, Dr. Pamela McCauley-Bell and Mrs. Jacqueline West-Lee for their mentoring of my heart and soul through so many transitions in my life since coming to graduate school.

I also want to thank the Physics Department office staff, who kept me laughing when I did not want to and helped to get the information I needed to do my job and research.

# TABLE OF CONTENTS

# LIST OF FIGURES

# LIST OF TABLES

# CHAPTER ONE: INTRODUCTION

A lot of work has been done to modify the performance of MOSFET (metal-oxide-semiconductor-field-effect-transistor) devices. One of the ways to do that is to improve the properties of MOS/MIS capacitors through new dielectrics or new semiconductors. According to Schroder [8], the deep-depletion MOS/MIS capacitor can be found as the unit cell of CCDs (coupled-charged devices) and DRAM (dynamic random access memory). A deep-depletion MOS capacitor can also be found between the source and drain of FET (field effect transistors) [6]. The standard MOS capacitor uses silicon dioxide as the dielectric, therefore the theoretical conditions will be based on that and the experimental results will show the deviations that are caused by changing the dielectric to ZnO. In order to use ZnO as an insulator, the quality of this oxide must be characterized. Capacitors will be fabricated to specifically study the use of ZnO as an insulator. The MOS/MIS is the only device that should stay in equilibrium when a voltage is applied; that is what separates the MOS capacitor from FETs, current will flow when a voltage is applied to a FET. This report will cover the theoretical ideal and non-ideal conditions that will apply to MOS/MIS capacitors [6]. It will also cover how capacitance-voltage measurements (C-V) will help to study the traps and charges in ZnO as-deposited and after thermal annealing. The Hall effect and XRD is used to support the evidence for the conclusion reached in this investigation.

## MOS/MIS Capacitors

The MOS/MIS capacitor is a simple structure with a simple fabrication set-up and it is relatively simple to analyze. The MOS/MIS capacitor is a great tool to study the electrical properties

of the MOS/MIS system. Analysis can be done on the silicon, silicon dioxide and the interface between the Si-$SiO_2$. There are several advantages in using an MOS/MIS capacitor to measure the properties of a MOS/MIS system such as finding the doping profile within the silicon, surface band bending and the depletion layer width in the Si as a function of the gate voltage, the avalanche breakdown voltage, oxide thickness, conductivity type of the silicon and properties of the electron and hole traps in the $SiO_2$. Other important properties are fixed oxide charges and interfacial trap level densities that will be addressed in the model of the non-ideal MOS/MIS capacitor. The MOS/MIS capacitor is essentially a parallel plate capacitor: one electrode is the metal contact located on the top of the oxide/insulator called the gate and the second electrode is the silicon on the bottom. These electrodes are separated by the insulating layer. Usually the insulating material is thin and predominately $SiO_2$. [3]

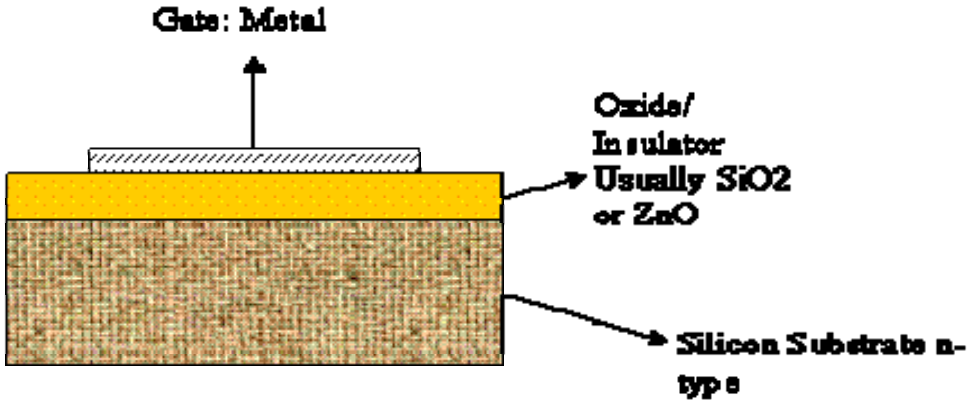


Figure 1: An example of a MOS/MIS capacitor.

The goal in studying the MOS/MIS capacitor is to improve the performance and the stability of devices such as MOSFET in integrated circuits. When there are any changes in processing that could improve the electrical properties of the actual device it can first be demonstrated in the MOS/MIS capacitor. There has been a significant research effort into using different types of insulators/oxide in MOSFET; the MOS/MIS transistor is essentially a MOS/MIS capacitor with two p-n junctions placed adjacent to the region of the semiconductor controlled by the MOS gate [5]. The basic operation of the FET is this: carriers enter the structure through a source and leaves through a drain; the silicon substrate that is used determines whether the source and drain is a heavily doped n+ or p+ junction. These carriers are subjected to the control of the gate (metal or polysilicon). For example, when the gate voltage is in accumulation or depletion bias (this will be discussed in greater detail later), the area between the source and drain will contain either an excess or deficit of holes and very few electrons thus creating an open circuit. When the gate voltage is in inversion (this will be discussed in greater detail later), an inversion layer containing mobile electrons is created next to the silicon surface, thus creating an open channel between the source and drain. When the inversion bias continues to increase, the increasing number of electrons piling up at the silicon surface will result in greater conductance in the inversion layer [5]. This area between the source and drain is a MOS/MIS capacitor.

## Parallel Plate Capacitors

Semiconductors are the materials that move between conductors and insulators. When a parallel plate capacitor (figure 2) is connected to a power source (usually a battery) these plates become charged and an electric field is generated between them. The direction of the electric field coincides with the direction that a positive charge would move. The electric field should be

uniform along the length of the capacitors. The electric field can easily be calculated using the following equation:

$$E = \frac{V}{d} \qquad \text{Equation (1)}$$

where $d$ is the distance between the parallel plate capacitors and $V$ is the applied potential (voltage). The charges along the plate would experience the same forces.

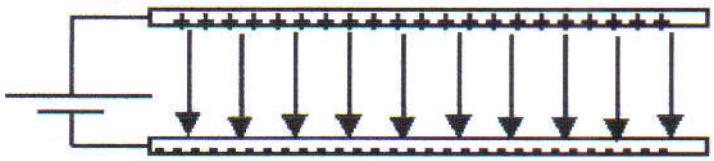

Figure 2: Basic parallel plate capacitor [16].

The whole purpose of the capacitor is to store energy, and when the capacitance is measured it is related to the amount of charge that can be stored on the parallel plates as a function of the applied voltage. For example, if the capacitance increases the amount of charges that can be stored also increases with the same applied potential. If a plot of the Q-V was done, the slope of the graph would represent the capacitance (see figure 3) and the area under the curve is the amount of energy stored in the electric field between the plates.

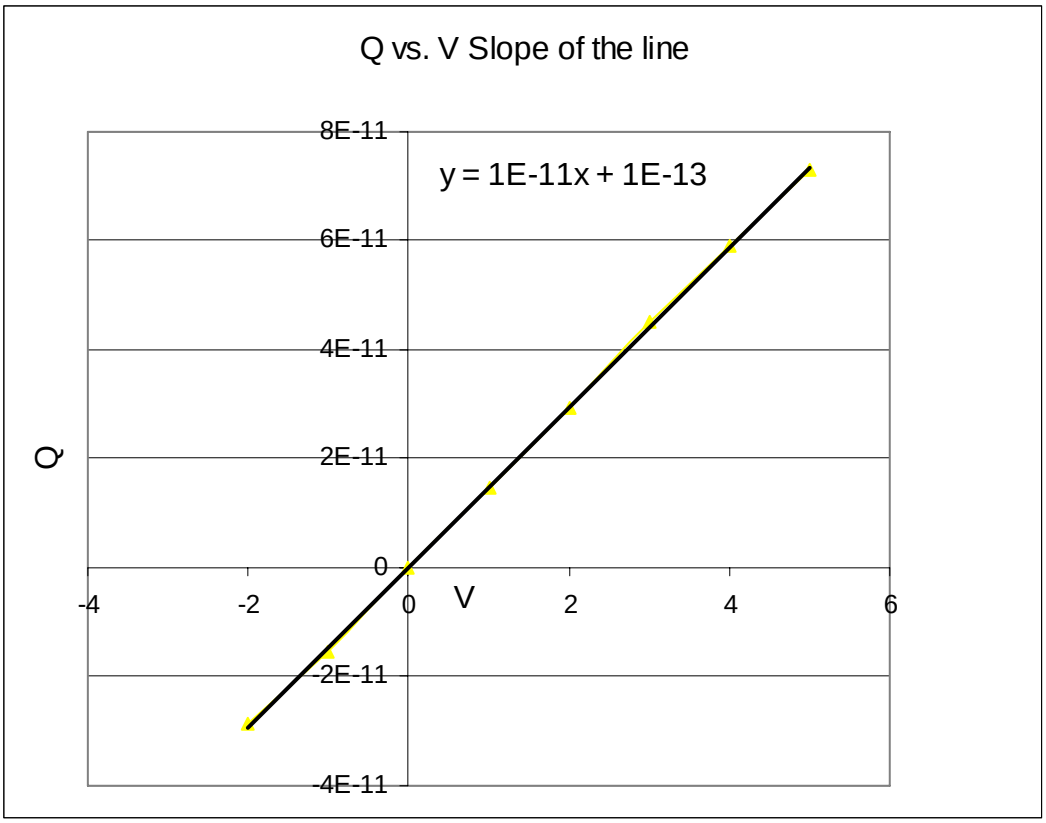


Figure 3: This is a Q vs V graph that was taken from a ZnO sample was UV radiated for over 10 minutes and a C-V measurement was performed on the sample. The slope of the curve represents the capacitance

$$C = \frac{q}{V} \qquad \text{Equation (2)}$$

The charge is $q = EA\varepsilon_o$ and the potential between the parallel plate capacitor is given by $V = Ed$. When you put both together with equation 2, we obtain the dependence of the capacitance on geometry.

$$C = \frac{q}{V} = \frac{A\varepsilon_o}{d} \qquad \text{Equation (3)}$$

where $A$ is the area of the gate and $\varepsilon_o$ is the permittivity of free space. What are these charges? Charges that flow through a conductor are electrons. When an electric circuit is connected, charges will flow through the circuit. When these electrons are flowing through the circuit they are driven by the electric field that the power source sets up in the connecting wire.

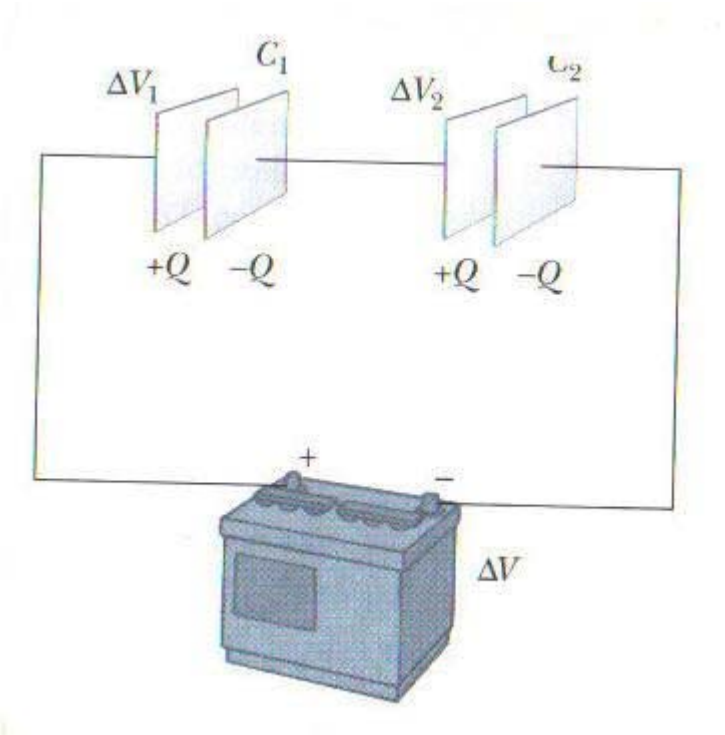


Figure 4: Circuit diagram of parallel plate capacitors in series, taken from [9].

As the charge accumulates on the capacitor plates, larger amounts of work must be done to transfer additional charge. The definition of work that will be used here is the electric potential energy "U" due to the electric field between the plates. Energy can be recovered to do work by discharging the capacitors:

$$U = \frac{q^2}{2C} = \frac{CV^2}{2} = W$$ Equation (4)

[9]. The above describes the case where there is no dielectric between the plates except air. The focus now is the addition of a dielectric between the plates which is what this research will investigate.

Theoretical: ideal and non-ideal MOS/MIS

When a dielectric is added between the two plates it has the effect of reducing the electric field and eliminating the possibility of charges sparking between the plates. However, there should be no effect on the potential. The difference between the capacitance with and without a dielectric is given by:

$$C = kC_{air}$$ Equation (5)

$C_{air}$ is the capacitance w/air between the plates and $k$ is the dielectric constant that will be different because it is related to $\varepsilon = \varepsilon_o k$. The material between the plates will be an insulator/oxide. Insulators require a lot of energy to free electrons so that they can move through the material. Therefore, it is safe to assume that electrons are not moving through the insulators and no current is generated even though an electric field is applied. One difference between a semiconductor and an insulator is that: it does not take a lot of energy to remove an electron ($e^-$). In semiconductors, e- finds it easier to move due to two things, 1) doping of the semiconductor and 2) the generation of

positive ions that are very loosely held within the material. Also with doping, the density of carriers can be controlled (i.e. current control). These carriers participate in the generation of current and the electrical properties of the material can also be controlled.

One of the most important aspects of semiconductor structures is the surface effects which often dominate the characterization of devices [1]. The ideal MOS/MIS structure will be studied and then the deviation from that will be elaborated on. The focus will be on using n-type silicon but the same principle can be applied to p-type silicon.

In MOS/MIS capacitors, the insulating material does not allow dc current to flow across the "space-charge region". The space-charge region for MOS/MIS capacitors can be found in thermal equilibrium which produces a constant Fermi level in the space-charge region and $np=n^2$. In Figure 5 below, an energy band diagram is shown for n-type and p-type semiconductors under zero bias.

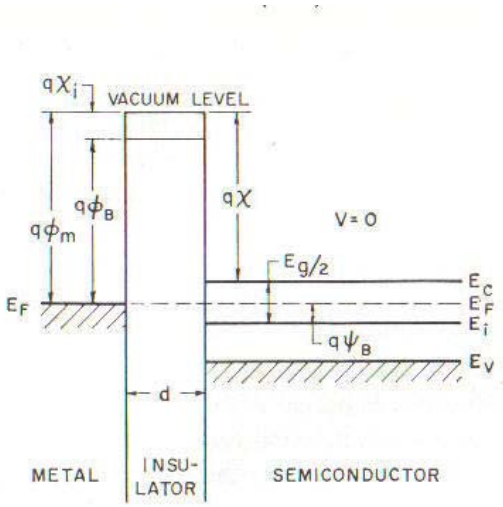


Figure 5: Energy band diagram under zero voltage for an n-type substrate. Picture was taken from Sze, *Physics of Semiconductor Devices*, p. 427.

The purpose of Figure 5 is to explain (limited detail) the initial set-up of the band bending diagram used in Figure 6. According to Wolf [13], the vertical axis represents the energy carried by electrons when they occupy energy levels at a certain location in the device. $E_c$ and $E_v$ represent the conduction band and the valence band edges. The $E_i$ is the middle of the band gap, corresponding to the Fermi energy level of an intrinsic (undoped) semiconductor. $\frac{E_g}{2}$ is the difference between the conduction and valence band energy ~ $E_c - E_i$, $q\phi_m$ is the metal work function which is the energy difference between vacuum level and the Fermi energy in the metal, $q\phi_B$ represents the semiconductor (bulk) work function, the $q\psi_B$ is the surface potential in the semiconductor and it lies between the constant Fermi level and the intrinsic energy level. The vacuum level is the minimum energy an electron must possess to completely escape from the material, and the $q\chi_i$ and $q\chi$ are the electron affinity for the insulator and semiconductor respectively which is the surface barrier and it remains fixed in zero gate voltage. For example, since I am using an n-type semiconductor, the Fermi level is closer to the conduction band than it is to the valence band (conduction band should contain electrons that jump from the valence band and leaves behind holes). If the semiconductor is in equilibrium, the Fermi level does not change its position in the material (straight, horizontal line). When you look at figure 5 in regards to an ideal MOS/MIS capacitor, the energy difference between the metal work function $(q\phi_m)$ and the semiconductor work function $(q\phi_B)$ is zero. The energy band diagram in figure 5 is called a flat-band diagram because at zero gate voltage the conduction band, valence band and intrinsic energy band are flat. Another aspect to consider is when there is a dc bias applied, the current is zero because it should be a perfect insulator; the silicon stays in equilibrium, implying that the Fermi energy level stays flat, but the other energy bands start to change at this point. Figure 6 and the explanation that describes this

change in energy bands are below. You will see that no matter what the bias voltage is the Fermi level stays at equilibrium.

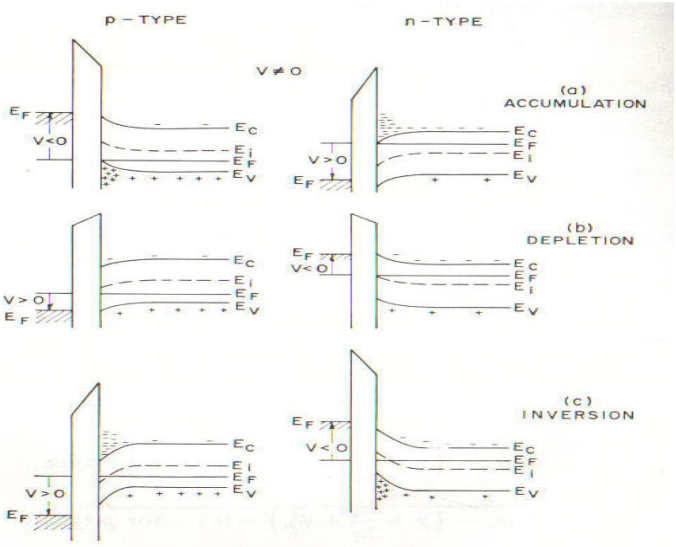


Figure 6: Band bending of a MOS/MIS structure under different bias. Picture is taken from Sze, *Physics of Semiconductor Devices*, p. 428

For an n-type substrate: when a large positive voltage is applied to a metal gate, a large potential will attract a negative charge in the semiconductor which consist of *accumulated* electrons near the oxide-semiconductor interface. The negative charge creates a mirror positive charge. As the voltage is slowly decreased the carriers become depleted at the oxide-semiconductor interface. This *depletion* will leave behind ionized particles (holes), the electrons are pushing away from the interface; these ionized charges are uncompensated donor ions [1]. This depleted region will continue to grow under negative voltage until it reaches a maximum at which *inversion* takes over. The maximum also corresponds to the conduction band bending close to the Fermi level. When there is an abrupt increase of electrons at the oxide-semiconductor interface, these additional charges create the inversion. The depletion region width can be calculated according to

$$W_{\max} = \sqrt{\frac{2K_s \varepsilon_o \phi_s (inv)}{qN_D}} \qquad \text{Equation (6)}$$

where $\varphi_s$(inv) is the surface potential (it is the total bending of the energy bands from the bulk of the semiconductor to the surface) ,$N_D$ is carrier concentration, and $K_s$ is dielectric constant for silicon. $W_{max}$ is a function of the impurity concentration [1]. An important quantity that will be calculated is the charge per unit area contained within the surface depleted region at and after strong inversion[1].

$$Q_{depletion} \equiv qN_D W_{\max} \qquad \text{Equation (7)}$$

This quantity is positive for n-type semiconductors and negative for p-type. Let us go more in-depth about the three regions that occur as a result of the different applied voltages (accumulation, depletion and inversion for n-type).

**Accumulation**

When a positive gate voltage is applied to a MOS/MIS capacitor, it generates an ac sinusoidal signal. During accumulation, where the capacitance is at a maximum, this positive voltage is characterized by majority carriers (electrons) being moved to the surface at the oxide-semiconductor interface. It is all right to assume that in accumulation, the MOS capacitor can follow the applied ac signal quasi-statically. The ac signal is adding or subtracting a small change in charge on both sides of the oxide (see figure 7), it is one reason why at accumulation the device takes on the characteristics of a resistor in series with the oxide capacitance [1]. Since there is an increase in electron concentration near the surface, this surface could form the second electrode of a parallel plate capacitor. Another aspect of the accumulation region is that, the Fermi level moves

closer to the valence band and remains constant. The capacitance in accumulation is the capacitance of the insulator/oxide and is given by:

$$C_{ox} = \frac{K_{ox} A_g \varepsilon_o}{d_{ox}} \qquad \text{Equation (8)}$$

$A_g$ is the area of the metal gate, $\varepsilon_o$ is the permittivity of free space and $K_{ox}$ is the dielectric constant of the oxide see figure 8 at point **a**. [7] The positive gate voltage lowers the Fermi level energy in the metal relative to the bulk Fermi level and this variation causes a positive slope of the energy band.[7]

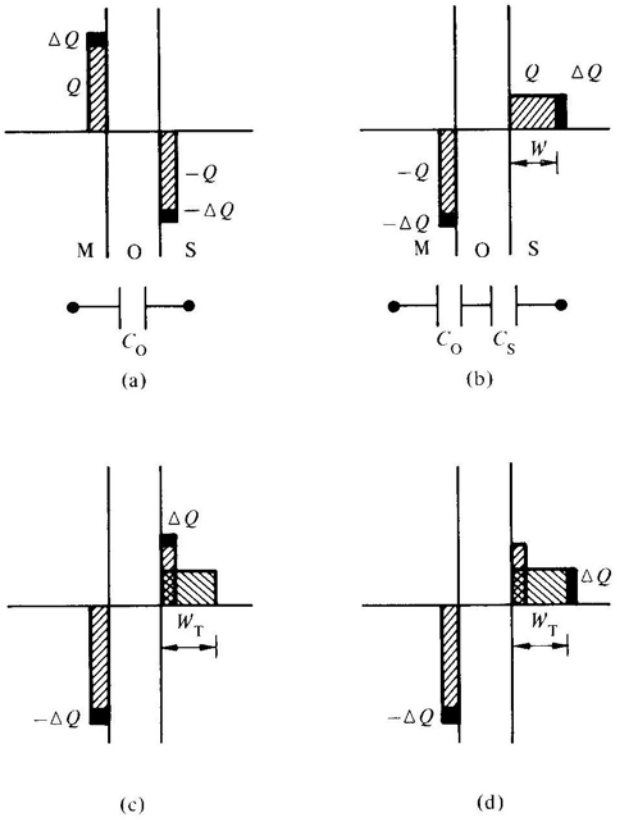


Figure 7: This is a block diagram that shows the affect of ac charge fluctuations inside an MOS capacitor during different dc biasing- (a)accumulation, (b) depletion (c) inversion at low frequency and (d) inversion at high frequency.

## Depletion

As the voltage starts to become less positive (more negative), there is a change in the charge on the gate and a charge in this depleted region. There is a negative gate charge and a positive charge in the depletion layer in the semiconductor. The concentration of electrons begins to decrease at the oxide-semiconductor interface (figure 6b) leaving behind ionized donors (holes). This removal of electrons from the interface causes a channel to open up under the oxide known as the depletion layer width. When the ac signal places that less positive to negative voltage on the gate, the depletion layer width continues to widen until it reaches a maximum length.

When the depletion region increases, the capacitance in depletion decreases because the capacitance of the oxide is in series with the semiconductor capacitance essentially forming two parallel plate capacitors see figure 8 at point **b**. [7] The Fermi level in the metal rises relative to the Fermi level in the semiconductor therefore causing a negative slope of the energy band in the insulator and semiconductor.

## Inversion

When inversion sets in under continued negative gate voltage, one of two things can happen at this point: High frequency (HF) (equilibrium state, constant capacitance) or deep-depletion (non-equilibrium condition). In inversion, a significant amount of positively charged ions pile-up at the oxide-semiconductor interface and the depletion layer width has reached a maximum width. Since, I am measuring only at high frequency, the sluggish generation-recombination process will not be able to give or eliminate holes (minority carriers) in response to the ac signal [6]. The bands bend up more, and the hole concentration will exceed the electron concentration at high frequency

(corresponds to strong inversion) For HF, the capacitance in inversion is similar to two parallel plate capacitors in series given by:

$$C_{inv} = \frac{C_{ox}C_{semi}}{C_{ox} + C_{semi}} \qquad \text{Equation (9)}$$

or

$$C_{inv} = \frac{C_{ox}}{1 + \frac{W_{max}}{d_{ox}^{'}}} \qquad \text{Equation (10)}$$

where $d_{ox}^{'} = \frac{K_{semi}d_{ox}}{K_{ox}}$. Also, the capacitance in inversion corresponds to the minimum depletion capacitance and this value should be constant because the capacitance at this point becomes a function of frequency. Pictured below is a C-V plot showing inversion starting past point b.

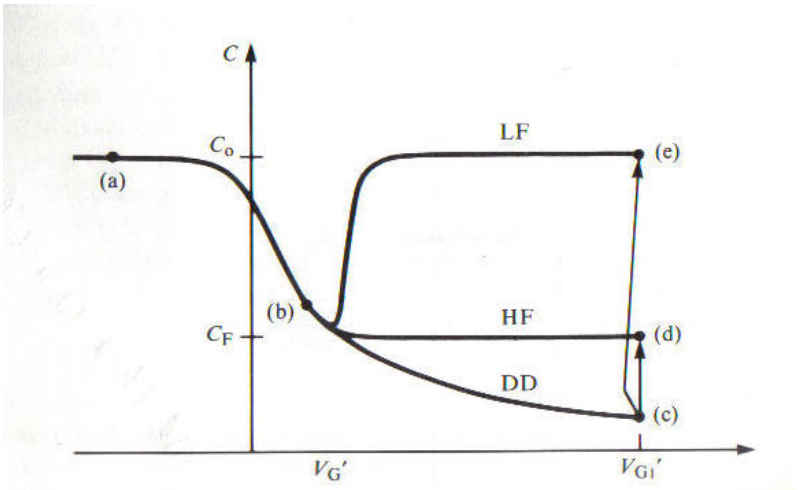


Figure 8: Capacitance-Voltage curve of a p-type substrate taken from Schroder 1987. It shows how at different frequencies this curve can be generated. This investigation targets the high frequency/DD curve because this generated at 1 MHz.

In the non-equilibrium state or deep depletion (DD), both the gate and semiconductor charges are significantly negative. The inversion layer should shield the bulk of the semiconductor from gate voltage changes. When the gate voltage is swept towards more negative values in inversion, it will cause the capacitance to be below its equilibrium value. This happens because the inversion layer charge is not generated rapidly enough to follow the sweep rate. More holes are injected into the bulk from the inversion layer. Eventually, the MOS/MIS capacitor will return to equilibrium through electron-hole pair generation [7]. One of the reasons why the inversion layer deviates from the idea is if the device has a slow generation rate or a long generation lifetime the inversion curve will not form because the bias sweep rate has to be extremely slow [7]. According to Schroder, the current always flows in a deep-depletion MOS/MIS capacitor. Another characteristic of the deep-depletion region is that the Fermi level is actually splitting into two quasi-Fermi levels because this is a non-equilibrium condition where the majority and minority carriers are no longer well defined. Schroder makes several assumptions about these quasi-Fermi levels [7] such as the majority carrier quasi-Fermi level remaining constant through out the semiconductor at its bulk value. Also, the minority carrier quasi-Fermi level remains constant in the near surface regions, but the location of the minority carrier quasi-Fermi level in the band gap is still unknown. Since, the MOS/MIS capacitor in this research is in deep-depletion mode based on the results for $SiO_2$ and ZnO C-V curves, the following deep-depletion solution can be applied [6]; the majority-carrier accumulation charges and the minority-carrier inversion charges are located in a shallow region (on the order of several hundred angstroms) in the semiconductor at the oxide-semiconductor interface. Figure 5 above shows the point at which inversion is in deep depletion. In my calculations, I used both the delta-depletion solution and the qualitative solution to find the capacitance at the main points on the C-V curve; these equations can be found in the appendix.

Table 1: Comparison of different capacitances

| **C-V Curve** | **Capacitance** |
|---|---|
| C (accumulation) | $C = C_{ox}$, maximum capacitance |
| C (depletion) | $C = \frac{C_{ox}}{1 + \frac{W}{d'_{ox}}}$ |
| C (inversion) | $C = \frac{C_{ox}}{1 + \frac{W_{max}}{d'_{ox}}}$, minimum capacitance |

Ideal MOS/MIS Structure

When there is not a contact potential or work-function present between the metal and semiconductor any applied voltage will appear across the oxide and silicon [1] given by the following equation:

$$V_g = V_o + \varphi_s \qquad \text{Equation (11)}$$

where $V_o$ is the potential across the oxide and the $\varphi_s$ is the potential across the silicon. When there are no charges at the interface between the oxide and semiconductor, Gauss' law requires that the electric displacement should be continuous at the interface: The electric field is uniform when there are no charges within the oxide. The electric field is given by:

$$E_o = \frac{V_o}{d_{ox}} \qquad \text{Equation (12)}$$

where the $d_{ox}$ is the oxide thickness. The electric field at the silicon surface is denoted by:

$$E_{semi} = -\frac{Q_s}{K_s \varepsilon_o}$$ Equation (13)

Once these equations are combined, they give an expression to calculate the voltage drop across the oxide and the $K_s$ is the dielectric of the semiconductor and the $Q_s$ is the charge in the semiconductor [1]:

$$V_o = -\frac{d_{ox}}{K_{ox} \varepsilon_o} Q_s = -\frac{Q_s}{C_{ox}}$$ Equation (14)

Now according to Pierret the ideal MOS/MIS should have some explicit properties:

- Metallic gate is sufficiently thick so that it can be considered an equipotential region under ac or dc biasing.
- The oxide is a perfect insulator with zero current flowing through the oxide layer under "all" static biasing.
- No charge centers are located in the oxide or at the oxide-semiconductor interface.
- Semiconductor is uniformly doped.
- Semiconductor is thick enough so that a field-free region (silicon bulk) is encountered before reaching the back contact.
- Ohmic contact is firmly established between the semiconductor and metal on the back side of the device.
- MOS/MIS capacitance is a 1-D structure with all variables taken as a function only of the x-axis.

## Non-Ideal MOS/MIS Capacitors

There are several factors which will affect the ideal characteristics of an MOS/MIS structures. A few of them will be discussed here as it applies to $SiO_2$ and ZnO as the insulator:

- Surface states or interface states: Theses are energy levels that can exist within the forbidden band gap at the oxide-semiconductor interface. These states can also exchange charges with the semiconductor during a short period of time [10].
- Fixed surface charges are located near or at the semiconductor surface and will be immobile under an applied electric field.
- Mobile ionic charges.
- Oxide trapped charges.

There are charges that will become trapped in the oxide during the operation of the MOS/MIS device even if it is not present during fabrication. Electrons and holes can be introduced in the oxide from the semiconductor or the gate. There is also the possibility that energetic radiation can produce e-h pairs in the oxide and therefore, these electrons and/or holes are trapped in the oxide. These trapped charges will often been seen in the shift of the flatband voltage (this is where the gate voltage is zero on the C-V curve). These charges are known as oxide trapped charges. Mobile charges in the oxide are the result of ionic impurities such as $Na^+$ which is the most dominate contaminant (figure 9). Sodium contamination is a problem even in the industrial setting. Sodium was documented to affect the stability of the gate bias, because it will drift through the $SiO_2$. It has been hypothesized that the motion of sodium in thermal $SiO_2$ is governed by the emission of ions from traps that already exist at the interface and by subsequent drift through the oxide. Sodium has a high drift velocity through $SiO_2$. Can the same be said of ZnO?

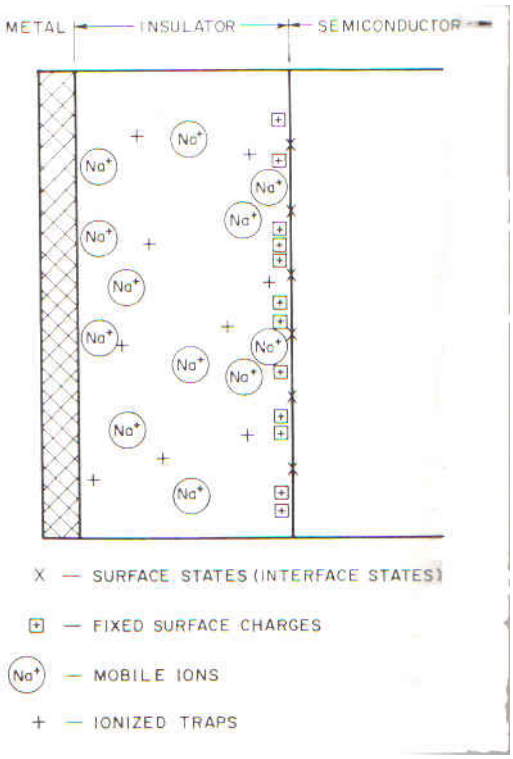


Figure 9: This figure shows the locations of the surface states and trapped charges that could be in the oxide and at the oxide-semiconductor interface.

C-V measurement has been determined to be the best way to determine the mobile charges. When characterizing fixed charges, the flatband voltage shift is used [9]. An experimental C-V curve is compared to a theoretical C-V curve by calculating the flatband capacitance. There are several parameters needed to find the fixed charge; the work-metal difference which is no longer zero as it is for the ideal MOS/MIS capacitor, flatband voltage and the oxide capacitance and in order to eliminate the effect of other oxide charges and to reduce the interface charges annealing is used.

## ZnO

Over the last decade, a lot of work has been done to fabricate, analyze and further develop the use of ZnO in industrial applications such as optical fibers, opto-electronic devices, solar cells, gas sensors and other devices. ZnO is an n-type transparent oxide with a wide and direct band gap which is transparent in the visible range of the spectra making it less sensitive to light [2]. Also, if the dielectric constant is higher it can lead to lower operating voltages with a constant insulator thickness therefore reducing gate leakage current without affecting the capacitance. ZnO with a dielectric constant of 8.66 should be a viable answer to this concern. It may even be possible to develop transparent thin film transistors based upon ZnO; these transistors could find applications in transparent and opaque displays; high electron mobility and visible transparency makes ZnO transparent field transistors another alternative to using amorphous silicon transparent field transistors for use in flat panel displays. Fortunato et al. [2] suggested that such devices could have faster operating speeds and higher drive currents due to the electron channel mobility. A future hope for ZnO is in the application of manufacturing cheaper LEDs (light emitting diodes) and piezoelectrical (materials ability to generate a voltage in response mechanical stress). ZnO can function in two roles: 1) as a semiconductor, and b) as a dielectric. In this work, I am exploring the use of ZnO as a dielectric. One method commonly employed to characterize the insulating layer in semiconductor devices is C-V. This technique provides valuable information about defects and charges in the oxide.

Table 2: Well known specifications of ZnO

| | |
|---|---|
| Theoretical Band Gap | 3.2-3.3 eV |
| Exciton Binding Energy | 60 MeV |
| Atomic Weight | 81.389 |
| Theoretical Electric Resistivity | 6.16 μΩ-cm |
| Bulk Resisitivity | 7.14 Ohm-cm |
| Density | 5.606 g/cm$^3$ |
| Crystal Structure | wurtzite |

The main objectives of my research consist of the fabrication and characterization of MOS/MIS capacitors based on ZnO as the insulating layer. The comparison with the already well known behavior of $SiO_2$ MOS/MIS capacitors will allow for the determination of ZnO characteristics. Moreover, thermal annealing of the samples will lead to an understanding of the role of defects in the oxide layers of MOS/MIS devices such as the Field Effect Transistors. This project will investigate whether deep depletion is a true common occurrence in C-V measurements of $SiO_2$ and ZnO whether they are annealed or not. I also found a standard capacitor value based on an actual two lead capacitor (~11.206 pF).

# CHAPTER TWO: EXPERIMENTAL METHODS

## Fabrication Process

### Cleaning

I used n-type silicon wafer with (100) orientation cut into reasonable size pieces, they were cleaned using the following steps.

- Start with cleaning the sample with a soapy detergent, then rinsed with DI water.
- The samples are then rinsed with Acetone, Methanol and then rinsed with DI water. Between each rinsing step, DI water is used to stop the last step and it was dried.
- Tweezers are used to hold the samples and a basic laboratory cotton swab tips were used to clean with the soapy detergent.
- Each sample is inspected for spots and other contaminants; if any were found the process was repeated until there were no seeable surface contaminants. This process was done before the samples are used in the RF Magnetron Sputtering were the ZnO was deposited onto the samples.
- Thick rubber gloves, goggles and a lab coat is used to handle all the samples under the chemical hood to prevent chemical exposure especially since for the etching, HCl and HF are used.

### RF Magnetron Sputtering

The n-type silicon pieces and a piece of a glass slide is mounted on the sample holder and inserted into the low-pressure chamber between two electrodes. These electrodes are driven by an RF power source that generates plasma and ionizes the Argon gas between the electrodes. A DC

potential is used to drive the ions towards the surface of the target causing atoms to be pushed off the target and these atoms condense onto the sample surface. The plasma is contained at the surface of the target by a strong magnetic field. RF Magnetron Sputtering has been documented as being a better method of deposition because it creates better adhesion and greater uniformity over large surfaces. The ZnO was deposited onto the silicon sample at room temperature [9]. The sputtering is driven by momentum exchange between the ions and atoms in the material, due to collisions. This process is similar to atomic billiards; the ion striking a large cluster of close-packed atoms. The initial collision will push the atoms already in the lattice deeper into the cluster (distorts the lattice structure), the collisions between the atoms at the surface will eventually cause atoms to be ejected. One of the important advantages to using sputter deposition is the fact that the deposited film will contain the same composition as the source material in our case ZnO or ZnS [9].

Table 3: Operation parameters for the magnetron sputter being used for a normal run.

| | |
|---|---|
| Main Dial (Voltage Divider) | 6 (or less for just ZnO) |
| Deposition Time | 45 minutes |
| Forward Power | 200 W |
| Maximum Power | 220 W |
| Chamber Pressure | 1.4 to 7.2 mTorr |
| Deposition Pressure | 13 mTorr |
| Room Temperature | 18°C – 21°C |

## Contact Sputtering/Etching

After the pieces were sputtered with ZnO, the samples were mounted in Denton desktop sputtering system to sputter the metal contacts; gold and palladium. The samples are fitted with a metal mask. This mask is very simple with holes drilled through it and each hole represents a capacitor. Regular masking tape is used to attach the sample to the mask; the sample is placed inside

the desktop sputtering system and sputtered in Argon gas. In order to make sure there is uniform contact sputtering, the sample was rotated 90° after the initial sputtering. The (ZnO) samples need to be etched along the sides with HCl & DI water before C-V measurements can be performed. Since the oxide thickness is thin (1000Å), there is a concern about current tunneling from the top of the capacitor (metal) to the bottom of the silicon wafer. HCl can etch ZnO so it is important to be very careful. This etching step can be done before sputtering the contacts or after. In order to reduce corrosion of the sample contacts by HCl it may be better to etch before sputtering the contacts.

Table 4: Specification of the Desktop Sputtering system being used

| | |
|---|---|
| Current | 20 mA |
| Sputtering Time | 300 seconds |
| 90° rotation Sputtering Time | 300 seconds |
| Pressure | 200 mTorr |
| Gas | Argon |

## Experimental Test

### Capacitance-Voltage

The analysis of semiconductor capacitance characteristics is measured on an HP 4280A 1MHz C-V Plotter and the maximum voltage range that is used is ± 42V. The plotter is attached to a Signatone probe station via coaxial cables. This is designed to measure high frequency C-V, but with a change in the test signal a low frequency curve change be achieved. The table below will show the parameters that must be set-up for taking measurements. The parameters used are based on continued study on the quality of each C-V on different samples. First, the C-V plotter must be warmed up for 30 minutes or more with the coaxial cables detached from the probe station. After

the 30 minutes the cables were attached and zeroed again. The probe station has a usual set-up; (since the backside of the sample is just silicon) I attached a piece of aluminum foil on a glass slide and placed the glass slide on the probe station. Probe #4 which is the low potential on the aluminum foil and I placed probe #1 the high potential directly on the contact. I recorded an initial reading with ambient light and no voltage. I closed the probe box to eliminate ambient light and waited a few seconds before starting the test to see if the capacitance stabilized.

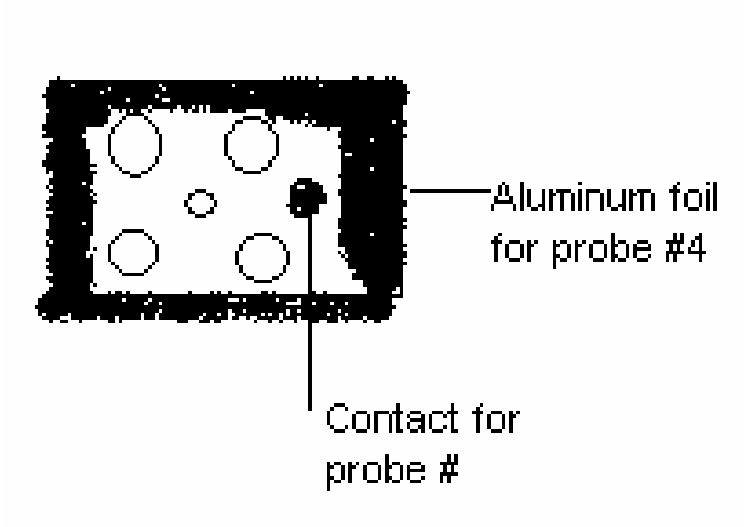


Figure 10: This is general picture of where the probe points go on the sample and aluminum slide.

Several characteristics can be calculated from the C-V such as threshold voltage, impurity concentration of the substrate, flat band voltage and the surface charge density. Since, there is not a X-Y Recorder to do actual real time plotting, one of the parameters that can be changed on the C-V plotter is the hold time as well as the step delay time. Slowing down the hold and step delay times to seconds instead of milliseconds will slow down the signal output and it allows the operator to actually record the capacitance by hand. Also, the larger the hold time (reasonably) the more time

the signal output has to become more stable. A picture of the C-V plotter system that is used in this research is pictured below as well as a typical theoretical C-V curve for the Si-$SiO_2$ capacitor.

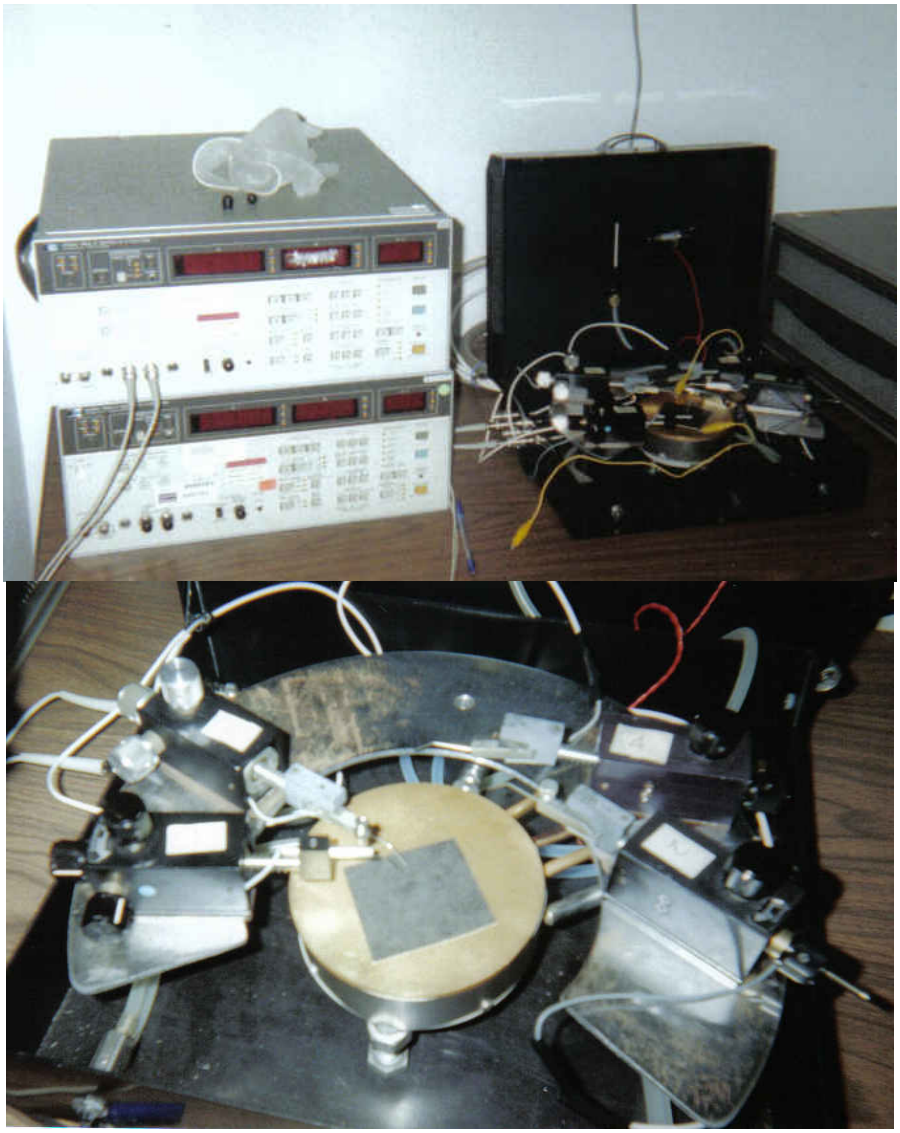

Figure 11: C-V Plotter used in this experiment along with the Signatone probe station with four probe tips.

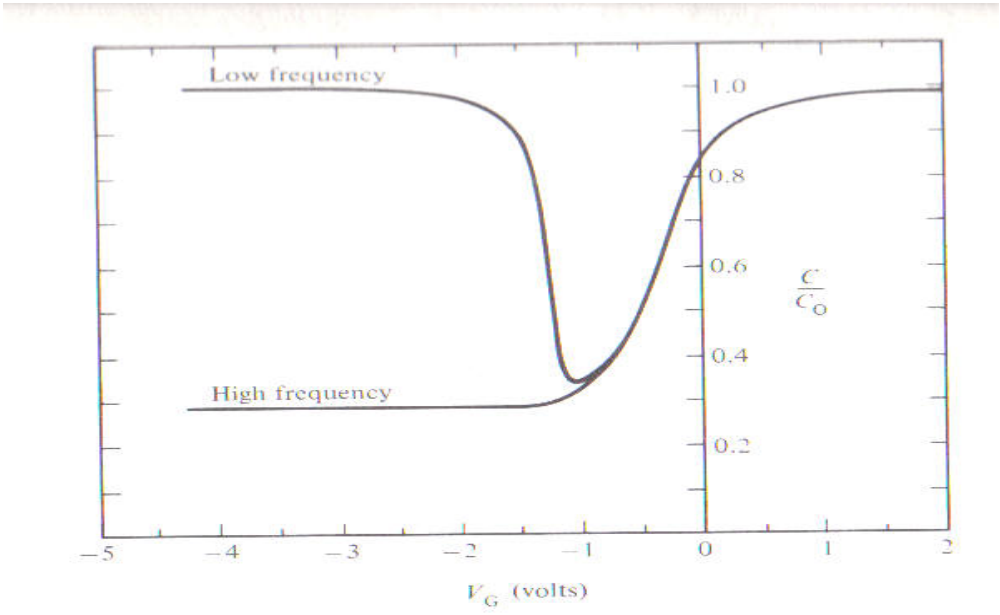


Figure 12: This is a typical n-type C-V curve for silicon-silicon dioxide capacitor [6].

Table 5: Operation parameters for C-V Measurements

| | |
|---|---|
| Start Voltage | 8 to 10 |
| Stop Voltage | -5 to –8 |
| Step Voltage | 1 |
| Hold Time | 40 sec |
| Step Delay Time | 40 sec – 50 sec |
| OSC level test signal | 10 mV |

## Optical Spectrophotometry

The optical spectrum is produced by using a Cary 500i Spectrophotometer. A cleaned unsputtered glass slide is loaded onto both holders to calibrate the machine. After calibration, the actual sample is loaded onto the sample holder closest to the front of the machine (beam side) and the other glass slide is kept in the other holder as a reference. Optical Transmission allows us to find the band gap energy and in some cases the oxide thickness.

## Hall Conductivity

Much of the information on the Hall Conductivity set-up and theory was taken from a website that explains the process [16]. The physical principle of the Hall Effect is the Lorentz force. When an electron moves along a direction perpendicular to an applied magnetic field, it experiences a force acting normal to both directions and moves in response to this force and the force affected by the internal electric field. Since we are working with n-type semiconductor, the carriers are predominately electrons of bulk density **n**. A constant current flow along the x-axis from left to right in the presence of a z-directed magnetic field. Electrons subject to the Lorentz force initially drift away from the current toward the negative y-axis resulting in an excess surface electrical charge on the side of the sample. This charge results in the Hall voltage, a potential drop across the two sides of the sample. This transverse voltage is the Hall voltage. If the magnetic field, current, bulk density and hall voltage is known, the sheet density of charge carriers in the semiconductor can be calculated. If everything is set-up correctly, the Hall voltage should be negative for n-type and positive for p-type semiconductors. The sheet resistance can be found using the van der Pauw resistivity measurement method, there are two characteristic resistances $R_A$ and $R_B$ associated with the terminals. To obtain these two characteristic resistances, a dc current is applied into contact 1 and out of contact 2 and measures the voltage $V_{43}$ from contact 4 to contact 3. Next, a current is applied into contact 2 and it comes out of contact 3 while measuring the voltage $V_{14}$ from contact 1 to contact 4. Since we are never far from Ohm's law, $R_A$ and $R_B$ are calculated using the following expression:

$$R_A = \frac{V_{43}}{I_{12}}$$

$$R_B = \frac{V_{14}}{I_{23}}$$

Equation (15)

Since the Hall Effect set-up uses a script program, determining the sheet resistance, mobility and Hall voltage is relatively simple. The van der Pauw method starts with setting up the sample like the picture below. Four very small ohmic contacts are placed on the corners of the samples and gold wires are soldered to the post in the Hall system. It is placed in the cylindrical test holder between two strong magnetics. Since this experiment is performed in vacuum at room temperature, a mechanical pump is turned on to apply the vacuum in the cylinder.

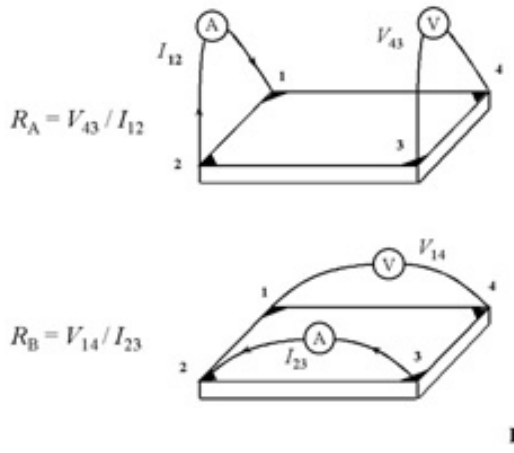


Figure 13: Van der Pauw set-up taken from website [16].

When I am setting up the Hall Effect and resistivity measurements, there are several factors to consider:

1) Sample uniformity and the accurate thickness determination.

2) The quality and size of the ohmic contacts.

3) Thermomagnetic effects due to non-uniform temperature and

4) Photoconductive and photovoltaic effects which can be minimized by measuring in the dark.

## Annealing

The purpose of annealing is to repair the lattice damage created by different types of deposition (sputtering, ion implantation). ZnO thin films were deposited by sputtering on silicon substrates and subsequently annealed in flowing oxygen at temperatures ranging from 500°C to 1100°C for 1 hour. The expectation in thermal annealing is the improvement of ZnO to become more insulating and reduce the number of defects and traps often found within a insulator (imperfect).

Figure 14: This is the oxygen furnace used for annealing made by Lindberg.

## XRD

Expectations: According to the AMPAC write-up, the Rigaku D/MAX XRD should be able to determine the crystal structure and lattice parameters of crystalline materials. As applied to thin films, which is what I am working on, it should be able to give the texture and orientation of the thin films. A very good feature of this equipment is the JCPDS database can be used to give estimated peak locations for unknown samples. Since, I am using zinc oxide; it will give peaks generally known for polycrystalline ZnO. X-ray diffraction is an important non-destructive, non-evasive method that can be used to analysis all kinds of matter. When x-ray radiation pass through materials, that radiation interacts with the electrons in the atoms, it will produce a scattering of the radiation. Destructive or constructive (rays are in phase, Bragg's law can be satisfied) interference can occur based on the crystalline orientation of the material. As a result, diffraction occurs where x-rays are emitted at characteristic angles based on the interatomic spacing between the atoms known as crystalline planes. The interplanar spacing will produce a diffraction pattern characteristic of the angle. Bragg's equation characterizes the relationship between the interatomic spacing, wavelength and the angle at which the x-ray is coming in [18].

$$n\lambda = 2d \sin\theta \qquad \text{Equation (16)}$$

AMPAC uses a copper x-ray target. The x-ray is dispersed toward the sample at a constant small angle because it is thin film. The detector is moving at small incremental angles starting at 2.5 degrees. Initially, there was a lot of noise coming at the detector at the small angles and then eventually more of the actual material became detectable as the angle from 2.5$^{o}$ became larger.

When the x-ray data is analyzed, since the x-ray wavelength is 1.5418Å, there should be peaks at certain theta values with a certain interplanar spacing that should correspond to ZnO as well as ZnS.

# CHAPTER THREE: EXPERIMENTAL RESULTS

Zinc Oxide

Optical Transmission

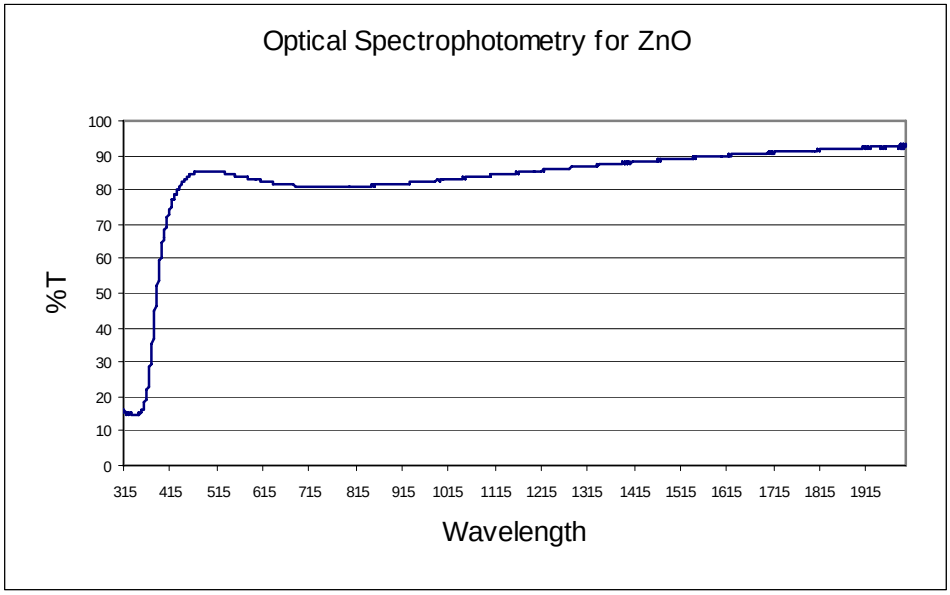


Figure 15: Optical Transmission for ZnO sputtered onto a glass slide.

Figure 15 shows the original data that came from a glass slide that was sputtered with ZnO and this same graph can be used to determine the oxide thickness of the sample if there is some uncertainty. The following expression was solved by taking the peak of the %T curve above at roughly 479 nm, 85.35% and the index of refraction ($n_f$=2.01) for zinc oxide:

$$d = \frac{\lambda_o}{2n_f} \qquad \text{Equation (17)}$$

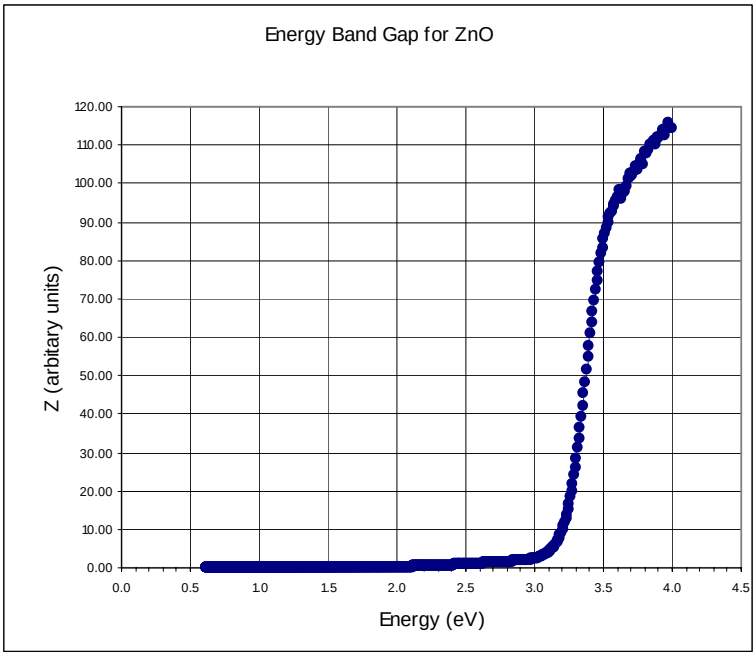


Figure 16: Converted data from optical transmission of ZnO to find energy band gap.

The following equation was used to convert the raw data from the optical transmission into a graph that can be used to extrapolate the energy band gap for ZnO.

$$Z = \left[\left(\ln\frac{1}{T}\right)\frac{hc}{\lambda}\right]^2 \qquad \text{Equation (18)}$$

Where *h*, is Planck's constant, *c* is the speed of light, λ is the wavelength of the raw data, and T is the transmission % from the raw data. The x-axis is converting from the following expression:

$$Energy = \frac{hc}{\lambda} \qquad \text{Equation (19)}$$

Hall Conductivity

Table 6: Experimental Values for ZnO thin film capacitor.

| | | |
|---|---|---|
| Sheet Resistance | 55.4657 | Ohm |
| Mobility | 226.86 | $cm^2/V\text{-}sec$ |
| Sheet density concentration | $4.8608 \times 10^{14}$ | $cm^{-2}$ |
| Carrier concentration | $8.268 \times 10^{17}$ | $cm^{-3}$ |
| Conductivity | 0.3480 | S/cm |
| Resistivity | 2.873 | Ohm-cm |
| Total capacitance | 35.28 | $nF/cm^2$ |
| Depletion capacitance | 48.29 | $nF/cm^2$ |
| $C/C_{MIN}$ | .90 (theo) | .54 (exp) |
| Cox | 76.68 | $nF/cm^2$ |

The Hall Effect was also done on the ZnO films by sputtering contacts onto the film and attaching the gold wires to the contacts (AuPd); table 6 shows the results of that experiment along with what the theoretical minimum capacitance will start at. This minimum capacitance corresponds to the start of strong inversion of the capacitance-voltage curve. This value is calculated from equations found in appendix B. The ZnO film on the silicon substrate shows a decrease in the carrier concentration and an increased resistivity. The carrier concentration, resistivity and mobility is for information only since the theoretical foundation for the calculation of the capacitance is still based upon silicon.

Table 7: Hall Conductivity on select ZnO samples unannealed/unetched and annealed.

| **Annealing Temperature** | **As-Is** | **980°C** | **1040°C** |
|---|---|---|---|
| Sheet Resistance, Ohm | 55.47 | $4.02 \times 10^4$ | $3.17 \times 10^5$ |
| Mobility, $cm^2/V\text{-}sec$ | -226.86 | $-3.59 \times 10^4$ | $-3.64 \times 10^6$ |
| Sheet Density, $cm^{-2}$ | $-4.96 \times 10^{14}$ | $-4.33 \times 10^9$ | $-5.41 \times 10^6$ |
| Carrier Concentration, $cm^{-3}$ | $-8.27 \times 10^{17}$ | $-8.36 \times 10^{10}$ | $-1.05 \times 10^8$ |
| Resistivity, Ohm-cm | 2.873 | $2.084 \times 10^3$ | $1.639 \times 10^4$ |

Table 7 introduces the new side of the ZnO films after they were annealed at different temperatures in oxygen. Different ranges of temperatures were used to find the best point of transition for the surface morphology of the zinc oxide films. The mobility shows a significant increase along with a decrease in carrier concentration. Note, the hall conductivity for ZnO when it is unannealed and unetched is also included to show the difference that annealing makes in the electrical properties of ZnO.

## Capacitance-Voltage Measurements

An experimental C-V for ZnO is pictured below in figure 17. This sample is unannealed and unetched for a p-type substrate.

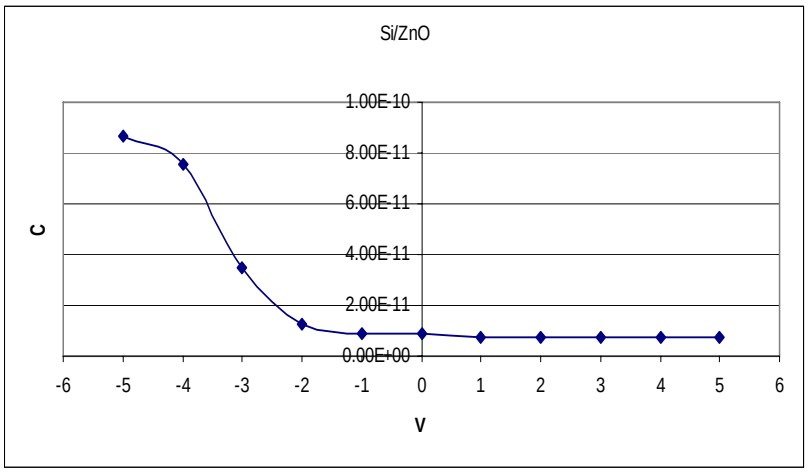


Figure 17: Experimental results for the AuPd/ZnO/silicon capacitors using an p-type substrate from an original sample batch (7-21-06).

The sample in figure 17 came from an original batch of samples that was sputtered last year. One of the initial tasks was to determine the type of substrate used through the hall effect measurement (the manufacturer will specify but with unknown sample history, the hall effect is sufficient to determine this), but with capacitance-voltage measurements it is not necessarily

important. The capacitance-voltage curve will tell you which type of substrate being used. It was swept from positive to negative gate voltage.

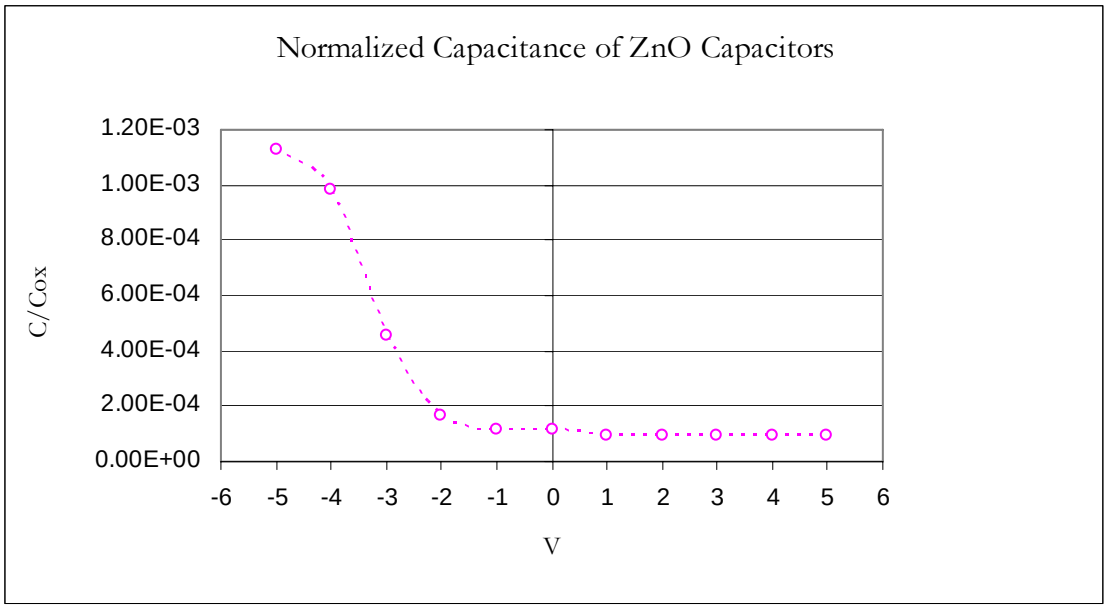


Figure 18: This is the normalized capacitance using the total MOS/MIS capacitance and the capacitance of the ZnO taken from figure 17.

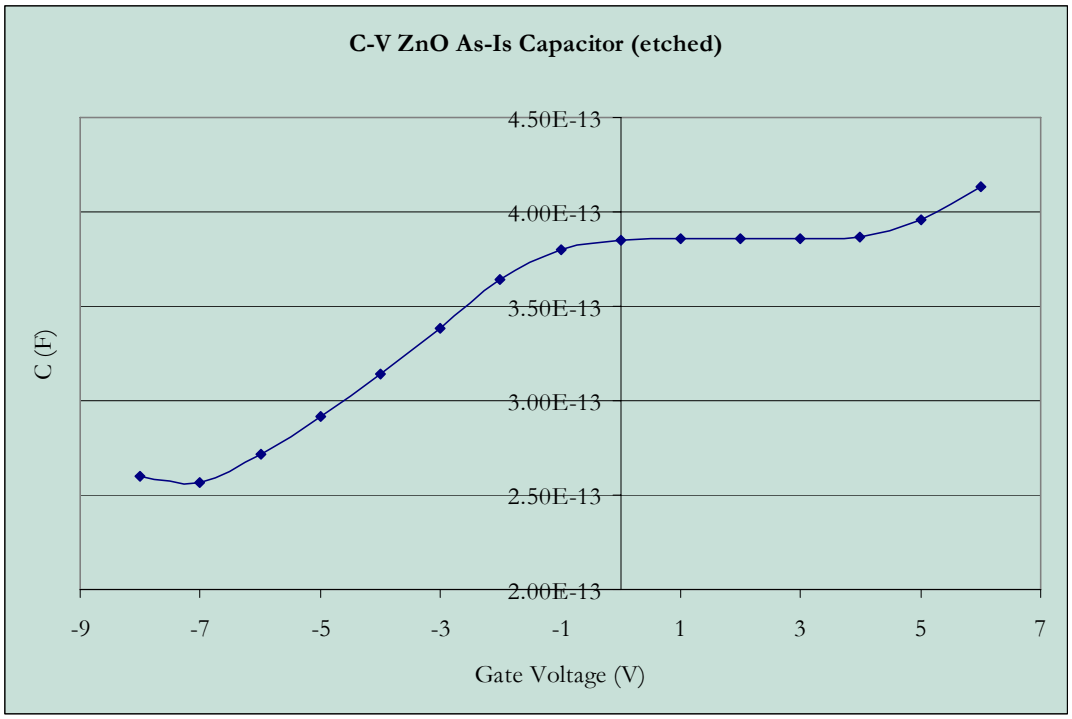


Figure 19: Show one of the ZnO MOS/MIS capacitors that went into deep depletion. This sample has not been annealed in oxygen.

The C-V curve above in figure 19 shows the results of an undoped, unannealed ZnO capacitor that was etched with HCl to reduce the risk of leakage current during the capacitance-voltage measurement. This actually correlates to theoretical C-V curves found. Figure 19 also shows that the minimum capacitance corresponds to the threshold voltage (turn-on voltage) for this particular sample of about roughly -7 volts.

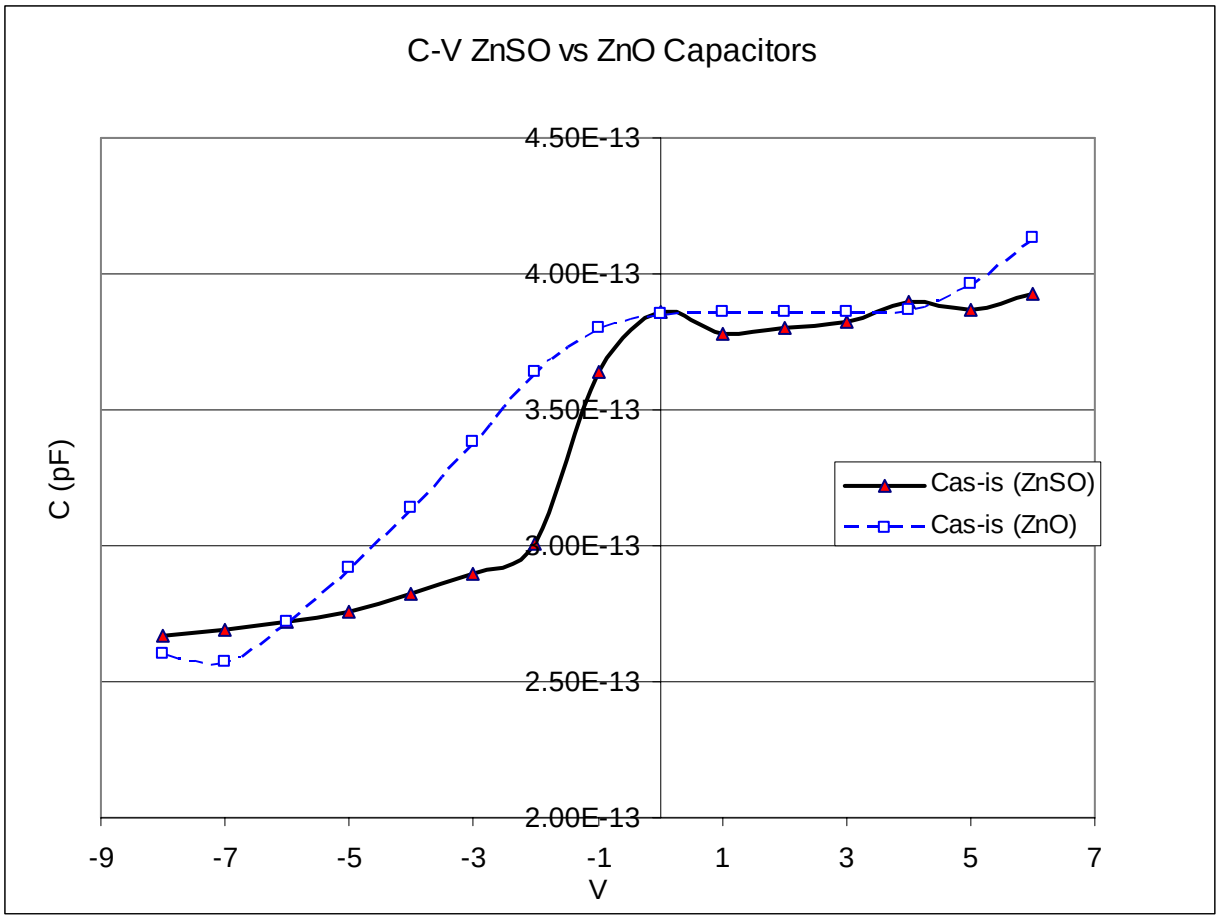


Figure 20: Shows what happens when ZnO is "doped" with sulfur. The depletion region is better defined than in ZnO. They are both unannealed.

I wanted to find out how much of a difference pseudo-doping the ZnO with ZnS since the rf sputtering system is a double target system where just adjusting the voltage divide will give a different composition of materials on the substrate. Figure 20 is a result of that pseudo-doping where the minimum capacitance is more well-defined and the MOS/MIS capacitor is still going into deep depletion. Also notice that the accumulation capacitance (maximum capacitance) correlates a lot closer than in the annealed samples pictured below.

## Annealing

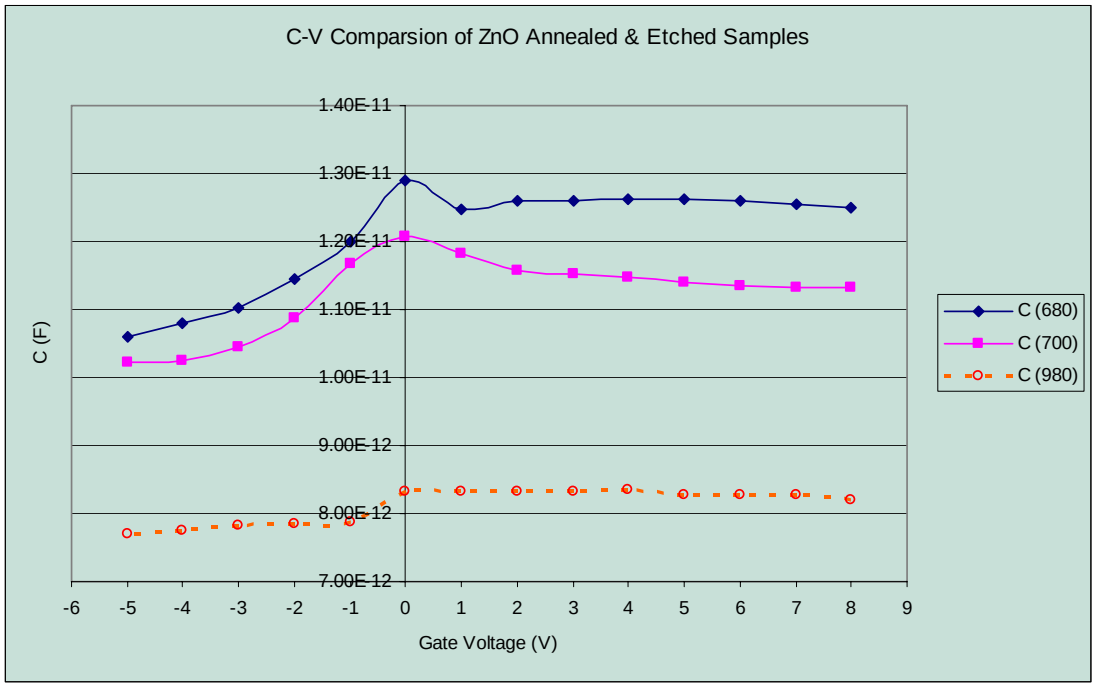


Figure 21: This is a comparison of ZnO samples which have been annealed at the above temperatures for 1 hour.

These samples were annealed at 680°C, 700°C, and 980°C for 1 hour and etched with HCl to prevent leakage current during the C-V measurements. These samples represent the best capacitance-voltage measurements made. Through literature research, the accumulation and inversion regions should be the sample for annealed samples with reasonable variations. The only thing that would change this is non-uniform ZnO composition on the substrate.

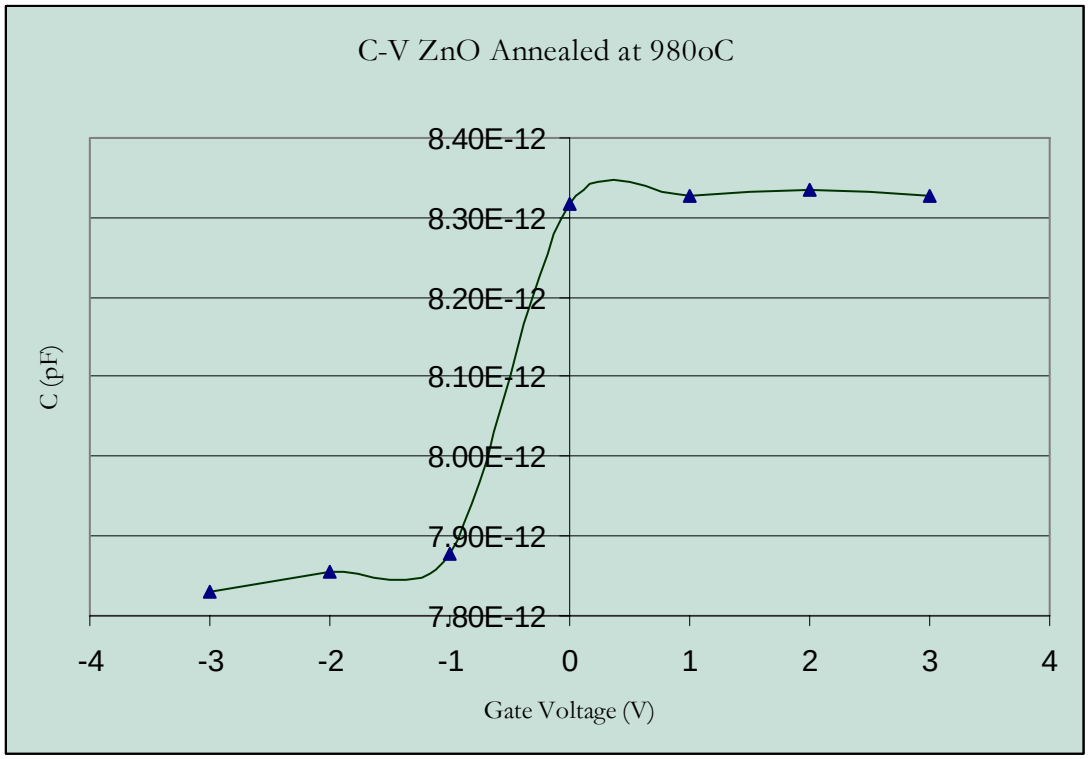


Figure 22: Shows the best example of an annealed & etched ZnO MOS/MIS capacitor.

Figure 22 was annealed at 980°C in oxygen and the points shown were extracted from the original data because the positive voltage after 3V was very chaotic and the points past -3V go into extreme deep-depletion.

X-Ray Diffraction

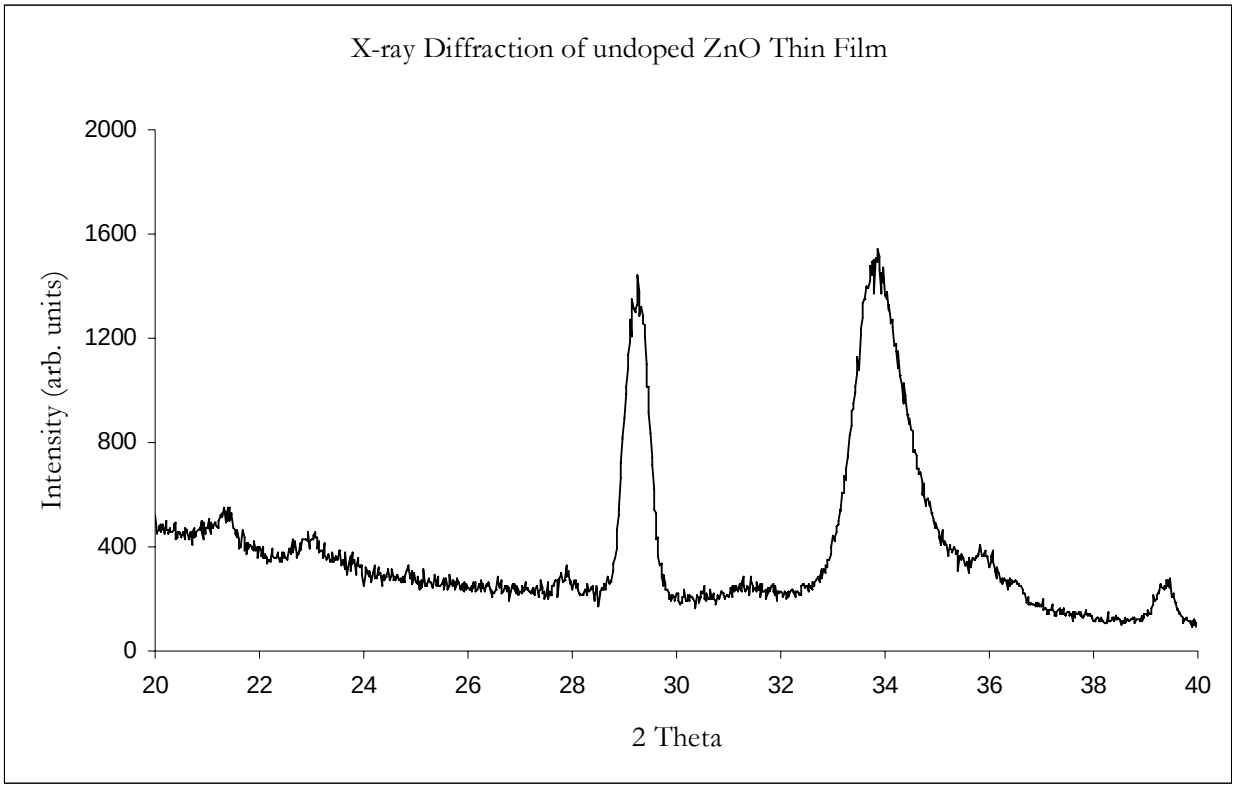


Figure 23: This is the x-ray diffraction for undoped ZnO thin film from the original deposition batch dated 7-21-06 with a main dial 6. There are two major peaks and one minor peak.

Figure 23 shows the x-ray diffraction measurement of ZnO that was deposited at room temperature. This sample was measured un-annealed and unetched. The question of course is whether this shows a polycrystalline or single crystal ZnO sample it will also give a reasonable picture of the interplanar distance at this point. There is one high peak that has its own interplanar distance and orientation relative to the other lattice sites indicated in figure 23.

## Silicon Dioxide

### Hall Conductivity

Table 8: Shows the initial values from the Hall Effect for silicon used to find the theoretical values.

| | | |
|---|---|---|
| $R_s$, Sheet Resistance | 40.49 | Ohms |
| Sample thickness | .0518 ± 0.0002 | cm |
| $\rho$, bulk resistivity | 2.097 | Ohm-cm |
| $\sigma$, conductivity | 0.4769 | S/cm |
| N, carrier concentration | $3.796 \times 10^{16}$ | $cm^{-3}$ |
| $\mu$, mobility | 81.206 | $cm^2$/V-sec |

In order to find out where we stand with the quality or characteristics of the silicon samples being used, the Hall Effect was performed on the sample and table 6 above shows the initial parameters used to form the theoretical results.

### Capacitance-Voltage Measurement

Table 9: Theoretical characteristics calculated from the Hall Effect.

| | | |
|---|---|---|
| $SiO_2$ capacitance | 34.53 | $nF/cm^2$ |
| W, depletion width | $7.996 \times 10^{-6}$ | cm |
| $W_m$, maximum depletion width | $1.599 \times 10^{-5}$ | cm |
| $C_{min}$, minimum capacitance (max depletion width)$SiO_2$ | 65.34 | $nF/cm^2$ |
| C, total capacitance | 22.59 | $nF/cm^2$ |
| $C/C_{min}$ | .35 (exp) | .80 (theo) |

Table 9 contains the values that were calculated using the Hall Effect parameter from table 8. It can be easy to assume from the manufacturer's packing label some of the values from table 8 in order to do a rough estimate, but the Hall Effect gives a reliable approximation to use.

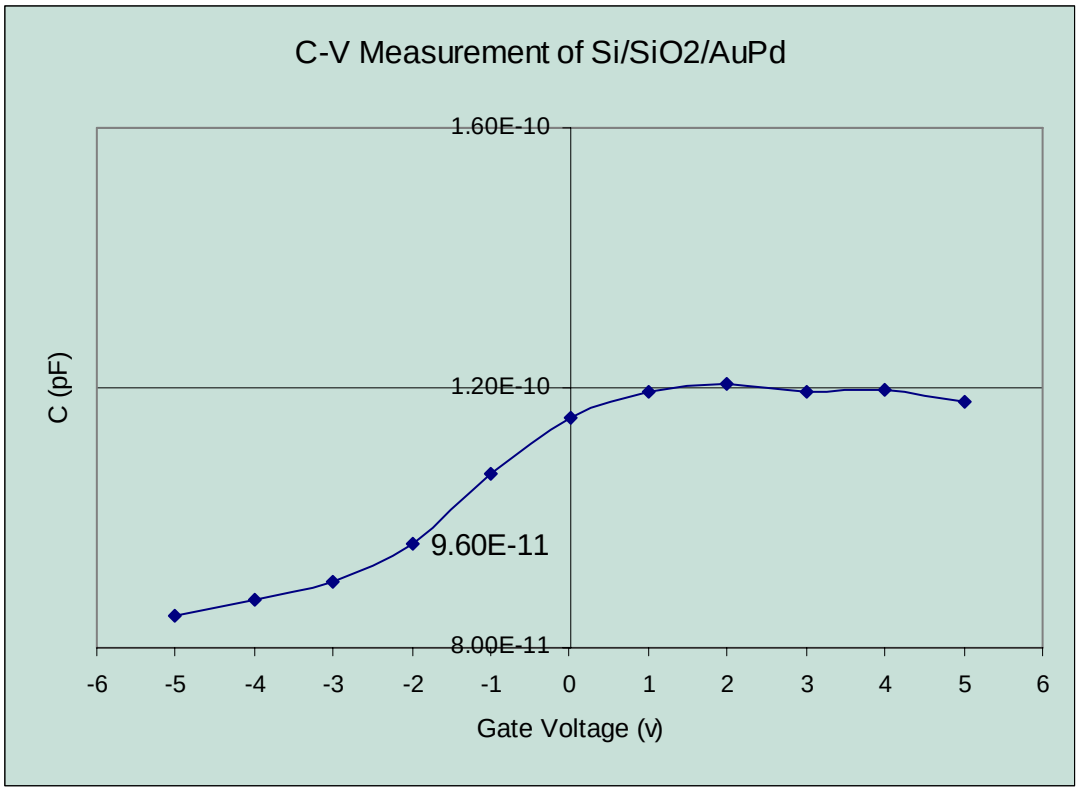


Figure 24: C-V Plot for $Si/SiO_2/AuPd$ with 1000 Ang oxide thickness.

Figure 24 is a plot that was taken of a MOS capacitor using silicon dioxide as the insulator. I need to find a comparison for the ZnO in order to find out if the C-V plotter is giving true values. Figure 24 also shows the three regions discussed in the theoretical section (accumulation, depletion and inversion). Accumulation lies between 1 to 5 V, depletion starts at 1 V and ends at -2 V, and inversion or deep depletion starts at -2 V and goes to -5V.

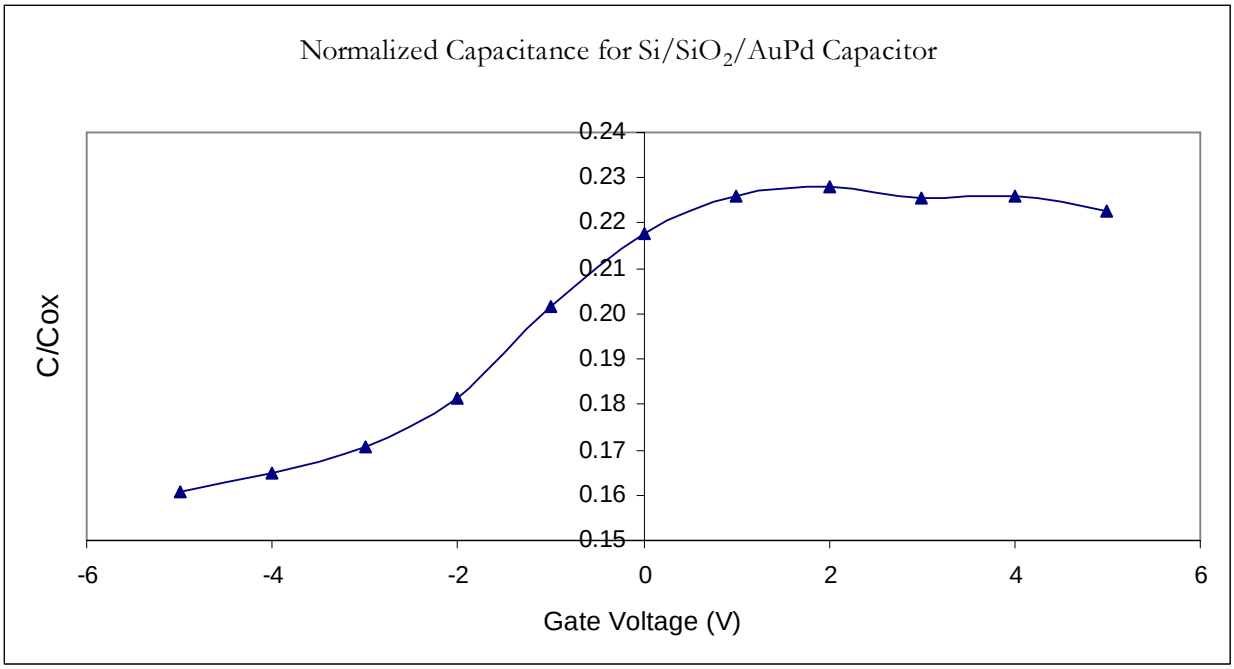


Figure 25: Normalized capacitance for $Si/SiO_2/AuPd$ capacitors.

Figure 25 represents the normalized capacitance of the SiO2 capacitor with an assumed oxide thickness of 1000Å. The silicon dioxide oxide capacitance used to normalize the capacitance-voltage measurement included a gate area of 0.01533 $cm^2$. But in the figure below, I found the difference in the capacitance-voltage measurement for silicon dioxide using the oxide thickness calculated using 1190Å. As you can see the difference in capacitance is fairly significant.

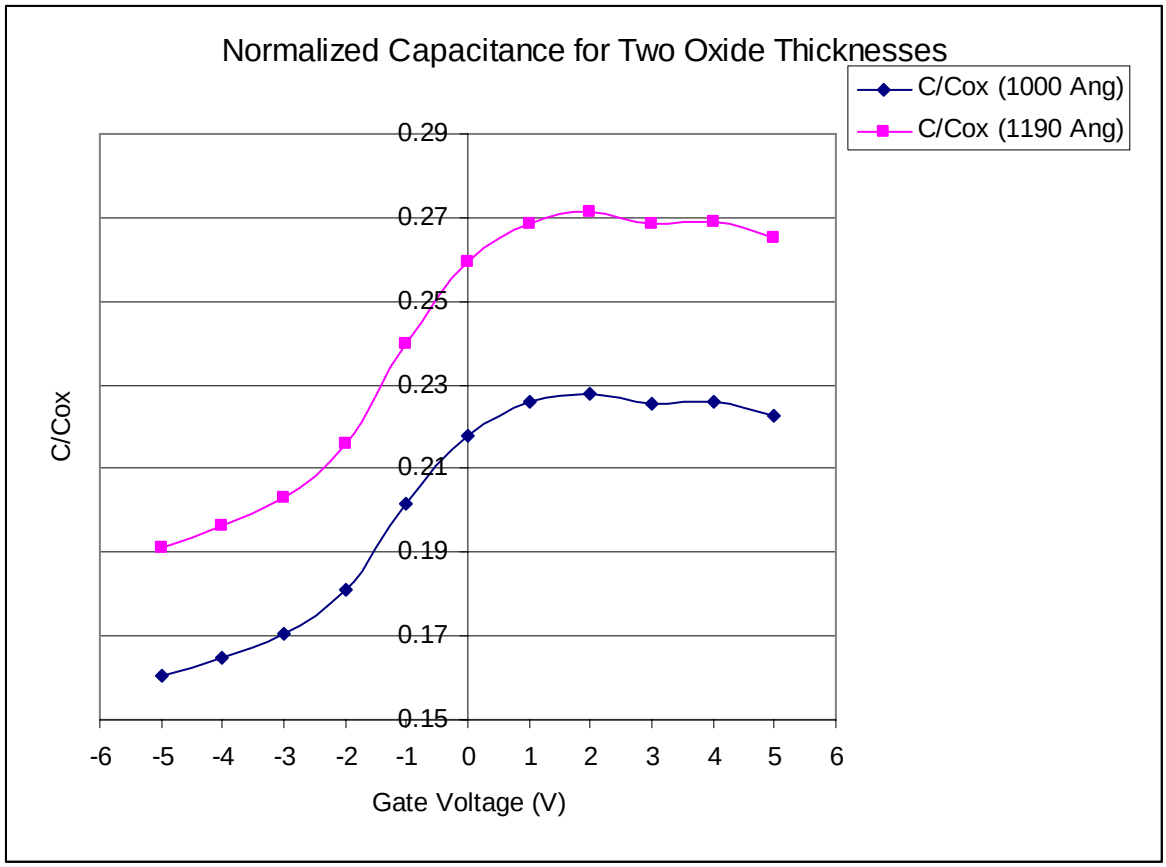


Figure 26: The oxide thickness difference for silicon dioxide demonstrates a significant change in the normalized capacitance.

In my research group the method for sputter deposition was established and followed when the ZnO was sputtered onto the n-silicon. When the silicon dioxide was thermally grown, the diffusion equations were used with reasonable approximation, but figure 26 represents the possibility of a non-uniformly distributed surface that could apply to both ZnO and $SiO_2$.

# CHAPTER FOUR: DISCUSSION OF RESULTS

## Silicon Dioxide

The main objectives of this investigation are to fabricate and characterize a MOS/MIS capacitor using zinc oxide as the dielectric instead of silicon dioxide. Since there has been significant research done on silicon dioxide as the dielectric of a MOS/MIS capacitor, this will be used as a standard to characterize zinc oxide. Also, will thermal annealing improve the electrical properties of zinc oxide?

The Hall effect measurement was used to identify the characteristics of the silicon wafer that is used as the foundation of the MOS/MIS capacitor. The Hall effect also identified key parameters such as the mobility, sheet resistance (used to find the resistivity) and the carrier concentration. These values can be found in Table 8; from these values I was able to calculate the depletion layer width, the capacitance and the bulk resistivity for silicon dioxide. Originally, I thought I was dealing with undoped silicon, but the carrier concentration was too high for undoped silicon. Table 9 contains the theoretical capacitance for silicon dioxide; these values were derived from the Hall effect parameters using theoretical equations which can be found in the appendix. The total capacitance for silicon dioxide is 22.59 $nF/cm^2$. The experimental depletion width for silicon dioxide was smaller which in turn made the experimental capacitance larger.

In figure 24, the minimum capacitance which roughly occurs at -2V corresponds to the onset of strong inversion. It is at this point that the C-V curve goes into deep depletion; the capacitance is not constant. The experimental C-V curve was shallow which could indicate trapped oxide charges and other defects compared to the theoretical curve and it was hard to pinpoint the transition point for the minimum capacitance. It is roughly $9.6 \times 10^{-11}$ farads. Even though the accumulation, depletion and inversion can be seen at their corresponding voltage range, the shallow

depletion range could make it hard to keep the device turned on. One of the cited observations about MOS/MIS capacitors [12] states that the capacitance-voltage curve of an unannealed sample should be higher than the annealed sample because there is a greater surface-state density before annealing using $SiO_2$ as the dielectric. Should this also be true for ZnO?

When I performed the C-V experiment for the Si/SiO2/AuPd capacitor, I placed both probe tips on the contacts in series instead of making a back contact. The oxide was thermally grown onto the silicon substrate at the Solid State Fabrication Lab in Electrical Engineering under the directorship of Dr. Donald Malocha, UCF; based on diffusion equations the engineer technician grew a 1000 Å oxide layer. The back side of this sample needed to be stripped with H.F.(acid): Deionized water in order to remove the oxide on the back. The experimental ratio of the total capacitance to the minimum capacitance is much smaller than the theoretical ratio (see table 9). There are several reasons for this; the doping concentration was higher experimentally (Hall effect) and the mobility was lower experimentally. According to Pierret [7], this lower mobility could indicate a greater number of motion-impeding collisions. Using the n-type C-V curve from figure 12, the minimum capacitance for this curve would be roughly (0.30) which comes close to the experimental $C_{min}$ of (0.35).

When I annealed the $SiO_2$ capacitors, I found that the capacitance raw data was higher when it was annealed at 980$^{o}$C and lowest without annealing, but the points were not consistent graphically after the samples were annealed. A characteristic of interfacial traps in silicon dioxide is the spread out nature of a C-V curve, but these interfacial traps can be minimized with annealing. For example, the interfacial trap charge under inversion becomes a large positive value and it gives rise to a large negative shift in the C-V curve. In depletion and towards accumulation the interfacial trap charge should decrease and the C-V curve should also decrease experimentally. According to

the model in Pierret [6], in accumulation the shifting should continue to decrease and stay negative. In my experimental results for annealing in oxygen, I could not positively identify any shifting. The only C-V silicon dioxide curve that was distinguishable and usable is figure 24 where there was no annealing.

## ZnO

When the optical transmission was performed on a glass slide sputtered with ZnO, the results were used to find and confirm the energy of the band gap is 3.2 eV the percent error from the theoretical band gap energy is 4.15%. Since the optical transmission graph can be used to determine the oxide thickness, I calculated this thickness as 1190Å.

The x-ray diffraction measurement was taken on an unannealed and unetched ZnO sample. The diffraction shows three peaks, one of which is the highest at 33.86$^{o}$ and the second highest is at 29.26$^{o}$, the diffraction tails around the peaks show a lot of phases such as Zn and ZnO along with silicon. According to Subramanyam et al [11], there should be peaks at (002) 43.6$^{o}$ and (102) 54.6$^{o}$ which denotes ZnO at a low temperature. This does not seem to be the case for my Si/ZnO thin fim. The first peak of 29.26 degrees could indicate the silicon substrate with a (100) orientation, the second peak of 33.86 degrees correlates reasonable with the database should in the set-up for a (002) orientation for ZnO; (002) is preferred orientation (c-axis) and indicates a stable plane which is always seen according to several sources researched including Subramanyam et al [11]. The smallest peak may represent the (102) orientation of Zn. This x-ray diffraction would look totally different had the sample been annealed; the (002) peak would have become sharper and higher due to increased crystallinity in the ZnO sample and the other peaks would have decreased significantly.

The Hall effect measurement was performed with a 10 μA current. In table 7, the Hall effect was performed on samples that were unannealed and etched with the oxide thickness being

held constant at 1000 Å. When the sample was annealed and unetched (HCl:DI water), the carrier concentration was lowered from $10^{17}$ to $10^{10}$, the sheet resistance was much higher and therefore the resistivity was higher. In figure 17, a p-type substrate is the base semiconductor. There was a short accumulation region and the depletion started at -4 V and goes to -2 V with a minimum capacitance of 12.61 pF/cm$^2$ after that inversion takes over and it actually follows a somewhat constant capacitance for high frequency. This particular sample is unannealed and unetched with HCl. This sample came from sputter deposition that was done 7-21-06 using the same deposition parameters; the bias voltage range was small from -5V to +5V. The flatband capacitance was 8.62 x $10^{-12}$F/cm$^2$. Since, the ZnO samples were annealed before the contacts were sputtered, there is a possibility (based on temperature) that an additional oxygen layer formed on the ZnO. Why? If silicon is annealed at temperatures of 900$^o$C and above, the silicon oxidizes on the bottom of the wafer and it must be stripped off with HF:DI water. A back ohmic contact cannot be formed otherwise. According to Ko et al [3], there should be an improvement in the crystallinity of ZnO. ZnO when RF sputtered may be uniform across the surface of the silicon, but it is a rough surface that has layers of voids. These voids are a product of the lattice structure of ZnO. Defects also come about by the lattice mismatch between ZnO and silicon which leaves behind dangling bonds. Here is what I hoped happened during annealing as the temperature increased the rough surface starts to expand in all directions to fill in the voids, the surface morphology should be changing from small islands to a smooth surface because the density of the atoms continue to increase. Supposedly, the islands are completely removed at 1000$^o$C, Ko et al [3] suggested that XRD is one way to verify whether the surface morphology actually smoothed out starting at 900$^o$C.

What does annealing mean for the Hall Effect and C-V measurements, in measuring the Hall Effect for samples of AuPd/ZnO/Si, the sheet resistance was very high on the order of $10^4$ to $10^5$

ohm and the carrier concentration was lower due to the increase of grain sizes. Since Zn interstitials can become mobile when annealed, there should be an increase in mobility. According to Sze [12], the capacitance of unannealed $SiO_2$ samples should be higher than annealed samples due to the larger surface states in the unannealed samples. Can the same be said of ZnO? According to the experimental C-V measurements made of the annealed samples to the unannealed samples; the unannealed/unetched ZnO MOS/MIS capacitor had a lower capacitance compared to a sample that was annealed and etched with HCl at 700°C. If you will look at figure 21, you will see a graph of the best C-V annealed ZnO samples. The higher the annealing temperature, the lower the capacitance, but that also corresponds to a well defined depletion region at 980°C compared to the shallow C-V curves at 680°C and 700°C which could still contain some trap charges in the insulator.

$C_{min}$ marks the threshold voltage of the MOS/MIS capacitor, which should be negative according to the theoretical calculations and the equations from Grove [1]; this is the point at which the conductivity type of the surface changes from n to p because there are more holes at the surface than electrons. This is where inversion starts. The sample annealed at 980°C is the only sample that showed a defined depletion region that pinpoints the threshold voltage that is the transition point from depletion into inversion. The threshold voltage is roughly -1V for this n-type sample. *Note:* Since I did conduct a measurement of the I-V curve for Si/ZnO/AuPd capacitor, which is not included in this paper this part is given, only as a suggestion of the kind of device I am working with. A normal I-V curve with good ohmic contacts would display a linear and symmetric graph for silicon dioxide as the dielectric, but my ZnO I-V curve showed a non-linear and asymmetric curve which is indicative of a Schottky contact, if I had annealed with the AuPd contacts on the samples, there is a possibility that the AuPd contacts could have improved to ohmic contacts.

There are errors to be considered as applied to C-V measurements and the Hall Effect specifically. For example, even though the samples are annealed there is still a chance that deep level impurities or traps in the semiconductor bulk can produce error in the C-V curve [12]. Another possible error in regards to the Hall Effect is poor ohmic contact between the gold wire and the metal surface on the capacitor could cause a significant difference in what is being counted as the sheet resistance, mobility and carrier concentration being observed. The carrier concentration could fluctuate in such ways that even the depletion layer width and capacitance calculations could be off by a higher percent. The fabrication process especially cleaning could also introduce unseen impurities and other defects. Another area not to be taken lightly is equipment calibration. According to Pierret [6], it would be easy to underestimate the affect that sodium ions could have on a MOS(FET). Sodium ions in the oxide can cause the threshold/turn-on voltage for both types of channel devices to occur at larger negative gate biases. If a large density of interfacial traps were present, it would cause the gate voltage to change and that in turn would affect the drain current for a given drain voltage. In other words, the gain of a transistor would be reduced significantly due to interfacial traps. It is important not to over look the affect that annealing should have on the ZnO samples; one of the methods to reduce oxygen vacancies, dislocations and zinc interstitials because it will allow the lattice structure to be re-aligned after annealing. If these imperfections are not annealed out, it could cause the C-V curve to be distorted and the threshold voltage could shift significantly. In the Hall Effect, another parameter that could drastically change the results is the wafer thickness. If the wafer thickness is not correctly measured the resistivity is wrong because the system is set-up to calculate the sheet resistance which in turn is used to calculate the resistivity. The next step in this research, it would be to make an actual field effect transistor from the ZnO insulator which would entail changing the fabrication process.

# CHAPTER FIVE: CONCLUSIONS

ZnO was deposited onto silicon by rf magnetron sputtering at room temperature as well as onto a glass slide. These samples were used to study the optical, electrical and structural properties of ZnO Thin Film capacitors. Thermal annealing in oxygen was also conducted on the samples to improve the surface morphology of thin films, but excessive thermal annealing degraded the surface due to bond structures breaking apart at higher temperatures. The capacitance-voltage measurements for several annealed samples were very chaotic and are not shown in this investigation.

The optical transmission of ZnO thin film deposited onto a glass slide was confirmed at the band gap energy of 3.2 eV with a transmission peak at roughly 85%. This sample was not annealed in oxygen therefore the results reflect unannealed conditions. When the $SiO_2$ thin film was annealed at 680°C, the capacitance was lower than the capacitance for the unannealed sample which is in agreement with Sze [12]. When ZnO was annealed the higher capacitance occurred at lower annealing temperatures which are not in agreement with Sze [12]. *Note:* In my original sample batch (7-21-06), (p-type silicon) the capacitance was higher (unannealed) which is in agreement with Sze [12]. Since there was a change in silicon (n-type), the unannealed sample for ZnO had a lower capacitance compared to ZnO annealed at 700°C which appears to be unique to n-type silicon substrates.

X-ray diffraction measurement of the ZnO thin film shows a mixed orientation. The most defined peak in the JCPDS database is the preferred orientation of (002) which indicates a polycrystalline with a wurtzite structure. This is the highest peak out of the three.

In the Hall effect measurements, the unannealed ZnO showed a resistivity of 2.873 Ohm-cm and a mobility of 226.86 $cm^2$/V-sec that is higher than the theoretical value of 200 $cm^2$/V-sec.

When the ZnO was annealed at 980°C, the resistivity jumped significantly to $10^3$ Ohm-cm and the mobility also increased. The silicon used for this experiment also displayed a lower mobility than the theoretical value. The sheet density for the ZnO thin film also decreased with increased annealing temperature; this could be a result of a reduction in oxygen vacancies or Zn interstitials. What does this all mean? In this investigation, the dielectric ZnO was used as the insulator in an MOS/MIS capacitor structure. The threshold voltage (turn-on) was lower in ZnO than in the $SiO_2$ which means less energy is needed to turn the device on. Since all the ZnO and $SiO_2$ samples went into deep-depletion without any obvious recovery to equilibrium I cannot comment on whether there was enough electron-hole pair recombination.

When the experimental data is reviewed for ZnO and $SiO_2$ as insulators, the ZnO did not provide a higher capacitance therefore a better carrier of larger charges. When the ZnO samples are annealed the depletion region improved significantly (980°C) even though the capacitance was not high compared to $SiO_2$ and other annealed samples. This is due to the presence of excess oxygen atoms in the ZnO lattice; this also affected the resistivity of the samples. It is important to control the oxide thickness when using rf magnetron sputtering due to a visible dividing line between two different oxide thicknesses. The change in the oxide thickness will change the capacitance (insulating characteristics) of the MOS/MIS capacitor as well as the parent structure of the MOSFET. When an analytical solution was calculated (appendix B), it showed the total capacitance of a ZnO MOS/MIS capacitor is larger than the $SiO_2$ which has not sufficiently held up experimentally. The ZnO however can only be applied to certain types of devices because the resistivity is high over a range of annealing temperatures such as in surface acoustic wave device and bulk acoustic resonators due to the strong piezoelectric effect. Normally, the goal is to have a low resistivity device, which only was viewed with the unannealed ZnO samples.

# APPENDIX A: THEORETICAL EQUATIONS

I am using the qualitative theory from Pierret (p. 46) compared with the delta-depletion theory also found in Pierret to calculate theoretically the capacitance history points on the C-V curve:

**Q-Theory:**

$$C_{ox} = \frac{K_o A_g \varepsilon_o}{d_{ox}}$$

$$C_{dep} = \frac{C_{ox} C_{semi}}{C_{ox} + C_{semi}}$$

$$C_{dep} = \frac{C_{ox}}{1 + \frac{W}{d'_{ox}}}$$

*where*

$$d'_{ox} = \frac{K_s d_{ox}}{K_{ox}}$$

**Delta-Depletion Theory:**

$$C_{ox} = \frac{K_o A_g \varepsilon_o}{d_{ox}}$$

$$C_{inv} = \frac{C_{ox}}{1 + \frac{W_{\max}}{d'_{ox}}}$$

# APPENDIX B: QUALITATIVE SOLUTIONS FOR THEORETICAL EQUATIONS

These are the analytical solutions for $SiO_2$ and ZnO insulators using the equations above. These calculations comprise the difference in the assumed oxide thickness and the calculated oxide thickness from optical spectrophotometry measurement. This does not take into account gate area.

$SiO_2$

| **Oxide Thickness** | **1000Å** | **1190Å** |
|---|---|---|
| Oxide Capacitance | $C_{ox}^{SiO_2} = 3.45\times10^{-8}\frac{F}{cm^2}$ | $C_{ox}^{SiO_2} = 2.90\times10^{-8}\frac{F}{cm^2}$ |
| Oxide Thickness | $d_{ox} = 3.025\times10^{-5}cm$ | $d_{ox} = 3.60\times10^{-5}cm$ |
| Depletion Capacitance | $C_{dep} = 2.73\times10^{-8}\frac{F}{cm^2}$ | $C_{dep} = 2.37\times10^{-8}\frac{F}{cm^2}$ |
| Inversion Capacitance (strong inversion) | $C_{inv} = 2.256\times10^{-8}\frac{F}{cm^2}$ | $C_{inv} = 2.008\times10^{-8}\frac{F}{cm^2}$ |
| Total Capacitance | $C = 1.36\times10^{-8}\frac{F}{cm^2}$ | $C = 1.19\times10^{-8}\frac{F}{cm^2}$ |
| Ratio of total capacitance to strong inversion | $\frac{C}{C_{inv}} = .60$ | $\frac{C}{C_{inv}} = .59$ |
| Depletion width and Max. depletion width | $W = 7.996\times10^{-6}cm$<br>$W_{\max} = 1.599\times10^{-5}cm$ | |

ZnO

| **Oxide Thickness** | **1000Å** | **1190Å** |
|---|---|---|
| Oxide Capacitance | $C_{ox}^{ZnO} = 7.668\times10^{-8}\,\frac{F}{cm^2}$ | $C_{ox}^{ZnO} = 6.443\times10^{-8}\,\frac{F}{cm^2}$ |
| Oxide Thickness | $d_{ox} = 1.36\times10^{-5}\,cm$ | $d_{ox} = 1.621\times10^{-5}\,cm$ |
| Depletion Capacitance | $C_{dep} = 4.829\times10^{-8}\,\frac{F}{cm^2}$ | $C_{dep} = 4.315\times10^{-8}\,\frac{F}{cm^2}$ |
| Inversion Capacitance (strong inversion) | $C_{inv} = 3.52\times10^{-8}\,\frac{F}{cm^2}$ | $C_{inv} = 3.244\times10^{-8}\,\frac{F}{cm^2}$ |
| Total Capacitance | $C = 2.412\times10^{-8}\,\frac{F}{cm^2}$ | $C = 2.157\times10^{-8}\,\frac{F}{cm^2}$ |
| Ratio of total capacitance to strong inversion | $\frac{C}{C_{inv}} = .68$ | $\frac{C}{C_{inv}} = .66$ |
| Depletion width and Max. depletion width | $W = 7.996\times10^{-6}\,cm$<br>$W_{\max} = 1.599\times10^{-5}\,cm$ | |

# APPENDIX C: THEORETICAL WORKSHEETS AND OTHER DATA

8/10/2006

## Capacitance Calculations for new oxide thicknesses:

**Si/SiO2/Metal:**

| dox | Cox | W | Cdep | Cmin | Total C | C/Cmin |
|---|---|---|---|---|---|---|
| 1.000E-05 | 3.453E-08 | 8.160E-06 | 1.280E-07 | 6.402E-08 | 2.243E-08 | 0.350 |
| 1.1900E-05 | 2.9017E-08 | 8.1600E-06 | 1.2804E-07 | 6.4018E-08 | 1.9967E-08 | 0.312 |
| 2.00E-07 | 1.73E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 1.36E-04 | 0.21 |
| 2.50E-07 | 1.38E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 1.14E-04 | 0.18 |
| 3.00E-07 | 1.15E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 9.76E-05 | 0.15 |
| 3.10E-07 | 1.11E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 9.49E-05 | 0.15 |
| 3.40E-07 | 1.02E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 8.77E-05 | 0.14 |

**Si/ZnO/Metal:**

| dox | Cox | W | Cdep | Cmin | Total C | C/Cmin |
|---|---|---|---|---|---|---|
| 1.00E-05 | 7.67E-08 | 8.16E-06 | 1.28E-07 | 6.40E-08 | 3.49E-08 | 0.54 |
| 1.19E-05 | 6.44E-08 | 8.16E-06 | 1.28E-07 | 6.40E-08 | 3.21E-08 | 0.50 |
| 2.00E-07 | 3.83E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 2.40E-04 | 0.37 |
| 2.50E-07 | 3.07E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 2.07E-04 | 0.32 |
| 3.00E-07 | 2.56E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 1.83E-04 | 0.29 |
| 3.10E-07 | 2.47E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 1.78E-04 | 0.28 |
| 3.40E-07 | 2.26E-04 | 8.16E-08 | 1.28E-03 | 6.40E-04 | 1.67E-04 | 0.26 |

# LIST OF REFERENCES


1) A.S. Grove. Physics and Technology of Semiconductor Devices. New York: Wiley & Sons, 1967, pp. 263-287.

2) Fortunato E., P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira and R. Martins, "Recent Advances in ZnO Transparent Thin Film Transistors", Thin Solid Films, 487 (2005) pp. 205-211.

3) Ko, Hang-Ju, Myung-Soo Han, Young-Sik Park, Yun-Sik Yu, Byong-In Kim, Sang Sub Kim and Jin-Hyeok Kim, "Improvement of the Quality of ZnO Substrates by Annealing", J. of Crystal Growth, (2004).

4) Nandi, S.K., S. Chatterjee, S.K. Samanta, P.K. Bose and C.K. Maiti, "Electrical Characterization of Low Temperature Deposited Oxide films on ZnO/n-Si Substrate", Bull. Mater. Science, Vol 26, No. 7, (2003), pp. 693-697.

5) Nicollian, E.H. and J.R. Brews. MOS (Metal Oxide Semiconductor) Physics and Technology. New York: Wiley-Interscience, 1982.

6) Pierret, Robert F. Modular Series on Solid State Devices: Field Effect Devices. Vol. 4. Massachusetts: Addison-Wesley, 1986.

7) Pierret, Robert F. Modular Series on Solid State Devices: Advanced Semiconductor Fundamentals. Vol. 6. Massachusetts: Addison-Wesley, 1987.

8) Schroder, Dieter K. Modular Series on Solid State Devices: Advanced MOS Devices. Massachusetts: Addison-Wesley, 1987

9) Schroder, Dieter K. Semiconductor Material and Device Characterization. New York: Wiley & Sons, 1990.

10) Serway, Raymond and John W. Jewett Jr., Principles of Physics. 4th ed, California: Thomson-Brooks/Cole, 2006.

11) Subramanyam, T.K., B. Srinivasulu Naidu, and S. Uthanna, "Effect of substrate temperature on the physical properties of DC reactive magneteron sputtered ZnO films", Optical Materials 13 (1999), pp. 239-247.

12) Sze, S. M. Physics of Semiconductor Devices. New York: Wiley-Interscience, 1969.

13) Wolf, S. Silicon Processing for the VLSI Era: The Submicron MOSFET. Vol. 3, California: Lattice Press, 1995.

14) www.mems-exchange.org/catalog/P1998, *Mems and Nanotechnology Exchange: RF-magnetron sputtering.*

15) www.wikipedia.com.

16) www.eeel.nist.gov/812/effe.htm, *National Institute of Standards and Technology: Electronics and Electrical Engineering Laboratory, Semiconductor Division, Hall effect.*

17) http://online.cctt.org/physicslab/content/PhyAPB/lessonnotes.

18) http://www.msc.com/xrd/about_tech.html, Materials Characterization Facility (AMPAC), University of Central Florida