THREE-PORT MICRO-INVERTER WITH POWER DECOUPLING CAPABILITY FOR PHOTOVOLTAIC (PV) SYSTEMS APPLICATIONS

by

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DEDICATION

To

My Father; Mohammad and My Late Mother; Mariam

ABSTRACT

The Photovoltaic (PV) systems have been realized using different architectures, starting with the string and centralized PV system to the modular PV system. Presently, decentralized inverters are being developed at the PV panel power level (known as AC – PV Modules). Such new PV systems are becoming more attractive and many expect this will be the trend of the future. The AC-Module PV system consists of an inverter attached to one PV panel. This integration requires that both devices have the same life-span. Although, the available commercial inverters have a relatively short life-span (10 years) compared to the 25 –year PV. It has been stated in literature that the energy storage capacitor (electrolytic type) in the single-phase inverter is the most vulnerable electronic component. Hence, many techniques such as (power decoupling techniques) have been proposed to solve this problem by replacing the large electrolytic capacitor with a small film capacitor. This thesis will present a quick review of these power decoupling techniques, and proposes a new three-port micro-inverter with power decoupling capability for AC-Module PV system applications.

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1 CHAPTER ONE: Introduction

1.1 Thesis Background: Renewable Energy and Solar potential

With levels of fossil fuels constantly decreasing, humans should find a way to become less dependent on these fuels. The high rate of consumption of fossil fuels is not only depleting these sources rapidly, it is also contributing to climate changes and the polluting of the air and surrounding environments. With carbon emissions at an all time high, air quality can be very low in some areas; this can lead to respiratory diseases and cancer. Figure 1.1 shows the energy production and consumption of the main three energy resources in USA [1]. It is clear the deficit in the produced fossil fuel. On the other hand, the produced amount from the other two clean energy resources is quite small. So, natural and renewable energy sources are needed to take the burden off on fossil fuels. The use of renewable (natural) energy sources to provide electricity is rapidly increasing in popularity among the private and public sectors.

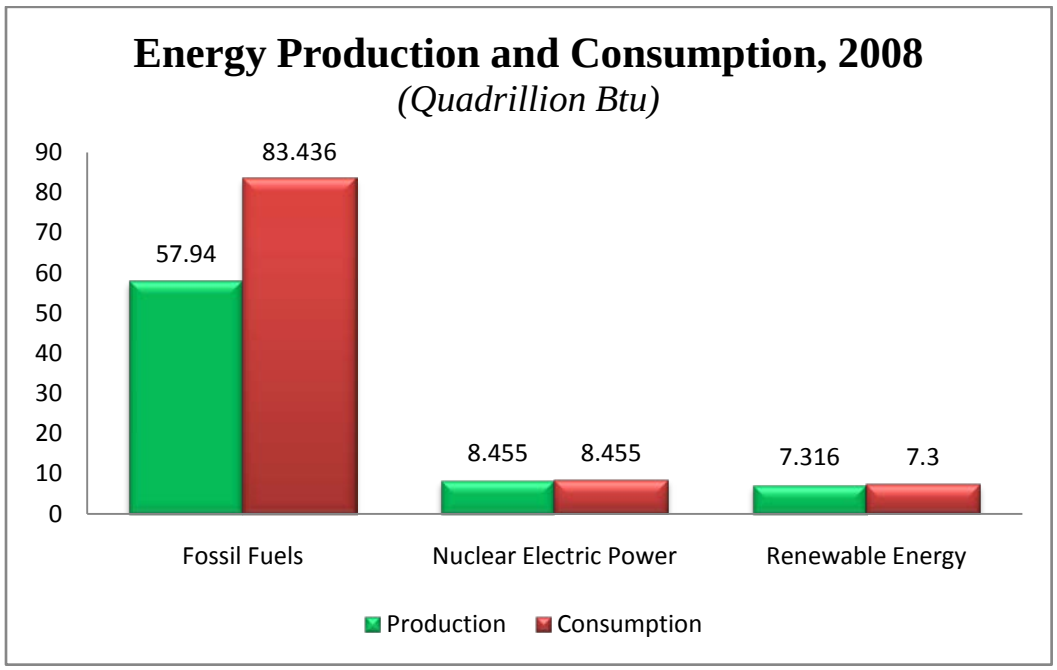

Figure 1.1: Energy Production and Consumption [1].

The three main elements for generating electricity from natural energy sources come in the form of the sun, wind, and tide. Among these three renewable energy candidates, sun energy source has no supply limitations and is predicted to become the biggest contributor to electricity generation.

"The SUN - Your source of natural light and energy for over 5 billion years!

Try it today, free while supplies last..." [2]

According to IEO2009 estimation, world electricity generation increases by 77 percent from 2006 to 2030, which increases from 18.0 trillion kWh in 2006 to 23.2 trillion kWh and 31.8 trillion kWh in 2030[1]. Based on the most advanced scenario which corresponds to IPCC emission reduction targets, renewable energy, by 2050, will account for 46% of global power. Among the renewable energy technologies, photovoltaic will play a major role. To meet the 2020 renewable energy targets of the European Union, the European Photovoltaic Association(EPIA) recently estimated that the possible contribution of photovoltaic up to 12% of the electricity supply by 2020[3]. The produced amount of energy by each energy source is presented in Figure 1.2. Yet, because of the high cost of the PV system, the energy from the sun (PV) is very low compared to other resources. Although, Figure 1.3 shows the cost of the PV cell and module in the last two decades, which tends to decrease due to a mass production along with using new fabrication technologies. The cost of the inverter stage becomes more dominant in the total PV system's cost [1].

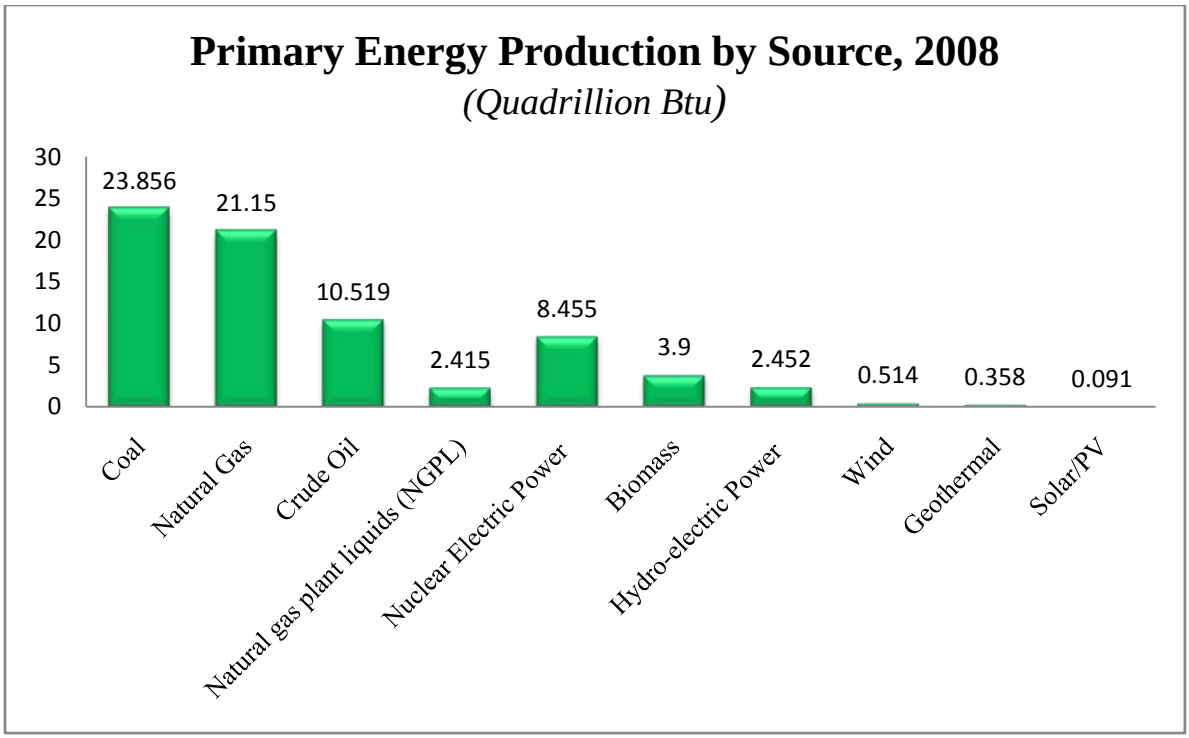

Figure 1.2: Primary Energy Production by Source, 2008 [1].

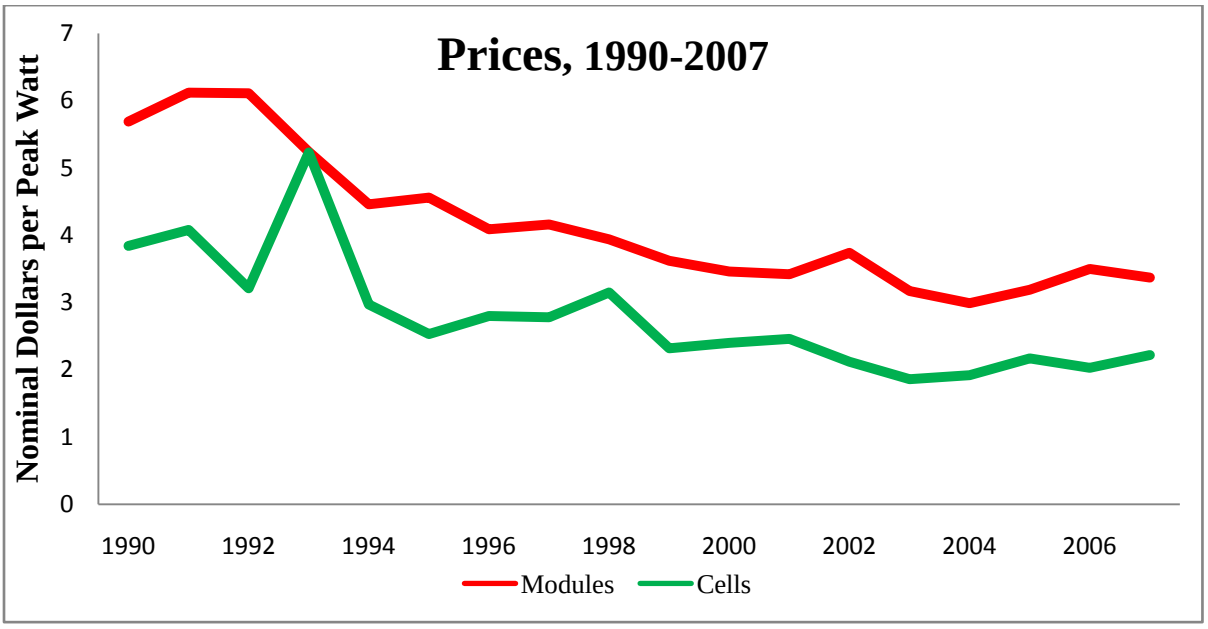

Figure 1.3: Photovoltaic Cell and Module Prices, 1990-2007 [1]. Note: Prices equal shipment value divided by quantity shipped. Value includes charges for advertising and warranties. Excluded are excise taxes and the cost of freight or transportation for the shipments].

1.2 Solar Energy: Photovoltaic System

Distributed generator (DG) renewable resources using photovoltaic systems are becoming more attractive among homeowners. DG resources can be in two forms, stand-alone or grid-connected. Stand alone DG systems are more useful in non-electrified regions, especially in developing countries, where the grid cannot reach these regions due to high cost [4]. On the other hand, grid-connected PV systems can be used everywhere and they are spreading rapidly due to their advantages. Grid-connected PV systems are easy to install at homes, schools, any public buildings. The generated electricity from these DG systems will mitigate the burden on the grid. In addition, the extra electricity will be pumped into the grid.

In both, stand-alone and grid-connected DG systems, an interface stage between them and the end user is needed to convert the generated power to a usable form. Power electronic plays an important role in the field of modern electrical systems that based on renewable sources. Renewable energy sources generate either DC or variable frequency AC and require some form of power conversion to generate a form that is compatible or required by the end user. Power electronic is an essential part for the integration of renewable energy system to achieve high efficiency and performance in power systems. The main goal of the power electronics technology is to convert electrical power from one stage to another stage as efficient as possible with a high level of intelligence.

In view of the fact that photovoltaic (PV) grid-connected system generates a DC power an DC/AC conversion stage (Inverter) must be used to convert the generated DC power into an acceptable AC power. The output of this stage has to satisfy all the standards required by the utility grid. In the subsequent sections we will explore the developments that have been done on the PV systems.

1.3 Grid-Connected Photovoltaic (PV) System

For grid-connected applications, there are several standards that must be guaranteed by the power inversion stage in the PV system. The dc-injected currents, total distortion harmonic (TDH), power factor, detection of islanding operation, and other factors all of them are governed by standards like IEEE 1547[5], IEC 61727[6] and NEC 690[7]. These standards aim to guarantee that the MIC injects high quality power to the grid. Table 1 lists the key parameters in these standards. The power inversion stage in the grid-connected PV system must accomplish some or all of the following tasks:

- Maximum Peek Power Tracking, MPPT
- Power decoupling
- Boost the PV dc input voltage
- DC-AC power conversion
- Provide interfacing between the PV side and the grid side (electrical isolation and detection of islanding operation)

1.4 Photovoltaic (PV) System

1.4.1 Centralized PV System

PV systems start with the centralized multi-string PV system, Figure 1.4. This system uses one huge inverter. Each PV string consists of multi-PV panel connected in series where then group of these strings are connected in parallel forming a high power centralized PV system. [8]

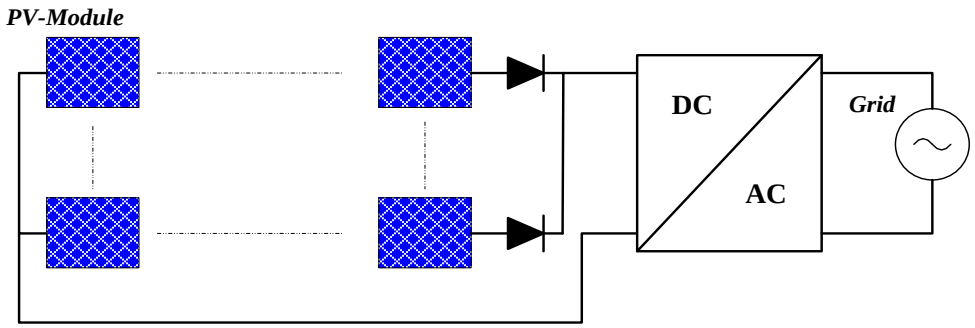

Figure 1.4: Centralized PV-System.

Although no amplification stage is needed but the power losses in the string diodes and the connection cables deteriorate the efficiency of this type. Furthermore, the mismatch between the module's tracking systems (maximum power point tracking MPPT) reduces the amount of the captured power. Therefore, new PV system approaches were used [8].

1.4.2 String PV System

Figure 1.5 shows two PV system approaches, string and multi string respectively. To overcome the losses due to the MPPT mismatch and the string diodes, each PV string is assigned its own inverter. The amplification stage can be avoided if the number of the PV panel is enough to generate the required DC input voltage, ≈ 190V for US system. Each PV-string has an MPPT which leads to improve the overall efficiency by increasing the captured energy. However, the cost of the inverter in this case increased due to the low power level.

The other approach is the multi-string PV system. In this case, each PV-string is assigned a DC/DC converter and all of them are connected in parallel to one inverter. Also here each string has a MPPT and can be controlled individually. The inverter in this case has a higher power level like in centralized case with higher efficiency. Yet, in both approaches, there is still some MPPT mismatch between the modules of one PV string. Consequently, not all available

energy from the sun can be captured by the installed PV system. Hence, the AC-Module PV system becomes the most efficient approach that guarantees 100% harvesting of the available power [8][9][10].

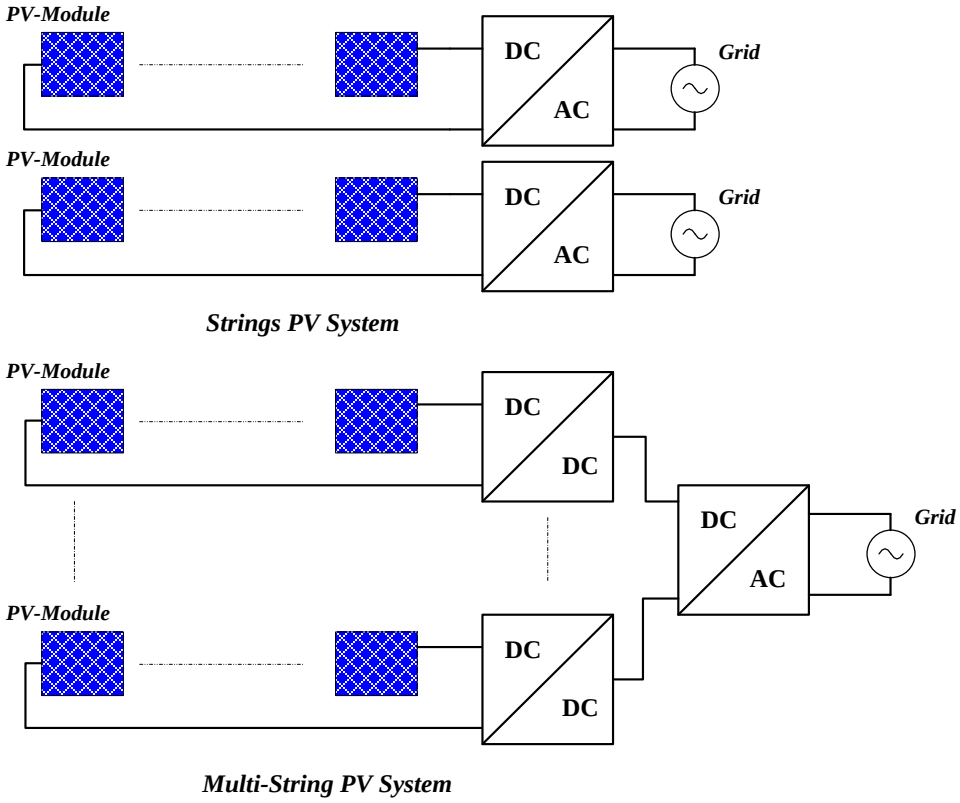

Figure 1.5: String PV and Multi-String PV Systems.

1.4.3 AC-Module PV System

The AC-module PV system is shown in Figure 1.6; where one DC/AC converter is attached to the PV panel. The definition of the AC-module is given as:

> *"An AC-module is an electrical product and is the combination of a single module and a single power electronic inverter that converts light into electrical alternating (AC) power when it is connected in parallel to the network. The inverter is mounted on the rear side of the module or is mounted on the support*

structure and connected to the module with a single point to point DC cable. Protection functions for the AC side (e.g. voltage and frequency) are integrated in the electronic control of the inverter." [9].

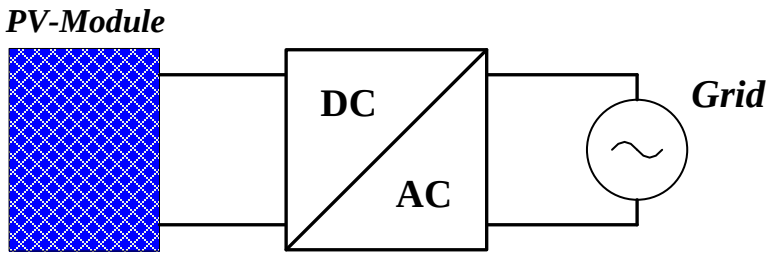

Figure 1.6: AC-Module PV System.

It is believed that this approach will be the trend for the future PV industry. In this kind of PV system, the MPPT problem is completely solved since each PV panel is connected to one inverter that has an MPPT. The AC-Module PV system offers Plug-N-Play concept. This option gives a high order of flexibility. This flexibility in the system makes it more common and easy to be used for end user application. Moreover, the modularity provided by the AC-Module PV system makes the future expansion of the whole system easier.

The available PV panels in the market, mono- and multi-crystalline silicon, have a MPP voltage in the range from 23V to 38V, and 45V at open circuit; 160W-300W [8] [11]. Therefore, it is desirable that the power electronic inverter in the AC-Module can operate in wide input voltage range to adapt the wide output voltage range of the PV panel, which may make the optimization design more challenging. Because of the low output voltage for the PV panel an amplification stage before the inversion process becomes indispensible. Either transformer or a DC/DC converter is used to accomplish the amplification; where the DC input voltage is amplified to a voltage level compatible with the grid voltage. Plug-N-Play concept that enhances the flexibility of the PV system requires that the power electronics stage (the inverter) is

integrated with the PV panel as it is stated in the definition of the AC-Module, so that it is called module integrated converter (MIC) in many references. Hence, the reliability (life-span), weight, and volume of the inverter become more important and have a vital role on the system.

The life-span of the inverter should be comparable to that of the PV panel; which is more than 20 years. The available (commercial) inverters used in AC-Module PV-system have a life-span less than the PV panel; about 3-6 years. Although, many researches have been done to solve this issue and find a new inverter with high life-span, yet this problem is one of the biggest challenges that researchers trying to solve it. The reliability of the inverter is measured by two indices, mean time to first failure (MTFF) and mean time between failures (MTBF). Inverters nowadays have 5 years for MTFF and 10 years for MTBF. The most vulnerable parts in the inverter are the power switches and the power decoupling capacitor; which have a strong impact on its life-span. The latter is the subject of this thesis and it will be discussed in more details in next chapters [8][11][12][13].

1.5 The cost Issue

The cost of the AC-Module PV system can be studied from two perspectives. The cost of the micro-inverter (MIC) alone and the cost of the AC-Module system as one package (the MIC and the PV panel). Due to low power level for the micro-grid inverter the cost per watt is high. The manufacturing cost will be reduced if a mass production is achieved. This is feasible in the AC-Module PV-system case since it is intended to be mass produced. Another feature for the AC-Module that also will reduce the overall cost comes from the fact that the MIC is connected directly to the grid with Plug-N-Play feature, which means that dc cabling and installation expertise are not necessary any more. This in turn reduces (or even eliminates) the cost of

installation. Figure 1.7 shows that about 1/3 (32%) of the cost of a PV system is for installation. By reducing this cost, the one can pay more on the MIC [14]

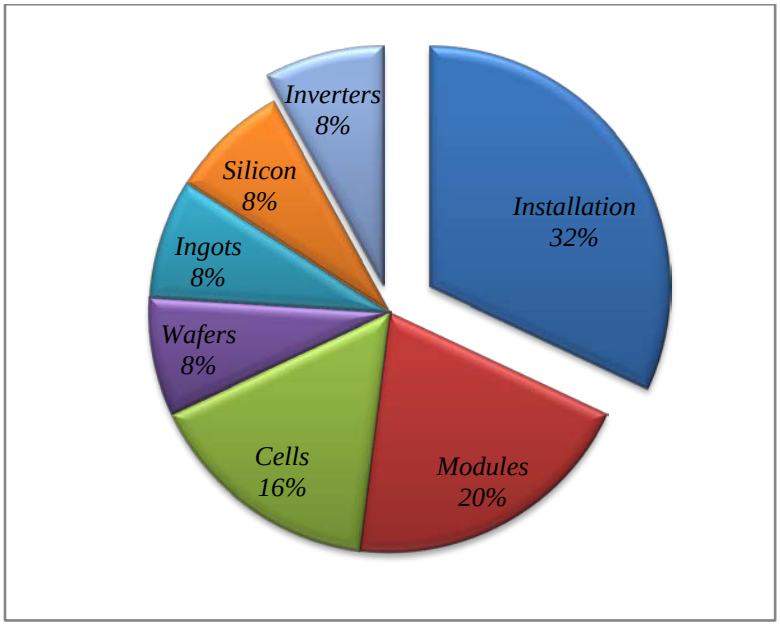

Figure 1.7: Composition of the photovoltaic power costs.

1.6 Thesis Outline

Chapter Two: the double-frequency power ripple problem in single-phase grid-connected inverter is explored in this chapter. It also presents different power decoupling techniques that aim to solve power ripple problem along with a reasonable comparison between them at the end of this chapter.

Chapter Three: A new three-port Micro-Inverter with a power decoupling capability is proposed in this chapter. Detailed analysis of the operation of this new topology is shown followed by the simulation results.

Chapter Four: Conclusion and future work.

2 CHAPTER TWO: DOUBLE-FREQUENCY POWER REIPPLE IN SINGLE PHASE MICRO-INVERTER AND POWER DECOUPLING SOLUTION

2.1 Double-Frequency Power Ripple in Single-Phase Micro-Inverter

In grid-connected single-phase inverter shown in Figure 2.1; assume that the injected current to the grid is given in 2.1 and the grid voltage which is given in 2.2.

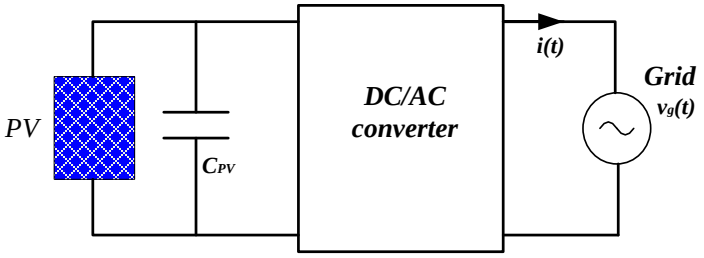

Figure 2.1: Single-Phase Inverter Architecture.

$$i(t) = Isin(\omega_o t + \varphi) \tag{2.1}$$

$$v_g(t) = V_g \sin(\omega_o t) \tag{2.2}$$

Where ω_o is the grid frequency and φ is the phase difference between the injected current and the grid voltage; which is desired to be zero for unity power factor operation. The instantaneous output power, $P_o(t)$, is given as follows:

$$P_o(t) = v_g(t) * i(t) \tag{2.3}$$

$$P_o(t) = \frac{1}{2}V_g Icos(\varphi) + \frac{1}{2}V_g Icos(2\omega t + \varphi) \tag{2.4}$$

If $\varphi = 0$, then $P_o(t)$ will be

$$P_o(t) = \frac{1}{2}V_g I + \frac{1}{2}V_g Icos(2\omega t) \tag{2.5}$$

The instantaneous power in (2.5) consists of two terms. The average output power$\left\{P_{o_{av}} = \frac{1}{2}V_g I\right\}$; which is constant. The second term $\left\{P_{o_{ac}}(t) = \frac{1}{2}V_g Icos(2\omega t)\right\}$ is a time varying term

with a twice line frequency oscillation. On the other hand, the power from the PV panel is controlled by the maximum power point tracking (MPPT) system and kept constant, $P_{PV} = P_{dc}$. By ignoring the losses in the inversion stage, the power generated by the PV panel will be equal to the average output power, $P_{o_{av}}$, as shown in Figure 2.2

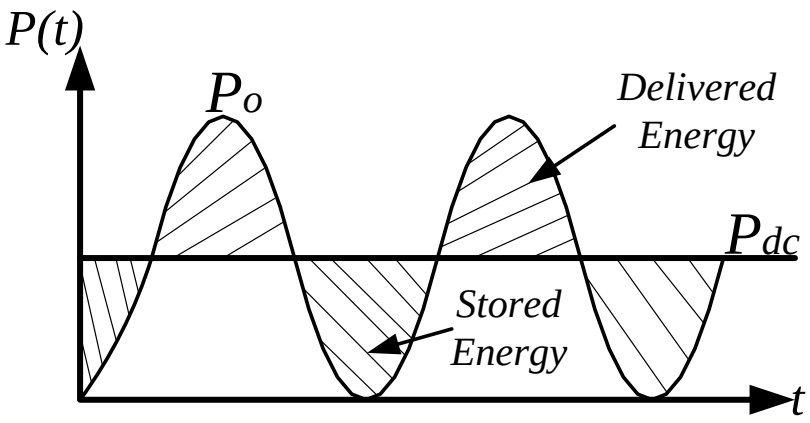

Figure 2.2: The total power processed by the decoupling capacitor.

The time varying term will degrade the PV system performance. This ripple has a strong negative impact on the MPPT system; where MPPT is trying to track the voltage and current which result in the maximum output power from the PV panel. Having this time varying components (voltage and current) at the PV panel will prevent from getting the maximum power and deteriorate the AC-Module's overall efficiency [2] For this reason, the pulsating power, $P_{o_{ac}}$, must be handled by an energy storage device. Usually, a capacitor (Decoupling Capacitor) is used to mitigate the power ripple effect at the PV panel. This decoupling capacitor can be embedded somewhere in the inverter or it just connected in parallel with the PV panel. The latter technique, Figure 2.2, has been used in almost all commercial inverters. Even though, it is an easy technique and straight forward to be employed but it is an eminent drawback in terms of life-span.

2.2 The Size of the Decoupling Capacitor

The value of the decoupling capacitor is determined based on the amount of the energy that has to be stored in the capacitor which is represented by the shaded area in Figure 2.3.

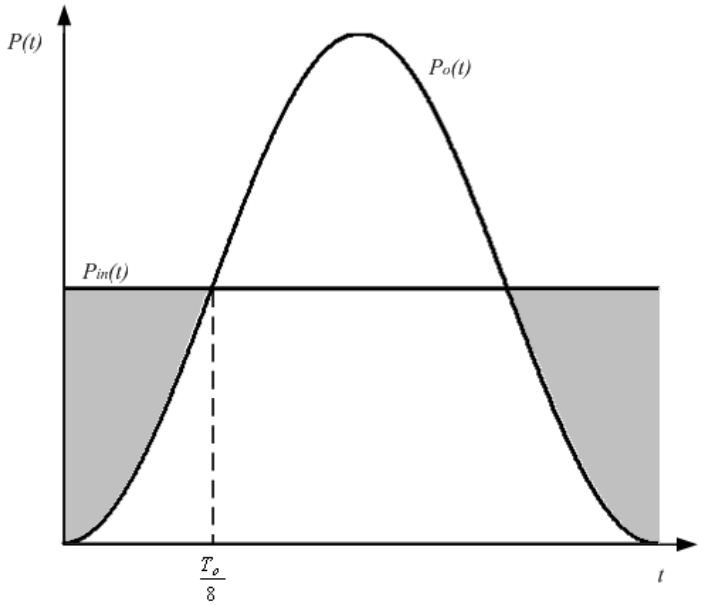

Figure 2.3: Input and Output Power Waveforms.

The energy stored in the decoupling capacitor during a half AC cycle can be calculated by integrating the shaded area as follows:

$$E_{C_D} = 2\left(\int_0^{T_o/8}(P_{in} - P_{ac}(t))dt\right) = \frac{1}{2}C_D\left(V_{C_D max}^2 - V_{C_D min}^2\right)$$

$$\frac{1}{2}C_D\left(V_{C_D max}^2 - V_{C_D min}^2\right) = P_{in}\frac{T_o}{4} - 2\left(\int_0^{T_o/8} V_o I_o sin^2(\omega_o t)dt\right)$$

Then, the decoupling capacitor is given by (2.6)

$$C_D = \frac{V_o I_o}{\omega_o\left(V_{C_D max}^2 - V_{C_D min}^2\right)} \tag{2.6}$$

Where:

$$P_{in} = \frac{V_o I_o}{2}$$

The Decoupling capacitor voltage can be expressed as follows:

$$V_{C_D max} = V_{C_D}(DC) + \frac{\Delta V_{C_D}}{2} \quad (2.7)$$

$$V_{C_D min} = V_{C_D}(DC) - \frac{\Delta V_{C_D}}{2} \quad (2.8)$$

Then, the final expression for the decoupling capacitance is given by (2.9).

$$C_D = \frac{2P_{in}}{2\pi f_o\left(4\frac{n_1}{n_2}V_{dc}V_o\right)} = \frac{P_{in}}{\omega_o\left(V_{C_D}(DC)\right)\Delta V_{C_D}} \quad (2.9)$$

Where:

C_D: The value of the decoupling capacitor.

P_{in}: The power generated by the PV panel, which is can be considered a constant because of the MPPT system.

ω_o: The angular frequency of the grid, $\omega_o = 2\pi f_o$.

$V_{C_D}(DC)$: The DC voltage level across the decoupling capacitor terminals.

ΔV_{C_D}: The maximum allowable peak-to-peak voltage variation across the decoupling capacitor.

Providing that the MPPT system is controlling the output of the PV panel, it is clear from the expression in (2.9) that the only two components that can be chosen by the design engineer are the DC voltage level, $V_{C_D}(DC)$, and the allowable voltage ripple, ΔV_{C_D}. Therefore, the value of the decoupling capacitor is determined by these two values. In the aforementioned conventional technique; where the decoupling capacitor is connected in parallel with the PV

panel there are constraints on both the DC voltage level and the voltage ripple; where $V_{C_D}(DC) = V_{PV}$ and ΔV_{C_D} should not exceed a specific percentage, usually not exceed 8% of the nominal value, in order to get the maximum power from the PV panel. For a typical PV panel with the following values: $P_{in} = 200W$ and $V_{C_D}(DC) = 35V$. Assume $\Delta V_{C_D} = 2V$, the minimum value of the decoupling capacitor is 7.6mF in order to achieve a 98% PV utilization factor [8]. Hence, a large electrolytic capacitor is needed, which increases the size of the micro-inverter and may negatively impact its life span.

Figure 2.4 shows the relationship between the minimum required decoupling capacitor and the voltage ripple across its terminals at different DC voltage levels. It is quite clear that as the DC voltage level and the allowable voltage ripple increase the needed decoupling capacitor reduces. Thus, a small non-polarized (film) capacitor can be used instead of the large electrolytic one.

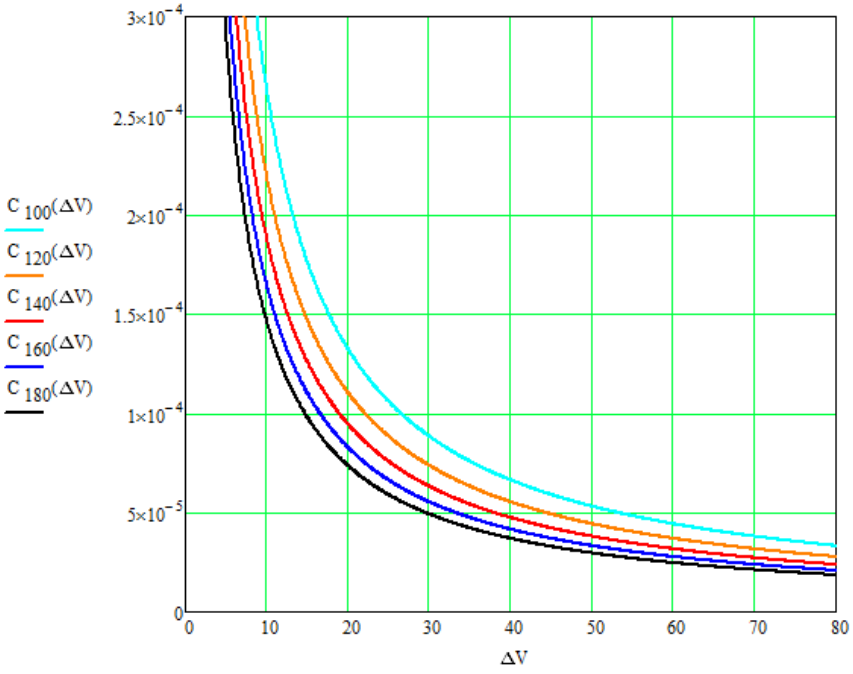

Figure 2.4: The Minimum Decoupling Capacitor (C_D) versus the allowable ripple at different DC voltage level

In the previous chapter we explained the importance of the reliability of the inverter; especially if it is needed to be used in AC-Module PV system. It is desirable that its life-span is close to the PV panel's one. It was found in literature that the electrolytic capacitor is the most vulnerable device in the inverter; so a film capacitor is used. Unlike the electrolytic capacitor, the film capacitor said to have longer life-span (better reliability). The life-span of different types of capacitors varies greatly, e.g. electrolytic capacitors typically have a limited lifetime, namely 16,000 hours at 75^{o}C operating temperature [15]. Assuming that the PV system has an average operation of 8 hours/day, then the actual life-span of the capacitor is less than six years. While life-span of film capacitors is about 80,000 hours at the same operation temperature. Then, it will last 27 years almost providing 8 hours/day operation.

In order to be able to use film capacitors as an energy storage device in the inverter, there shouldn't be any constraints on the DC voltage and voltage ripple across the decoupling capacitor. Figure 2.4 shows the decoupling capacitance for five different DC voltage levels. It is noticeable that for all DC voltage levels, voltage ripple above 50V will allow us to use a small capacitor with a capacitance $\leq$50μF. This implicitly means that the decoupling capacitor cannot be connected in parallel with the PV panel. So, it should be integrated somewhere in the inverter, where there is no strong constraint on the DC voltage level and the voltage ripple. Different decoupling techniques have been proposed in literature which will be presented and categorized in next section.

2.3 Power Decoupling Techniques for Micro-Inverter

As it has been shown before, the electrolytic decoupling capacitor has relatively short life-span compared with other components in the inverter. More important, the short life-span of

the decoupling capacitor makes attaching the inverter to the PV panel more complex, inefficient, and expensive. During the last few years, many efforts have been addressing this problem. Researchers have been trying to solve this problem from different point of view. This section focuses on the power decoupling techniques which have been proposed in the last few years.

Figure 2.5 shows the possibilities where the decoupling capacitor can be placed in single-stage inverter option. The dotted line means that the capacitor is embedded somehow in the inverter circuit. Different scenarios for multi-stage inverter options are shown in Figure 2.6, where Figure 2.6 (a) shows the possible places where the decoupling capacitor can be employed if the first stage accomplishes the DC/DC conversion while the DC/AC is accomplished by the second stage. In Figure 2.6 (b), another option of multi-stage inverter is considered. Here, DC/AC inversion with high frequency output is done first then it is applied to a cyclone inverter (frequency changer) that gives an output compatible with the grid frequency. Based on the used inverter topology (single-stage or multi-stage topology) different power decoupling techniques are employed. These techniques can be categorized into the following main categories: I- Power decoupling at PV-side, II- Two stages DC-Link power decoupling, III- High-frequency power decoupling port, and IV- Power decoupling at the AC-side. The key point in all these techniques is to modify the inverter topology in a way that allows us to use small capacitance.

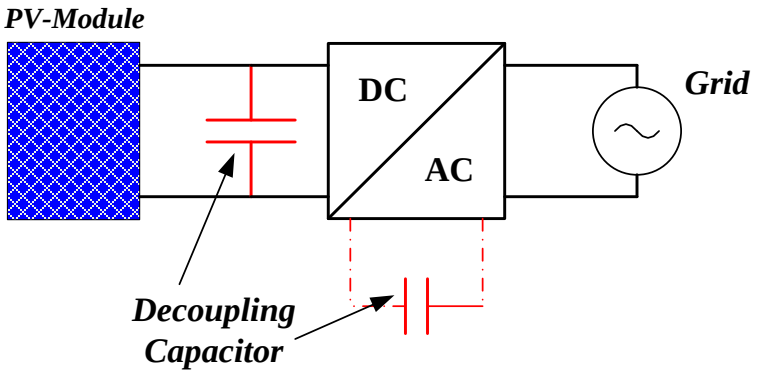

Figure 2.5: Single-Stage Inverter Decoupling Options.

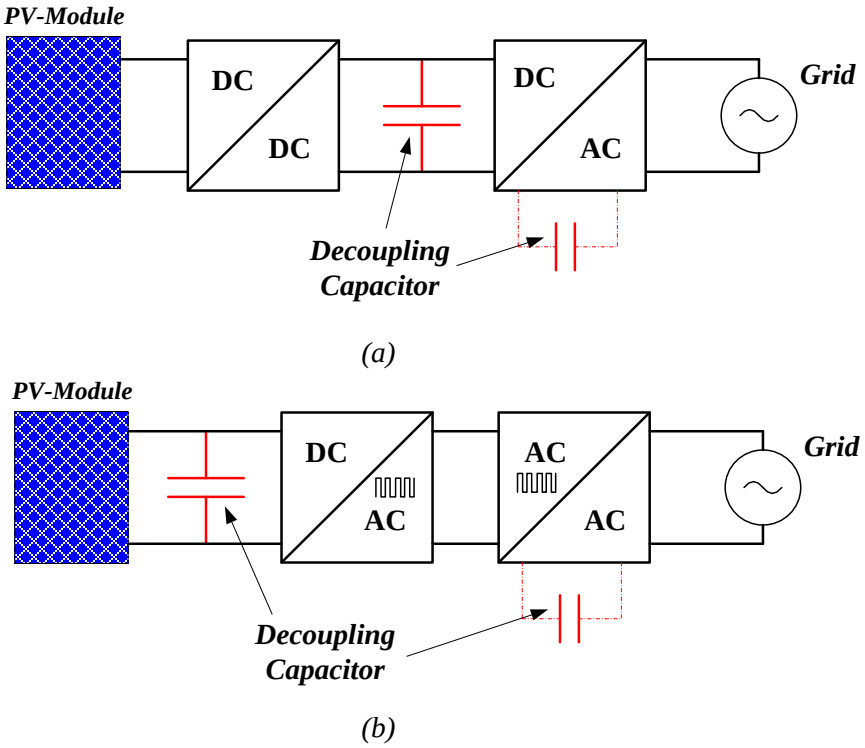

Figure 2.6: Multi-Stage Inverter Decoupling Options.

2.3.1 Power Decoupling at PV-side

The first approach to handle the double-frequency power ripple is based on modifying the input stage of the inverter. This modification allows the decoupling capacitor to have a DC-voltage level and voltage ripple across its terminals which is high enough to use a film capacitor instead of electrolytic one.

The modification can be performed by adding an auxiliary (extra) circuit between the PV panel and the DC-AC inverter; which contains the decoupling capacitor; or by embedding the decoupling capacitor within the inverter circuit at the input side (PV-side). Next, three topologies employing power decoupling at PV side will be presented.

2.3.1.1 Current Pulsation Smoothing Parallel Active Filter (Kyritsis, et al.):

The power decoupling capacitor is connected to the PV panel through a buck-boost converter between the PV panel and the Inverter as shown in Figure 2.7 [16]. The power decoupling circuit can be controlled independently.

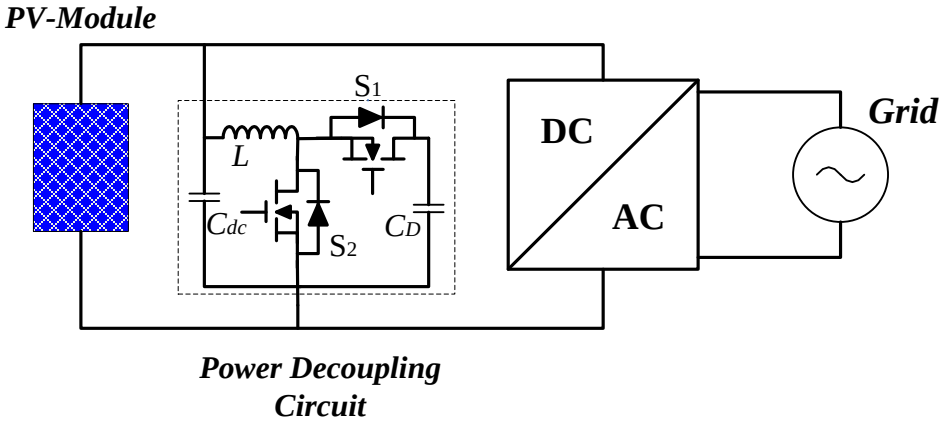

Figure 2.7: CPS-PAF topology proposed by Kyritsis, et al. [16].

The operation of this added circuit depends on the input and output power levels. Whenever the output power is less than the input power, the circuit will work in the boosting mode and charging the decoupling capacitor (C_D). In the other mode (output power greater than the input power), the circuit will behave as a buck converter and the decoupling capacitor will be discharged. 100µF film capacitor is used by setting a DC voltage level 68V and voltage ripple of 35V. Current hysteresis control is employed to control the current and make it following a certain function. Although, in [16] no specific number about the efficiency is mentioned, the power losses associated with the decoupling circuit will reduce the overall efficiency. Moreover, using a smaller decoupling capacitor leads to have higher stresses on the power devices, which means more power losses and lower efficiency.

Flyback Type Topology:

Flyback topology shows high efficiency with the capability of voltage amplification and electrical isolation. For this reasons, the next two topologies are based on the flyback converter. The primary side of the flyback is modified in a way that allows the accommodation of the power decoupling capacitor away from the PV panel.

2.3.1.2 Flyback-Type Single-Phase Utility Interactive Inverter with Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System (Shimizu, et al.):

Figure 2.8 shows the topology which was proposed in [17], in which a 40μF film capacitor was used as a decoupling capacitor for 100Watts micro-inverter design. The operation of this topology is divided into four modes. First, by closing S_1 the magnetizing inductor is charged from the PV panel. This lasts until the inductor current reaches the desired peak value I_{Lp}, then S_1 is turned off. At this point, the second mode starts and the inductor current will be charging the decoupling capacitor C_D through the build-in diode of S_2. Then, the capacitor's current will change its direction and the magnetizing inductance will be charged from the decoupling capacitor again during this mode. This mode is controlled by the output voltage, where the peak value of the magnetizing current in this mode depends on the rectified version of the output voltage. In the third mode, the power is transferred to the output side (to the grid). Both, $S_1$and S_2 are open and one of the AC switches (either S_3 or S_4 depending on the grid voltage) is turned on. Finally, in the fourth mode no current flows through the circuit, and the transformer is initialized.

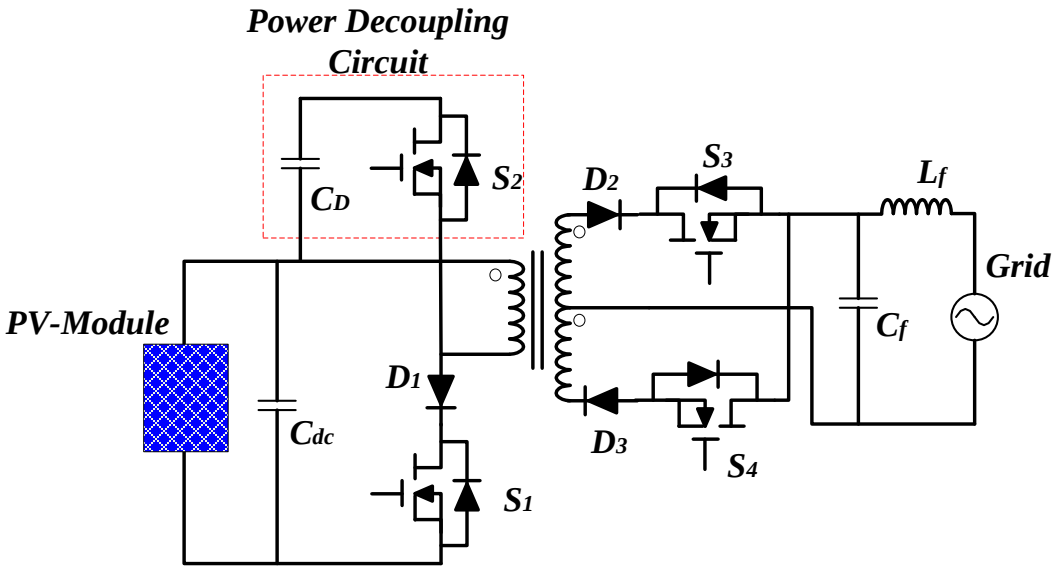

Figure 2.8: Topology proposed by Shimizu, et al. [17].

The decoupling capacitor is embedded to the circuit via S_2. This capacitor is responsible on handling the power ripple at the input side. Peak current control scheme is used to generate the driving signals of the switches.

2.3.1.3 Design Optimization of a Single-Phase Inverter for Photovoltaic Applications (Kjaer, et al.):

A modified version of the previous topology was proposed in [18], Figure 2.9. The operation of this topology is quite similar to the previous one. First, the magnetizing inductance is charged from the PV panel through S_{BB} and the body diode of S_{sync}. Once the magnetizing current reaches the desired peak value, S_{BB} is turned off. The decoupling capacitor (intermediate capacitor) will be charged from the transformer through the body diodes of the flyback switches (S_1 and S_2); which are turned on before the magnetizing current reaches the zero value.

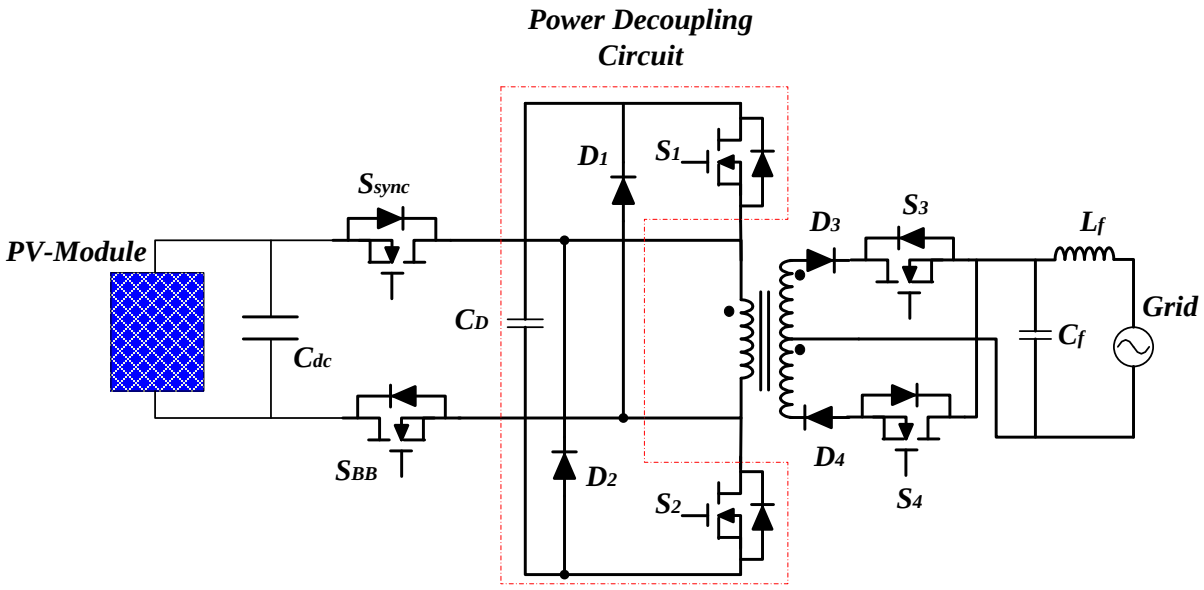

Figure 2.9: Modified topology proposed by Kjaer, et al. Note: the polarity of the PV panel is reversed in this topology [18]

In the third mode, the transformer will be charged again from the decoupling capacitor with the amount of energy that is required to be transferred to the secondary side during the next mode. In the last mode all the switches are open and the circuit is initialized for the next cycle.

The flyback diodes (D_1 and D_2) are providing path for the leakage energy generated in the transformer to be stored in the decoupling capacitor when flyback switches are turned off and the power is transferred into the secondary side. In the previous topology [17], there is no way for this leakage energy when S is turned off and it results in a spike across its terminals. This leakage energy is handled by an additional circuit. Usually, a dissipative RCD, LCDD clamp, or an active SC clamp circuit is used [2]. This way of handling the transformer leakage energy will reduce to some extent the losses and cost associated with the auxiliary circuits.

The decoupling capacitor versus the efficiency:

Using small film capacitor needs high DC voltage level and high voltage ripple. Hence, the stress on the power components (MOSFETs and Diodes) will be high, which leads to use semiconductor devices with relatively high power losses. Thus, the semiconductor technology is the key point to improve the efficiency of this kind of topologies. The experimental results in [17] show 70% maximum efficiency although the authors expect a higher efficiency if a power switching devices with a high performance and low power loss are used. On the other hand, the calculated results in [18] show 66% maximum efficiency but the authors expected an improvement on the efficiency if an enhanced gate circuit and semiconductor devices are used from 66% to 87%.

2.3.2 Multi-stages DC-Link power decoupling

For a multi-stage micro-inverter design, the main power decoupling capacitor is placed at the high voltage DC link as shown in Figure 2.6 (a). Unlike PV side decoupling, where PV nominal voltage is fixed and the voltage ripple should be limited to a very small range to maximize the energy harvest from the PV panel, DC link decoupling allows for a higher DC link voltage as well as a higher voltage ripple, with the constraint that the lowest DC link voltage should be greater than the peak grid voltage. Figure 2.10 shows the waveforms of the voltage across the decoupling capacitor and the output AC voltage. In order to have modulation index less than one ($m \leq 1$), the following condition must be satisfied.

$$V_{C\_min} \geq V_{ac\_P}$$

But, the minimum capacitor's voltage is given by (2.10).

$$V_{C\_min} = V_{DC} - \frac{\Delta V}{2} \tag{2.10}$$

Where:

V_{DC} : is the DC link voltage across the decoupling capacitor and

ΔV : is the voltage ripple across it.

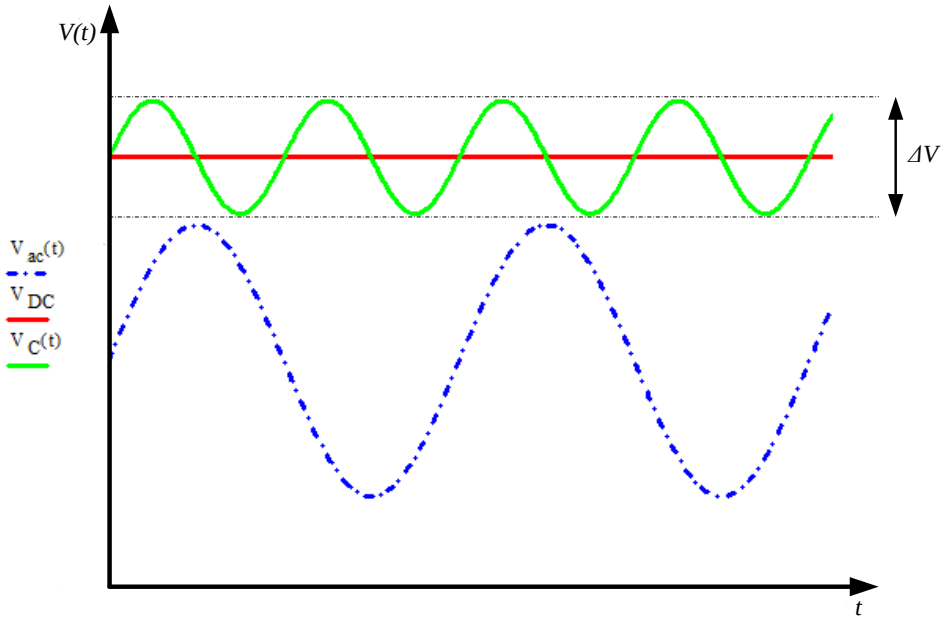

Figure 2.10: Output voltage and capacitor voltage waveforms.

From (2.10), the voltage ripple is given by (2.11)

$$\Delta V = 2\left(V_{DC} - V_{C\_min}\right) \tag{2.11}$$

This is also equal to

$$\Delta V = rV_{DC} \tag{2.12}$$

From (2.11) and (2.12), we get:

$$r = 2\left(1 - \frac{V_{C\_min}}{V_{DC}}\right) \tag{2.13}$$

The maximum value is when $V_{C\_min} = V_{ac\_P}$, then (2.13) becomes as follows:

$$r = 2\left(1 - \frac{V_{ac\_P}}{V_{DC}}\right) \tag{2.14}$$

Substituting (r) in (2.9), the minimum decoupling capacitor will be equal to:

$$C_{min} = \frac{P_{in}}{\omega_o r_{max} V_{DC}^2} = \frac{P_{in}}{2\omega_o V_{DC}(V_{DC} - V_{ac\_P})} \tag{2.15}$$

The minimum required decoupling capacitance can be calculated according to (2.15). For a 200W, 110Vac micro-inverter design, the relationship between the minimal capacitance(C_{min}), the DC voltage(V_{DC}), and peak-peak voltage ripple (r) is depicted in Figure 2.11.

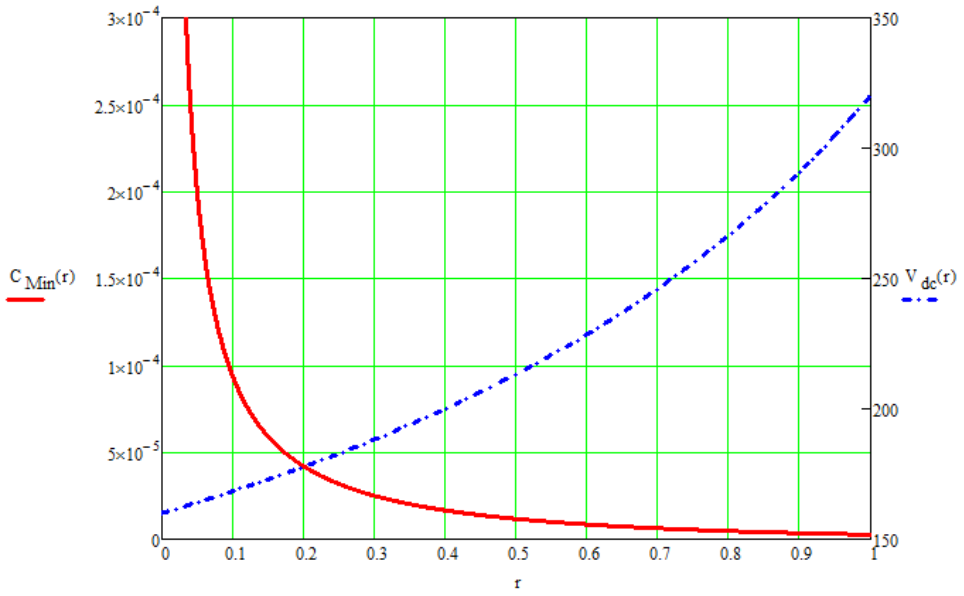

Figure 2.11: The relationship between the minimum decoupling capacitance, the DC voltage level, and the voltage ripple.

Figure 2.11 shows that the DC voltage level increases as the value of the ripple is increases. This leads to increase the voltage stress on the semiconductor devices, which means a higher losses and cost.

A large voltage ripple at the DC link results in deterioration of the output current waveform. *Enjeti* [19] proposed a modified modulation strategy to reject the DC-link voltage ripple in the control system as illustrated in Figure 2.12. *Brekken* [20] proposed a control technique, Figure 2.13, which allows for 25% ripple voltage without distorting the output current waveform. The voltage loop cutoff frequency was designed at 10Hz, greatly attenuating the double line frequency DC voltage ripple in the control loop. However, the low cutoff frequency in the proposed control system definitely degrades the system dynamic performance.

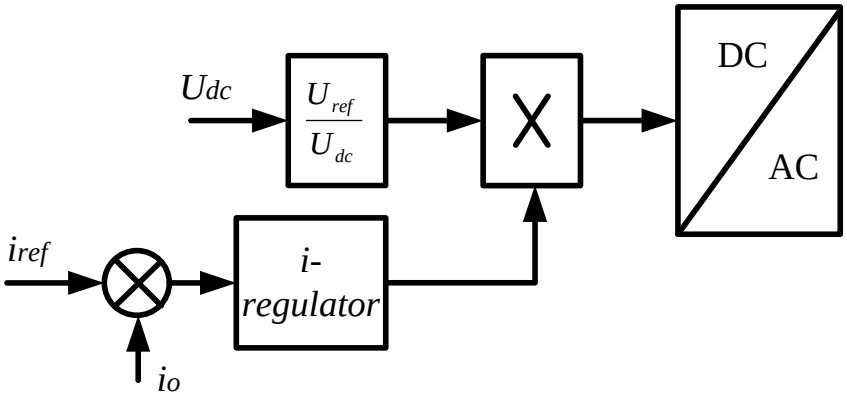

Figure 2.12: Modulation technique proposed by Enjeti [19]

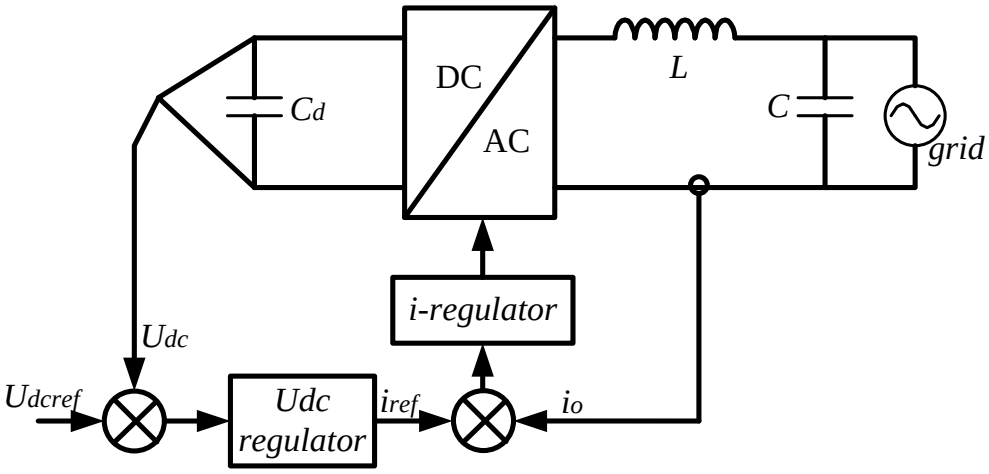

Figure 2.13: Control proposed by Brekken [20]

To overcome this limitation, *Ninad* [21] proposed a DC voltage ripple estimation control strategy to enable wide bandwidth design of the voltage loop. As shown in Figure 2.14, in which no DC voltage ripple is fed to the DC voltage regulator by subtracting DC voltage from the estimated voltage ripple. In this manner, the DC voltage regulator can achieve a faster transient response. Many works have been done in this area [22 - 28]

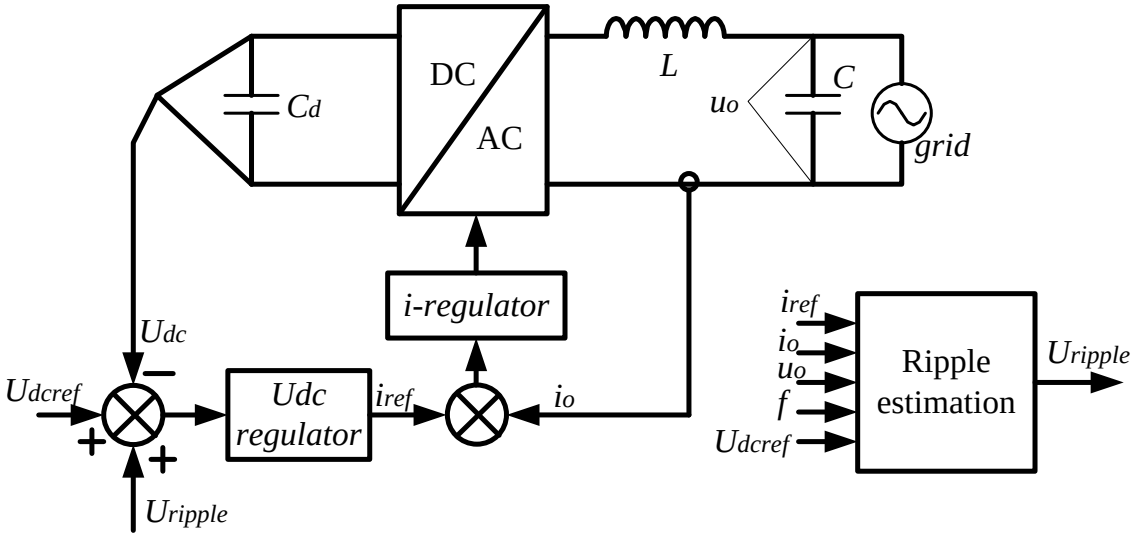

Figure 2.14: voltage ripple estimation strategy for large DC ripple proposed by Nayeem A. Ninad [21]

2.3.3 High-Frequency Power Decoupling Port (Krein, et al.):

The decoupling in [29], Figure 2.12, is different in the way of connecting the decoupling circuit. A third port is added at high-frequency AC link to connect the decoupling circuit with the inverter. The added port has no impact on the DC link voltage and current. So, the DC level and the voltage ripple across the decoupling capacitor can be set by the designer in order to achieve the minimum capacitance without any constraints from the DC link. For 100W design a 3.3µF film capacitor is used at 400*V* in [29].

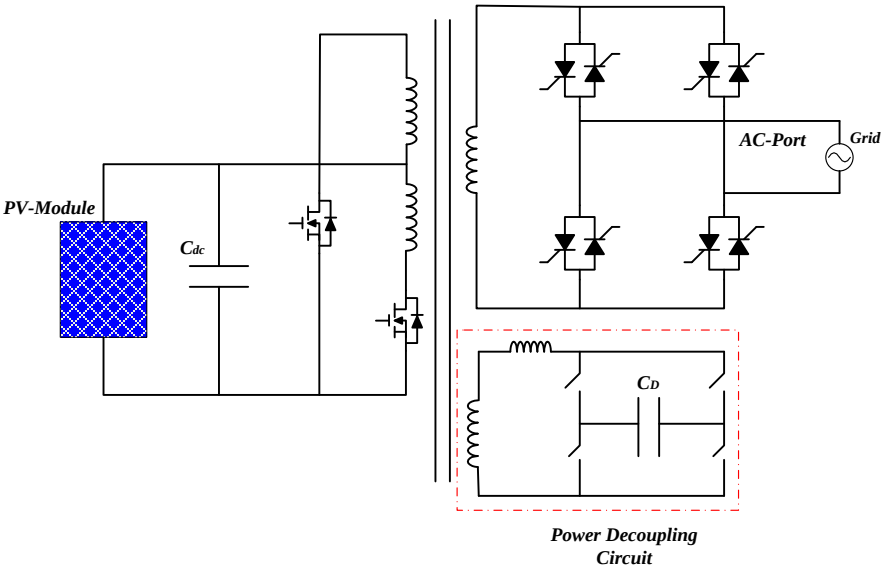

Figure 2.15: Topology proposed by krein, et al. [29].

2.3.4 Power Decoupling at AC-side

In AC side decoupling circuit, the decoupling capacitor is usually embedded in the inverter stage itself, where the voltage across the capacitor terminals is controlled. Because of the high voltage swing at the AC side, the capacitor value can be small and a non-polarized (film) capacitor can be used. In topologies that employ this kind of decoupling, bi-directional switches are required to provide a path for the positive and negative currents. The possible integration of the bi-directional switch and its driver circuit will simplify these topologies and enhance the overall system reliability.

Embedding the decoupling capacitor into the inverter that used in [30] [31] was done by adding a third phase leg to the H-bridge inverter. This phase-leg is connected to the grid through the decoupling capacitor and its voltage and the current are controlled in a way that makes the instantaneous power transferring across the inverter constant.

2.3.4.1 A hard switched high frequency link converter with constant power output for photovoltaic (PV) applications (Li, et al.):

The topology shown in Figure 2.16 [30] is based on the half bridge dual converter as an input stage; which boosts the low input voltage into a higher level compatible with the grid voltage. The input stage consists of two MOSFETs, two inductors, two diodes, and a transformer. These input inductors are sized at the switching frequency (f_s) since the decoupling capacitor will take care of the double-frequency power ripple. The diodes are connected in series with the MOSFETs (Q_1 and Q_2) to block the negative voltage reflected from the output side. The inversion stage consists of three bidirectional switches and three small capacitors. These capacitors supporting the high frequency ripple. The decoupling capacitor (C_b) is embedded in the circuit through the secondary bidirectional switch Q_3. No experimental results are given in [30], but a 5.53μF decoupling capacitor is used in the simulation.

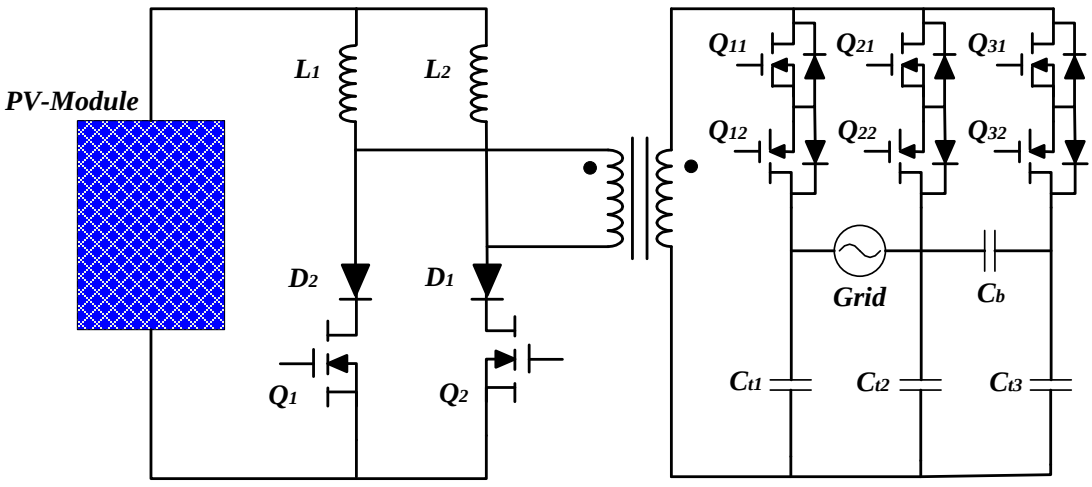

Figure 2.16: Topology proposed by Li, et al. [30].

2.3.4.2 A Single-Phase Current Source Solar Inverter with Reduced-Size DC Link (Bush, et al.):

A current source inverter topology employs an AC decoupling technique proposed by Bush [31] is shown in Figure 2.17. Again, it can be seen as a three phase bridge where the added phase leg (phase-leg b) is dedicated for accommodating the decoupling capacitor (C_b). It consists of six bidirectional switches. In [31], an IGBT with a diode in series are used to implement the bidirectional switch. It is worth mentioning that this topology needs a pre-boosting stage in order to be used in AC-Module PV system, thus additional components, cost, control, and losses.

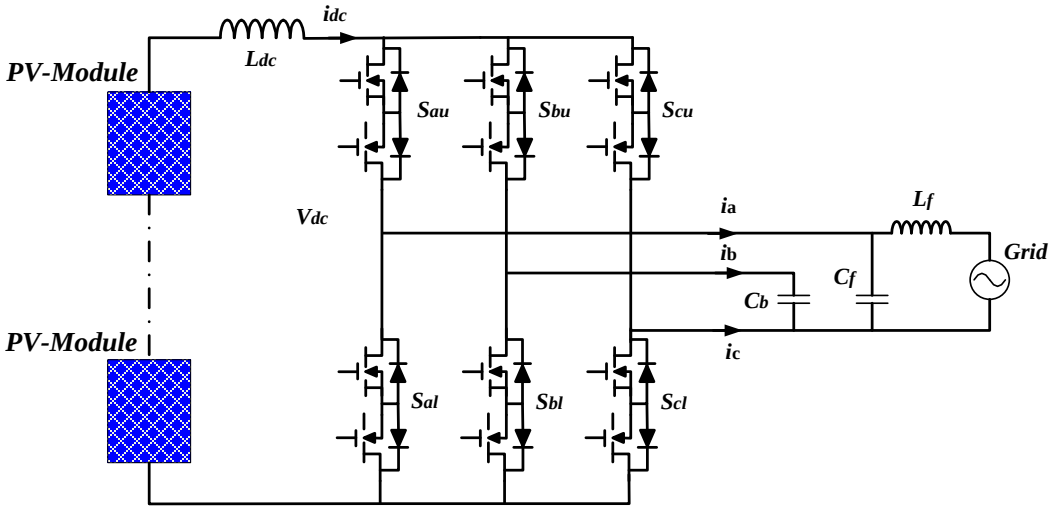

Figure 2.17: Topology Proposed by Bush, et al. [31].

Both topologies, which employ AC power decoupling, are based on the current source inverter (CSI) implementation. In current source inverter, the switches action must be controlled such that there is always a path for the dc-link current (i_{dc}) and preventing the short circuit of the AC side. Therefore, one and only one switch from the upper and lower switches can be closed at the same time. The detailed derivation can be found on [31].

2.4 Power Decoupling Circuit's Performance Comparison:

The power decoupling techniques presented above will impact the overall system reliability, cost, and efficiency. The power process in the grid-connected PV system is shown in Figure 2. 18. Assuming the power from the PV panel is P_{PV}, the efficiency of the inverter without the decoupling circuit is η_o, and the efficiency of the decoupling circuit is η_d.

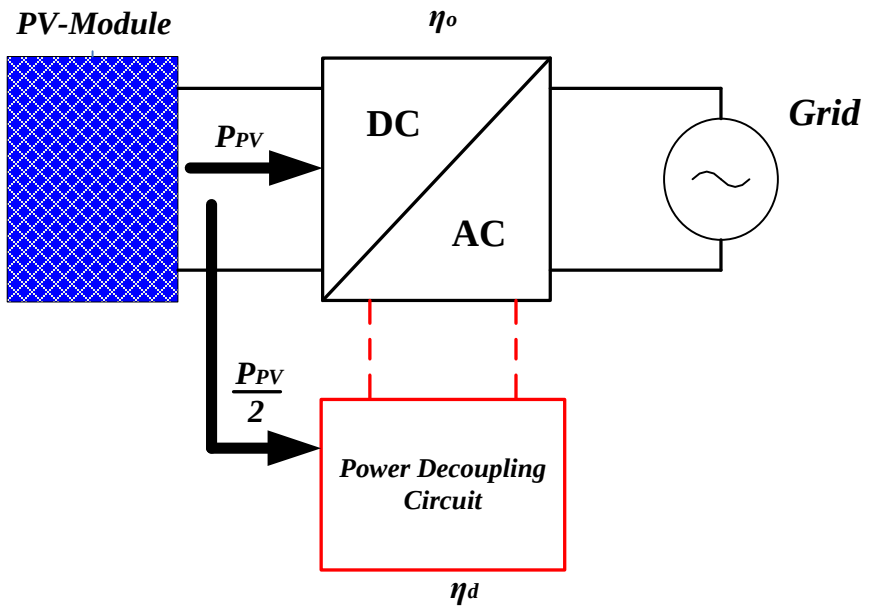

Figure 2.18: The Power Process in the PV system.

The main inversion stage is processing the whole power from the PV panel while half of that power is processed by the decoupling circuit as shown in Figure 2.18. Then, the power losses in both circuit is given as follows:

$$L_{inv} = (1 - \eta_o)P_{PV}$$

$$L_D = (1 - \eta_d)\frac{P_{PV}}{2}$$

And the total power losses are:

$$L_T = L_{inv} + L_D$$

$$L_T = (1-\eta_o)P_{PV} + (1-\eta_d)\frac{P_{PV}}{2}$$

Finally, the efficiency of the whole system is given by (2.16):

$$\eta_T = 1 - \frac{(1-\eta_o)P_{PV} + (1-\eta_d)\frac{P_{PV}}{2}}{P_{PV}}$$

$$\eta_T = \eta_o - \frac{(1-\eta_d)}{2} \tag{2.16}$$

Table 2.1 shows the comparison results of the various decoupling techniques with respect to the size of decoupling capacitor, the added cost, the efficiency impact, and decoupling control circuit complexity.

Table 2.1: Performance Comparison of the Various Power Decoupling Techniques.

Decoupling techniques		***Power rating(W)***	***decoupling capacitor***	***Additional Cost***	***Efficiency***	***Control Complexity***
Decoupling at PV side	Fig.2.1	200	7.6mF	capacitor	η_o	No added control
	Fig.2.7	70	100µF	Capacitor+2 switches+1 inductor	$\eta_o - \frac{(1-\eta_d)}{2}$	Active filter control
	Fig.2.8	100	40µF	Capacitor+1 switch +1diode	$\eta_o - 2(1-\eta_d)$	Peak current control
	Fig.2.9	156	314µF	Capacitor+3 switches+2 diodes	$\eta_o - 2(1-\eta_d)$	Peak current control
Decoupling at DC- link	Fig.2.12			capacitor	η_o	DC voltage Feed-forward control
	Fig.2.13	200	15µF	capacitor	η_o	Low voltage loop bandwidth
	Fig.2.14	100	500µF	capacitor	η_o	Voltage ripple estimation
High-Frequency Decoupling	Fig.2.15	100	3.3 µF	Capacitor+4 switches+1transforme r winding		
Decoupling at AC side	Fig.2.16	100	5.53µF	Capacitor+2 switches	$\eta_o - \frac{(1-\eta_d)}{2}$	Three-phase current modulation
	Fig.2.17	-	-	Capacitor+2 switches	$\eta_o - \frac{(1-\eta_d)}{2}$	Modified three-phase current modulation

3 CHAPTER THREE: THREE-PORT MICRO-INVERTER WITH POWER DECOUPLING CAPABILITY FOR PV SYSTEMS APPLICATIONS

3.1 The Proposed Three-Port topology

The proposed three-port-topology based on the flyback type topology. Adding one switch and two diodes to the input side will allow us to move the decoupling capacitor from being in parallel with the PV panel. Where there are no constraints on the DC voltage and voltage ripple on the capacitor's terminals. The decoupling capacitor will act as a load during mode I and as a source during mode II.

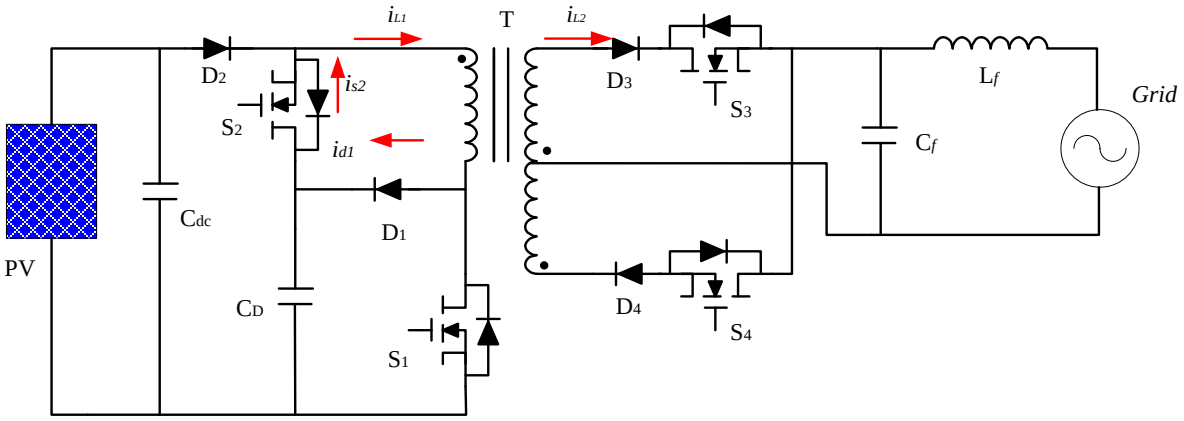

Figure 3.1: The Proposed Three-Port Topology.

3.2 Operation Modes

The operation of the circuit is divided into two main modes, Figure 3.2. Mode I: *charging mode* and Mode II: *discharging mode*. In mode I, the decoupling capacitor will be charged form the input (PV panel) through the magnetizing inductance. The amount of the stored energy is determined by how much energy is needed to be transferred into the output side. In the second

mode, this stored energy will support the PV panel to deliver the demanded power into the output side (the grid).

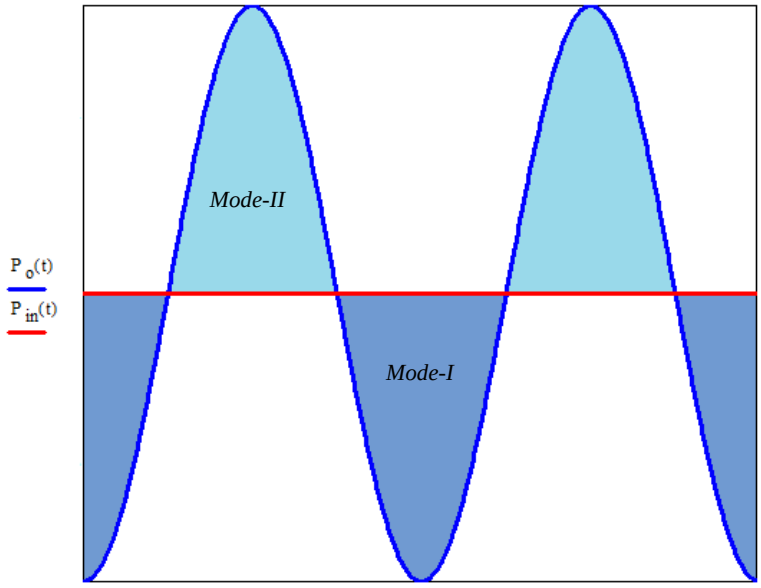

Figure 3.2: Input and Output Power Waveforms.

3.2.1 Mode-I

When the input power is greater than the output power, the circuit will operate in mode-I. The dark blue areas represent the amount of energy that will be stored in the decoupling capacitor (C_D) during this mode; it will act as a load. The operation of this mode is divided into three sub-modes. First, the magnetizing inductance is storing energy from the PV panel. Then, a certain amount of this energy is stored in the decoupling capacitor. Finally, the remaining portion; which is required from the output, is transferred into output side. Figure 3.3 illustrates the operation of the circuit during both modes. It shows the corresponding waveforms of the magnetizing current, the input and secondary side current waveforms, and the switches' driving signal for one switching cycle in each mode.

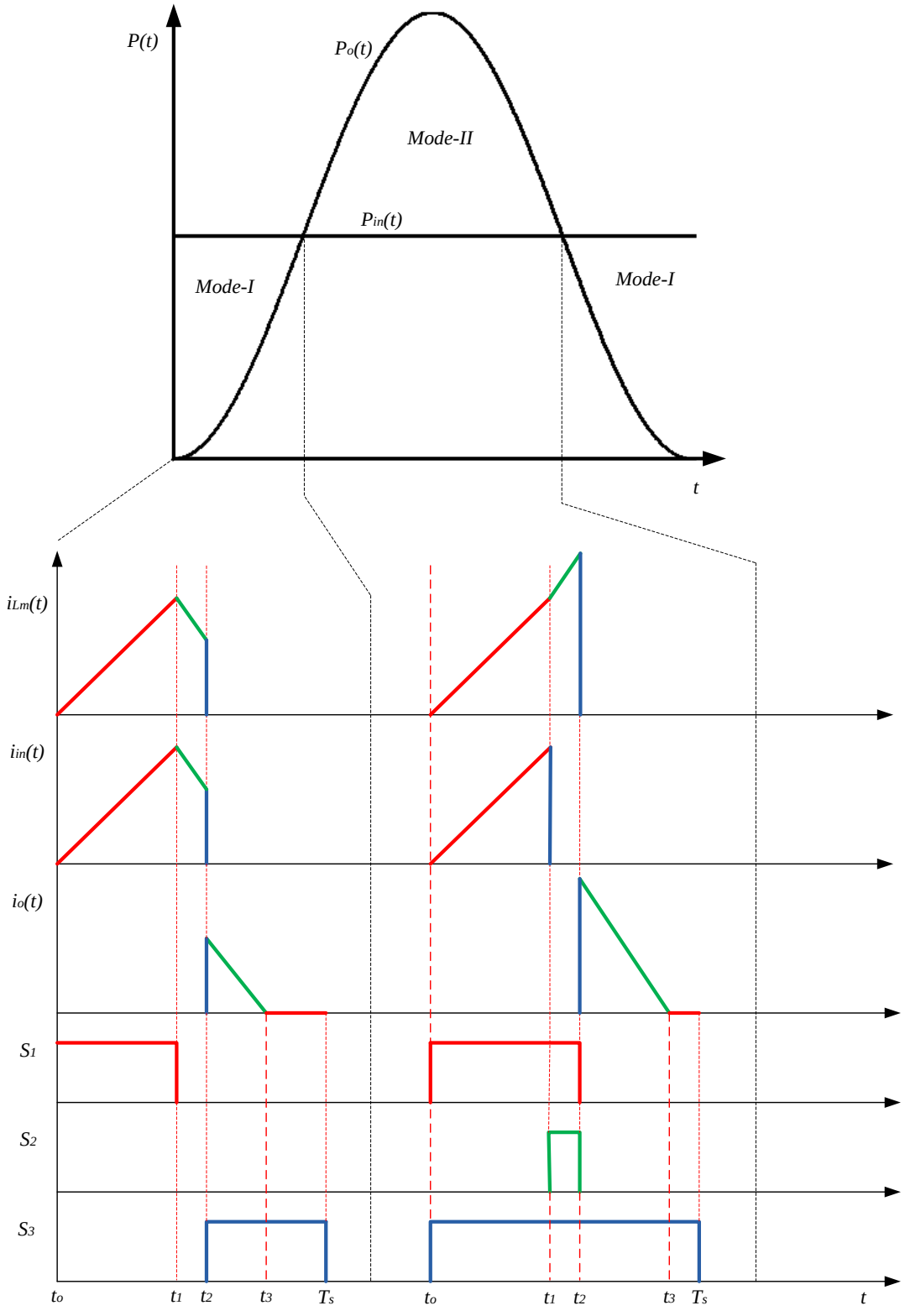

Figure 3.3: Inductor current, Input current, output current waveforms, S_1, S_2, S_3 gate signals for the two main operation modes.

The operation starts with sub-mode-1. S_1 is turned on and all other switches are kept off, Figure 3.4 (a). The PV panel is charging the magnetizing inductance. The magnetizing current is given by (3.1).

$$\boldsymbol{i_{L_m}(t) = \frac{V_{in}}{L_m} t} \tag{3.1}$$

At $t = t_1 = D_1 T_s$, the inductor current reaches its peak value, I_{LP}, which is given by (3.2). At this point, sub-mode-1 ends.

$$I_{L_P} = \frac{V_{in}}{L_m} D_1 T_s \tag{3.2}$$

This peak value varies with time in order to keep the input power constant. The detailed derivation will be derived later. Once S_1 is turned off sub-mode-2 starts, where all switches are off, Figure 3.3 (b). The magnetizing inductance starts charging the decoupling capacitor, C_D, from t_1 to t_2. The voltage across the magnetizing inductance is given by (3.3).

$$L_m \frac{di_{Lm}(t)}{dt} = V_{in} - V_{C_D} \tag{3.3}$$

And the magnetizing current is:

$$i_{Lm}(t) = \frac{V_{in} - V_{C_D}}{L_m}(t - t_1) + I_{L_P} \tag{3.4}$$

The magnetizing current will keep discharging until it reaches the reflected value of the secondary current at time (t_2), which will be derived later. At this point sub-mode-3 starts by turning on one of the secondary side switches (AC-side switches) depending on the polarity of the output voltage (grid voltage), Figure 3.3 (c).

$$i_{L_m}(t_2) - I_{L_P} = \frac{V_{in} - V_{C_D}}{L_m}(t_2 - t_1) = \frac{V_{in} - V_{C_D}}{L_m} D_2 T_s \tag{3.5}$$

The voltage across the secondary side of the transformer (across L_2) is given by (3.6).

$$V_{L_2} = L_2 \frac{di_{L_2}(t)}{dt} = -V_o sin(\omega_o t) \tag{3.6}$$

Integrating both sides we get the current flows during the sub-mode-3 through the secondary inductance.

$$i_{L_2}(t) = \frac{-V_o sin(\omega_o t)}{L_2}(t - t_2) + i_{L_2}(t_2) \tag{3.7}$$

Providing that the circuit is aimed to operate in DCM mode, the inductor current must be discharged to zero before the next switching cycle starts. So, the current at t = t_3 is zero and its value at t = t_2 is given by (3.8).

$$i_{L_2}(t_2) = \frac{V_o sin(\omega_o t)}{L_2}(t_3 - t_2) = \frac{V_o sin(\omega_o t)}{L_2} D_3 T_s \tag{3.8}$$

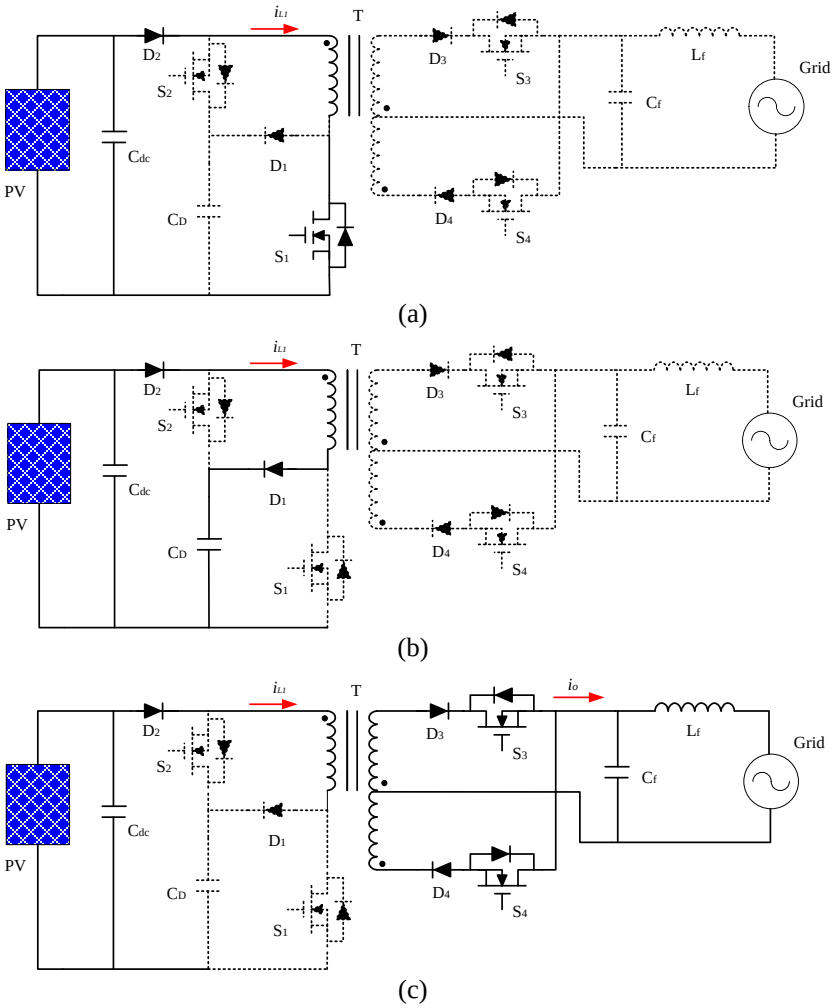

Figure 3.4: Operation Sub-modes during Mode I

(*Note: $V_o sin(\omega_o t)$ can be considered as a constant value giving a very small switching cycle compared to the output AC cycle*).

The average value of the output current is given by (3.9) as follows:

$$i_{o_{av}}(t) = \frac{1}{2}\frac{(t_3 - t_2) i_{L_2}(t)}{T_s} = I_o sin(\omega_o t) \tag{3.9}$$

Using (3.8) and (3.9), as it is shown below, the result is $i_{L_2}(t)$ in (3.10)

$$i_{L_2}(t) = \frac{2I_o sin(\omega_o t) T_s}{(t_3 - t_2)} = \frac{2I_o sin(\omega_o t) T_s}{D_3 T_s}$$

$$D_3 T_s = \sqrt{\frac{2I_o L_2 T_s}{V_o}}$$

Then

$$i_{L_2}(t_2) = \left(\sqrt{\frac{2I_o T_s}{V_o L_2}}\right) V_o sin(\omega_o t) \tag{3.10}$$

Its reflection into the primary side gives us the magnetizing current during that sub-mode.

$$i_{L_m}(t_2) = \left(\frac{n_2}{n_1}\right)\left(\sqrt{\frac{2I_o T_s}{V_o L_2}}\right) V_o sin(\omega_o t) \tag{3.11}$$

Equation (3.11) shows that the value of the magnetizing current at t = t_2 is following the output voltage.

Now, after we derived the expressions of the magnetizing current during all sub-modes of mode I, we can derive the I_{L_P} formula. The key point is to keep the input power constant. Since we know the value of $i_{L_m}(t_2)$, we can derive I_{L_P} using the power law as it is shown in (3.12).

$$P_{in} = \frac{\frac{1}{2} I_{L_P} D_1 T_s V_{in} + \frac{1}{2}\left(I_{L_P} + i_{L_m}(t_2)\right) D_2 T_s V_{in}}{T_s} \tag{3.12}$$

From (3.2) and (3.5) we find the following:

$$D_1 T_s = \frac{L_m I_{L_P}}{V_{in}} \tag{3.13}$$

$$D_2 T_s = \frac{L_m \left(i_{L_m}(t_2) - I_{L_P}\right)}{V_{in} - V_{C_D}} \tag{3.14}$$

Substitute (3.13) and (3.14) in (3.12), I_{L_P} is given by (3.15)

$$I_{L_P} = \sqrt{\left(\frac{V_{in}}{V_{C_D}}\left(i_{L_m}(t_2)\right)^2 - \left(\frac{2P_{in}T_s}{L_m}\right)\left(\frac{V_{in}}{V_{C_D}} - 1\right)\right)} \tag{3.15}$$

3.2.2 Mode-II:

This mode operates when the output power is greater than the input power (supplied power) as it is shown in Figure 3.2. Here, the stored energy in the decoupling capacitor will subsidize the input source (PV panel) by providing the extra demanded power to the output. The decoupling capacitor will act as a secondary source during this mode. The operation of this mode also is divided into three sub-modes. (1) storing energy into the transformer's magnetizing inductance from the PV panel, (2) continue storing energy from the decoupling capacitor, and (3) transferring the power to the output side. These modes are illustrated in Figure 3.3.

Sub-mode-1 starts by closing S_1 while keeping S_2 off, Figure 3.5 (a). It is worth to mention that one of the AC side switches will be on always during mode-II as it is shown in Figure 3.3. Then, the magnetizing current is charged from the PV panel. It will keep charging until it reaches the peak value, I_{L_P} which is given by (3.16).

$$I_{L_P} = \sqrt{\frac{2P_{in}T_s}{L_m}} \tag{3.16}$$

Then, sub-mode-2 starts by turning on S_2 while keeping S_1 closed Figure -5 (b). D_1 and D_2 block any current from flowing in opposite direction. Now, the magnetizing inductance is continuing charging from the decoupling capacitor until it reaches the peak value; which depends on the output voltage. The peak current value, $I_{L_{P2}}$, is given by (3.17).

$$I_{L_{P2}} = \left(\frac{n_2}{n_1}\right)\left(\sqrt{\frac{2I_o T_s}{V_o L_2}}\right) V_o sin(\omega_o t) \tag{3.17}$$

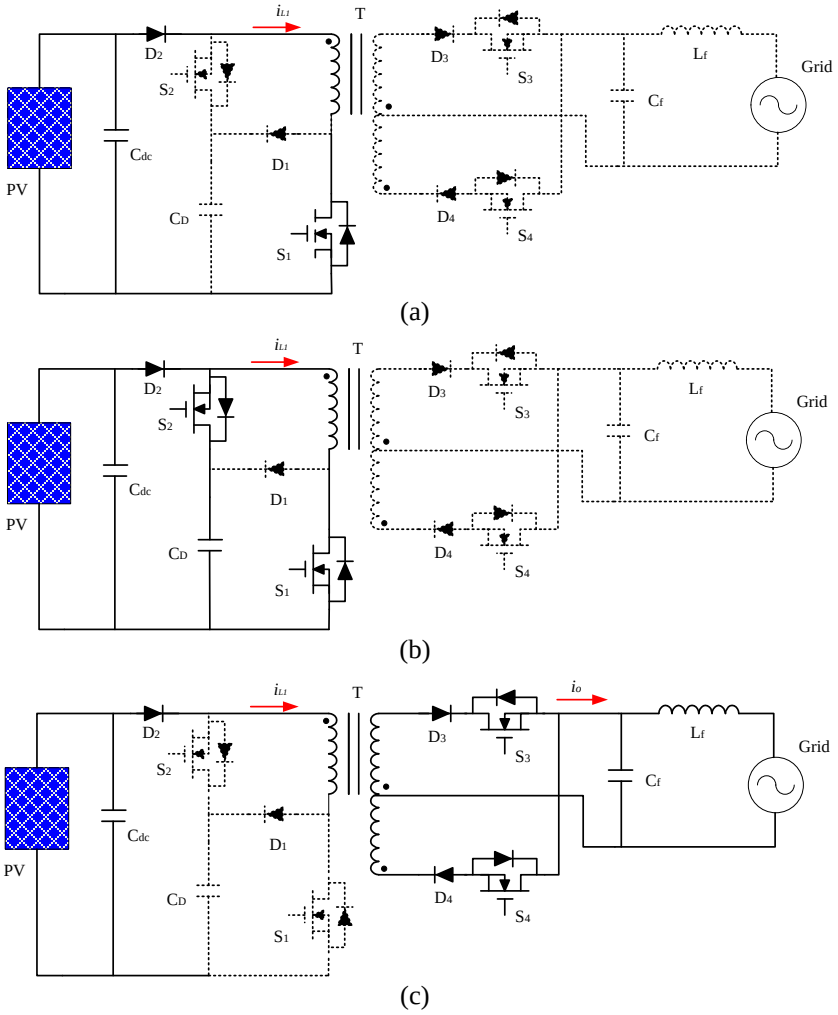

Figure 3.5: Operation Sub-modes during Mode II.

Finally, sub-mode-3 starts when both S_1 and S_2 are turned off, Figure -5 (c). An exact amount of energy will be transferred into the output through either S_3 or S_4 (depending on the output voltage polarity)

It can be noticed from the operation modes that the leakage energy is stored in the decoupling capacitor without using any additional circuit. This is one of the advantages of the proposed topology. In [17], this leakage energy will cause a spike on the decoupling switch (S_2 in Figure 2.8) at turn off time to transfer the energy into the AC side. The modified topology in

[18] solved this problem by storing the leakage energy in the decoupling capacitor through the flyback diodes (D_1 and D_2) in Figure 2.9. Three switches and two diodes are used to solve the leakage energy problem.

3.3 The Decoupling Capacitor Design

In chapter two we derived the formula for the decoupling capacitance, which is given in (2.9). During sub-mode-3 in both main modes, the energy that has been stored in the magnetizing inductance will be transferred into the secondary side. Wherefore, the voltage across the decoupling capacitor must be greater than the stress voltage across S_1, which is given in (3.18).

$$V_{S_1} = V_{in} + \frac{n_1}{n_2} V_o sin(2\omega_o t) \tag{3.18}$$

Then, equation (3.19) represents the condition that must be guaranteed during the circuit operation.

$$V_{C_D} \geq V_{in} + \frac{n_1}{n_2} V_o sin(2\omega_o t) \tag{3.19}$$

To be more accurate we will assume that the minimum voltage across the decoupling capacitor must be greater than the maximum stress voltage across S_1.

$$V_{C_D min} \geq V_{in} + \frac{n_1}{n_2} V_o \tag{3.20}$$

Use (3.20) and (2.8), we will get a relationship between the DC-level and the voltage ripple across the decoupling capacitor. By assuming a certain DC-level we can find the possible range of the voltage ripple as it is shown in (3.21)

$$\Delta V_{C_D} \leq 2\left(V_{C_D}(DC) - V_{in} - \frac{n_1}{n_2} V_o\right) \tag{3.21}$$

When we choose the DC-level voltage across the decoupling capacitor we should take in the consideration the stresses on the power devices at the input side (S_1, S_2, D_1, and D_2). We

will show later in this chapter that the stress voltages on the power devices is related to the decoupling capacitor voltage. Now, for a certain system parameters, we can design (choose) the appropriate value for the decoupling capacitor. Consider a 100W system with 35V as an input voltage and the grid voltage and frequency are $110V_{rms}$ and 60Hz, respectively. Let us choose a DC-level across the decoupling capacitor of 120V, and then the ripple should be less than 107V, assume it is 100V. Using eq. (3.9), 22.1µF is needed as a decoupling capacitance.

3.4 Simulation Results

PSIM software is use to simulate the proposed topology. Table 3.1 lists the components values that we used in the simulation.

Table 3.1: Proposed topology component values.

Input Power (P_{in})	100 W	Input Voltage (V_{in})	35 V
Magnetizing Inductance (L_m)	7µH	Turns Ration (N)	5
Decoupling Capacitance (C_D)	40µF	C_f	1µF
Output Resistor (R_o)	120Ω	L_f	1mH

Figure 3.6 shows the magnetizing inductance, input, and secondary currents waveforms for one complete grid cycle. It is clear how the input current is following the magnetizing current during mode I. while during mode II, it keeps at constant value, I_{L_P} in (3.16). The magnetizing current is following the output voltage waveform to transfer the required power into the output side (the grid). Figure 3.7 and Figure 3.8 show an expanded view of the circuit operation in mode-I and mode-II, respectively. The similarity between the simulation results and the analysis waveforms is very clear.

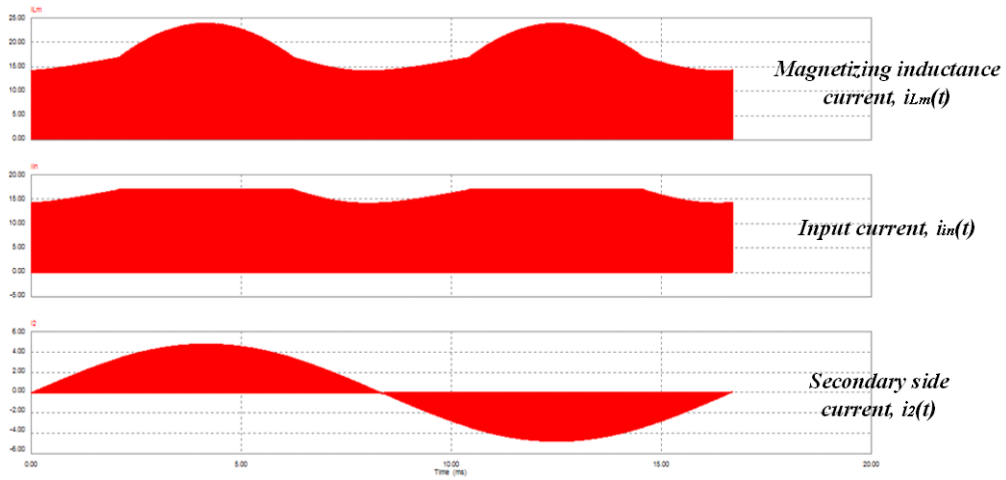

Figure 3.6: the magnetizing inductance, input, and secondary currents waveforms for one complete grid cycle.

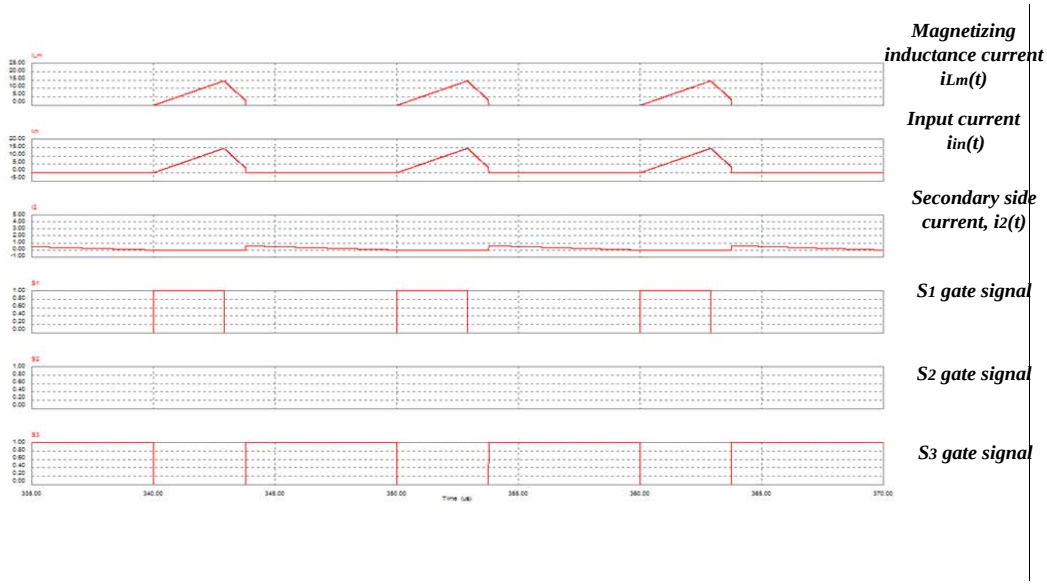

Figure 3.7: An expanded view of mode I.

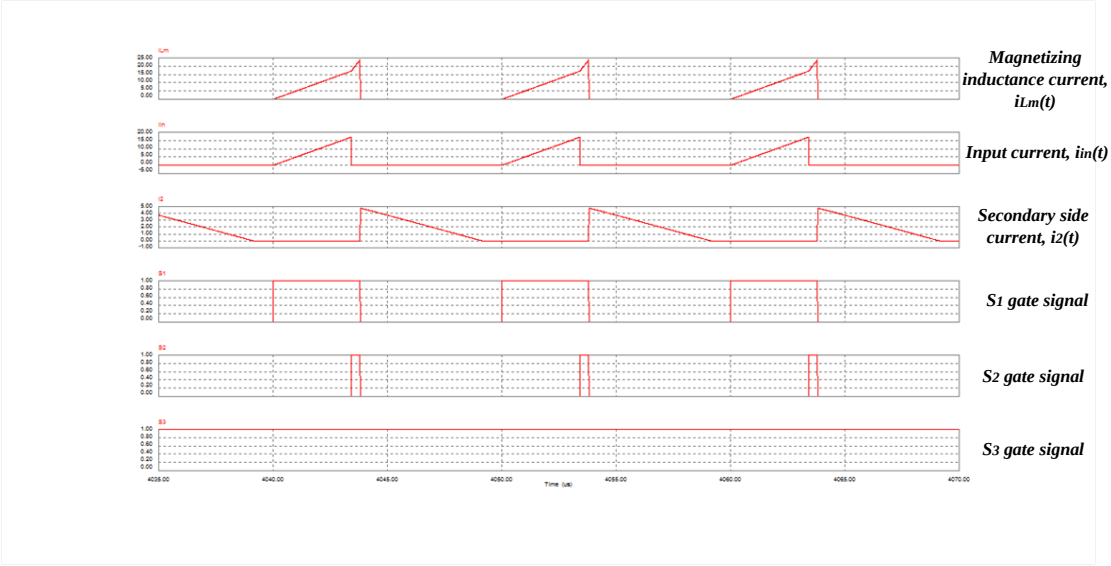

Figure 3.8: An expanded view of mode II.

On the AC side, Figure 3.9 shows the secondary inductor current, the output current, and the output voltage waveforms for one grid cycle. in Figure 3.10 shows the following starting from above, output current, output voltage, V_{C_D}, the stress voltage across S_1 and V_{C_D}, and finally the input and output power waveforms.

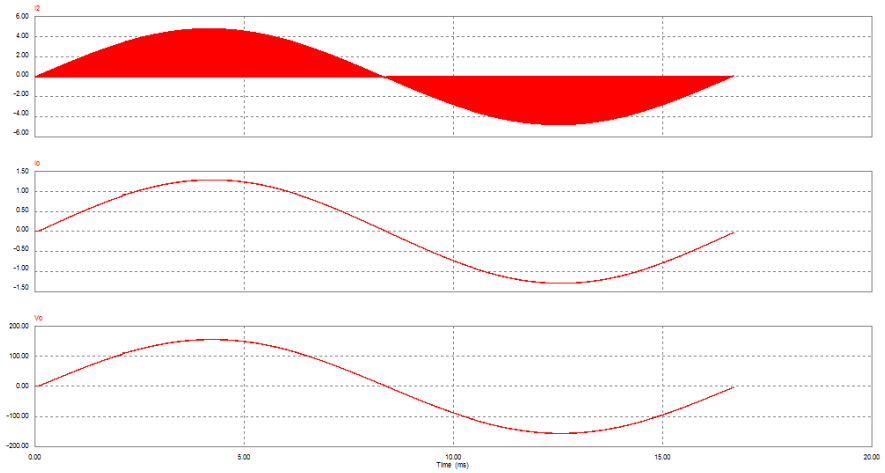

Figure 3.9: The secondary inductor current, the output current, and the output voltage waveforms.

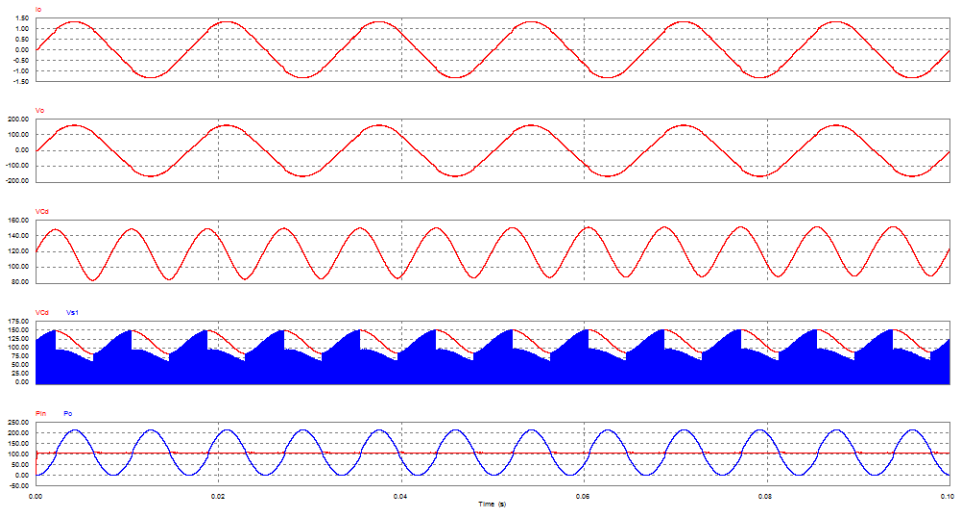

Figure 3.10: output current and voltage, V_{CD}, the stress voltage across S_1 and V_{CD}, and finally the input and output power waveforms.

3.5 Experimental Results

An open loop prototype was built and tested at fixed point to verify the operation modes of the proposed topology. We used the same values that have been used in simulation. Figure 3.11 and Figure 3.12 show the magnetizing inductance current and the switches' gating signal in mode-I and mode-II, respectively.

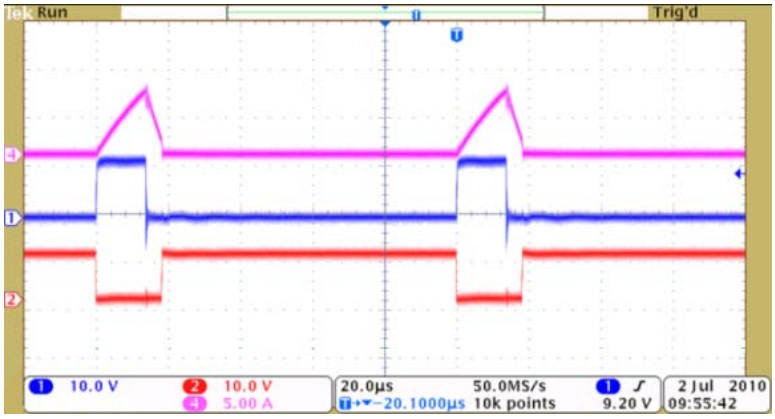

Figure 3.11: Magnetizing Current and the switches' gating signal in mode-I

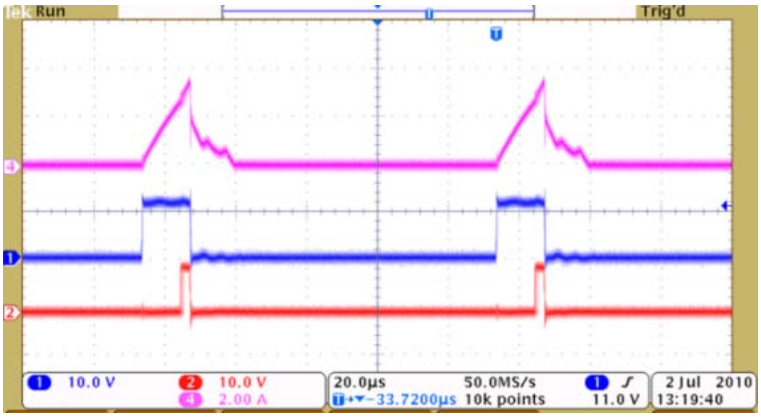

Figure 3.12: Magnetizing Current and the switches' gating signal in mode-II

4 CHAPTER FOUR: CONCLUSION AND FUTURE WORK

4.1 Conclusion

The power ripple problem in single-phase micro-inverter has been studied in this thesis. Different power decoupling techniques also have been presented and classified. A comparison table between these techniques was made.

A new three-port topology that employs power decoupling at PV side and its complete analysis for the operation of the proposed topology have been presented in chapter three. Finally, the simulation and experimental results have been shown.

The advantages of the proposed topology when compared to previous topologies may be summarized as follows:

(1) No double power conversion, which results in reduced power losses.

(2) The transformer leakage energy is stored in the decoupling capacitor. This means that there is no need for extra dissipative clamp circuits. Again, this will reduce the power losses.

(3) Fewer components are used in the proposed decoupling circuit.

4.2 Future Work

The efficiency of the proposed topology should be studied thoroughly. But, with a quick comparison with the results in [18], the proposed topology is expected to have a maximum efficiency of more than 87%.

A closed loop prototype for the proposed topology has to be done in order to test the efficiency and the performance accurately. Even though that an open loop prototype was built and tested in this thesis to verify the operation modes of the proposed topology.

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