DESIGN AND SIMULATION OF CMOS ACTIVE MIXERS

by

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ABSTRACT

This paper introduces a component of the Radio Frequency transceiver called the mixer. The mixer is a critical component in the RF systems, because of its ability for frequency conversion. This passage focuses on the design analysis and simulation of multiple topologies for the active down-conversion mixer. This mixer is characterized by its important design properties which consist of conversion gain, linearity, noise figure, and port isolation. The topologies that are given in this passage range from the most commonly known mixer design, to implemented design techniques that are used to increase the mixers important design properties as the demand of CMOS technology and the overall RF system rises. All mixer topologies were designed and simulated using TSMC 0.18 μm CMOS technology in Advanced Design Systems, a simulator used specifically for RF designs.

To my parents, family, and friends

ACKNOWLEDGMENTS

I would like take this time to thank my advisor Dr. Jiann S. Yuan, for his guidance and complete support throughout not only my graduate career, but my undergraduate career at UCF. Also I would like to thank my committee members Dr. Sundaram and Dr. Lei Wei for their corporation and support.

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LIST OF ACRONYMS AND ABBREVIATIONS

ADS	Advanced Design System
ADC	Analog-to-Digital Converter
CG	Conversion Gain
dB	Decibels
dBm	Milli-decibels
DAC	Digital-to-Analog Converter
DB	Double Balance
HPF	High-pass Filter
IF	Intermediate Frequency
LO	Local Oscillator
LNA	Low-noise Amplifier
LPF	Low-pass Filter
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
NF	Noise Figure
PMOS	P-channel Metal Oxide Semiconductor
PA	Power Amplifier
RF	Radio Frequency
SNR	Signal–to-Noise Ratio
SB	Single Balance
SW	Switched
TSMC	Taiwan Semiconductor Manufacturing Company

CHAPTER ONE: INTRODUCTION

The subject of Radio Frequency circuitry has been becoming more importance throughout recent years. The topic of radio frequency (RF) communications has taken great strides from cell phones to base stations. With that being said the communication industry has been revolutionizing the way the world transmits and receives information with growing demand. With this increase in demand the communication industry has been motivated to expand and create more reliable and efficient components.

Introduction to RF Communications

In order to accomplish these goals there needs to be an increase in frequency range, software, and hardware design. The quality of software design has been steadily inclining due to the increase of computing power. An increase in Hardware and range can be reached by more complex component designs. An example of this is shown via block diagram in Figure 1. This figure depicts a simplified diagram of a base station transceiver.

This system consists of a receiver and a transmitter sections. In the receiver section the signal would enter into the antenna. The signal usually becomes weak due to noise interference and attenuation at the antenna, and needs to be properly arranged to enter the system. This is reached by using a Low-Noise-Amplifier (LNA). The LNA will amplify the desired signal while adding as little distortion as possible. Then the signal is sent to the down conversion mixer and low pass filter (LPF) to be converted and tuned.

This change into a lower frequency is necessary for the signal to be converted for processers purposes. The analog signal is then converted to digital data via the analog-to-digital converter (ADC). Finally, the bits of data are used for processing purposes.

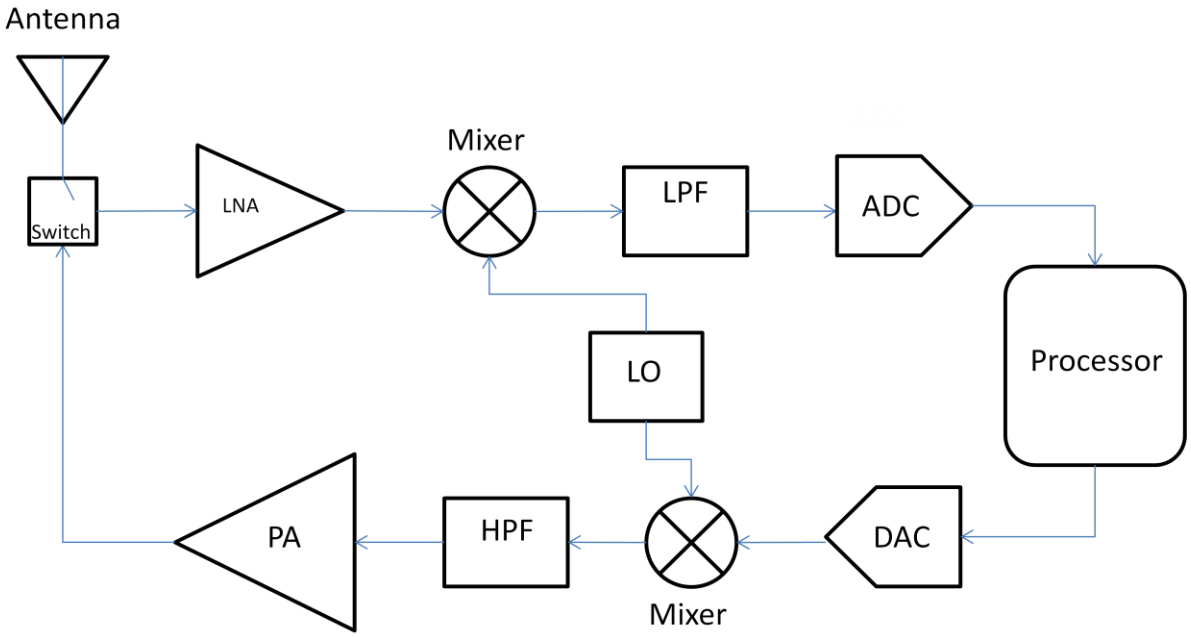

Figure 1: General RF Transceiver Diagram

In the transmission section the bits of data are converted from digital bits to an analog signal by the digital-to-analog converter (DAC). The signal is then sent to an up conversion mixer and high pass filter (HPF), which shifts the original frequency to a higher frequency for communication. The new signal is then sent to a power amplifier (PA) to increase the power for the signal, and prepare the signal for its distance travel. The signal is then transmitted though the antenna.

Introduction of the Basic Mixer

The basic configuration of a single mixer is that it has two inputs and one output. It multiplies or 'mixes' the carrier signal, either RF or intermediate frequency (IF) depending on an up conversion or down conversion mixer, with another input from the local oscillator (LO). The LO signal input terminal is used to assist in the heterodyning process, produces the difference and sum frequencies of the two input terminals of interest. After, the output frequencies come out of the output terminal. This subject is built upon and expanded in more depth in the paragraphs below.

In an ideal nonlinear mixer the heterodyning process will become clearer in the following equations, which were obtained and summarized from [1].

If both input signals show:

$$a = A\cos\omega_1 t \tag{2.1}$$

and

$$b = B\cos\omega_2 t \tag{2.2}$$

The mixer output signal after mixing yields,

$$a \cdot b = A\cos\omega_1 t \cdot B\cos\omega_2 t = \frac{AB}{2}\cos(\omega_1 - \omega_2)t + \frac{AB}{2}\cos(\omega_1 + \omega_2)t \tag{2.3}$$

This shows that the mixers output consists of the difference and summation of both input frequencies. A mixer can cater to either output function where the unwanted function can be filtered out. The chosen function, which can be either the differences or summation of the input frequencies, receives the term down conversion mixer or up conversion mixer respectively.

In a typical mixer design there are four primary defined specifications that are shown and explained below: Conversion Gain (CG), Linearity, Noise Figure (NF), and

Port isolations. The CG is a ratio between the output signal and the input signal usually in the measure in decibels (dB) or, milli-decibels (dBm). The linearity of the mixer is defined as how well the mixer reacts to the mixing of frequencies and ideal law of superposition in the ideal case explained in above text. NF is a ratio of the signal-to-noise ratio (SNR) at the IF output and the SNR at the RF input port. Finally, the port isolation parameter shows how much leakage of signal occurs between two ports.

Goals and outline

The primary goal of the research paper is to study and research the different design topologies of the active down conversion Mixer, and compare the models of the mixer to the designs used in Advance Design System (ADS). The data from the simulation will then be compared to other designs specifications.

In Chapter Two, the different mixer specifications will be provided for a better understanding of the mixer component. Then the single balance (SB) Gilbert cell mixer design will be introduced and explained using analytical equations. Part of the explanation will include how different components that are used in the makeup of the mixer can affect its outputs. Advantages and disadvantages of the design will then be compared to other mixer designs. Chapter Three will introduce the current bleeding mixer design technique topology, and compare its simulated results to the results of the standard Gilbert cell design in the previous chapter. Chapter Four explains the double balance (DB) Gilbert cell design and compares its simulated data to the SB design. The

pros and cons of this design are also betrayed in this section. Chapter Five will introduce a switch transconductance mixer design, and explicate the simulated data in comparison to the fundamental build of the conventional mixer design. Finally, in Chapter Six the overall work is then summarized and concluded.

References

[1] J.P.Silver, “Gilbert Cell Mixer Design Tutorial,” 2003, http://www.odyseus.nildram.co.uk/RFIC_Circuits_Files/MOS_Gilbert_Cell_Mixer

CHAPTER 2: SINGLE BALANCE GILBERT CELL MIXER

With multiple mixer designs that can be used in practical applications in today's industry, a designer now has a broader choice of which topologies are better suited to meet system requirements. One of the most popular mixer designs is the Gilbert cell mixer. The reasons for its popularity are its balanced operation, and ability to allow a more clear output. The design gives a moderate gain, port isolation & linearity at a low LO power while maintaining a low noise figure, and overall power consumption. The specific topology will be expanded and explained in the sections below.

Single Balance Gilbert Cell Mixer Design

The way that the SB Gilbert cell mixer design operates is depicted in Figure 2 below. The single wave RF signal first enters into the base of the lower transistor M1, while the LO signal is separated into the based into the base transistors M2 and M3. The input RF signal is then converted into current in the transconductance stage. The current signal is then mixed in with the switching LO signals in M2 & M3. The mixed current is then converted back into voltage via the load, in this case resistors R1 & R2, then the output exits from the respective IF outputs. When this process is taking place the mixer definitions can be controlled and manipulated using particular sections of the layout.

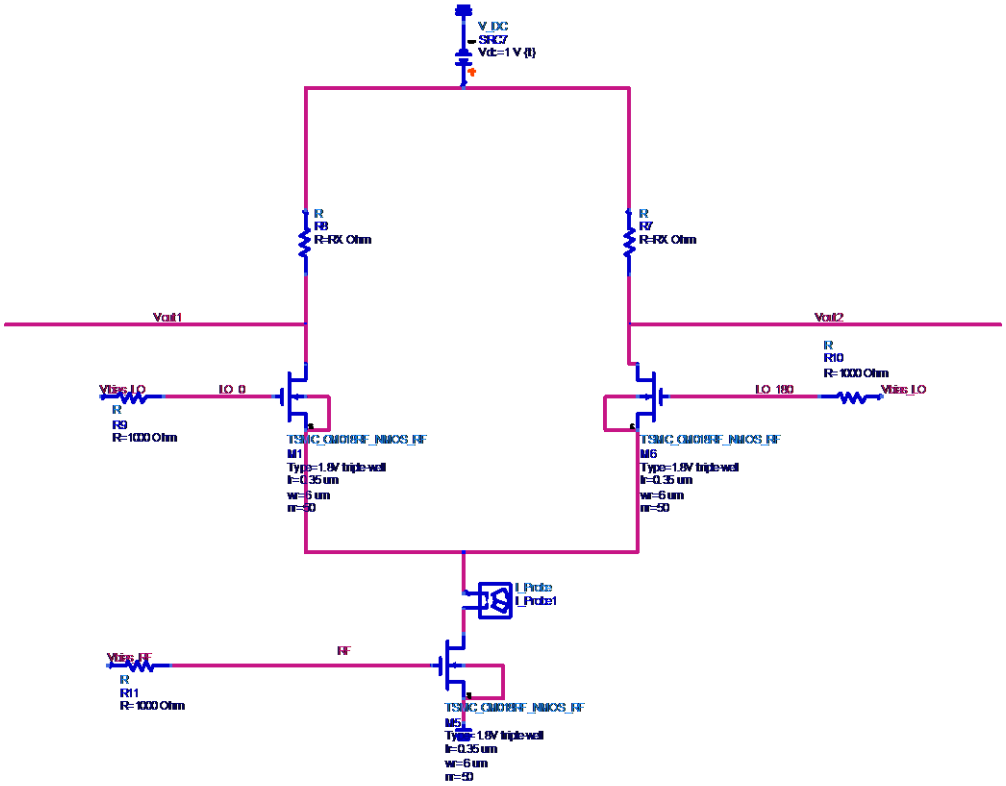

Figure 2: SB Gilbert Cell Schematic layout

Gilbert Cell Mixer Design Parameter Analysis

Then it comes to CG there is a tradeoff between the resistive load and the drain current in the transconductance stage shown in the following equations below from [1].

$$R_L = \frac{V_{DD} - V_3}{I_{DSswitch}} \tag{2.1}$$

and

$$CG = \frac{2}{\pi} R_L \sqrt{K_{nRF} \cdot I_{dsRF}} \tag{2.2}$$

where

$$I_{dsRF} = \frac{k_n \cdot W}{2 \cdot L} \cdot \left(V_{gs} - V_T\right)^2 \quad (2.3)$$

The resistive load is limited to the supply voltage (V_{DD}) and the dc currents of M2 & M3. Also shown in equation 2.2, a mixers CG is directly proportional to R_L and I_{dsRF}. A raise in biasing current ($I_{DSswitch}$) will disturb the voltage drop on the switching transistors and cause the overall load resistance to decrease lowering the CG. Also for a given V_{DD}, if the bias current in the transconductance stage is raised or lowered the resistive load also needs to be tweaked in order to maintain the voltage biasing conditions of the switching transistors, and not cause a drop in gain.

The linearity, more specifically IIP3, of the SB Gilbert cell can be controlled by both the transconductance stage and switching stages. IIP3 is directly proportional to both the drive current and the overdrive voltage shown below.

$$IIP_3 = 4\sqrt{\frac{2}{3} \cdot \frac{I_{dsRF}}{K_n}} \quad (2.4)$$

and

$$IIP_3 = 4\sqrt{\frac{2}{3} \cdot \left(V_{gs} - V_T\right)} \quad (2.5)$$

Where the V_{gs} is the gate voltage of the switching transistors and V_T is the threshold voltage of the given Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Also note that the overdrive voltage in equation 2.4 can affect the CG in the previous

paragraph. The transistors need enough voltage head room so that the LO amplitude will not swing too high allowing the MOSFET to leave the active regions in the I-V curve and warping the CG.

The NF of the Gilbert cell mixer is mainly affected by the transconductance stage, and secondly by the switching stage via transistor size. The increase in the driver current is inversely proportional to g_m, which is inversely proportional to the NF given below [2].

$$NF = 10log\left(1 + \frac{2\gamma_n}{g_m \cdot R_s} + \frac{2}{g_m^2 \cdot RR_s}\right) \quad (2.6)$$

where

$$g_m = \frac{2 \cdot I_{dsRF}}{(V_{gs} - V_T)} \quad (2.7)$$

Lastly, the port isolations are controlled by three equations given in ADS.

$$LO_{IF}\ isolation = dBm\big(mix(HB.V_{out2}, \{0,1\})\big) - LO\_power \quad (2.8)$$

$$RF_{IF}\ isolation = dBm\big(mix(HB.V_{out2}, \{1,0\})\big) - RF\_power \quad (2.9)$$

$$RF_{LO}\ isolation = dBm\big(mix(HB.LO.0, \{1,0\})\big) - RF\_power \quad (2.10)$$

These equations find the dBm of the mixed outputs of the desired frequencies, and then subtract them from the respected input ports. The secondary factors that assist in determining these mixer topology definitions will be presented in the conclusion section via informative tables.

Advantages and Disadvantages

Given the information stated in the above sections the ideal SB Gilbert cell appears to be very beneficial. With that being said, every design has this hits and misses. While this design gives moderate good gain at a lower LO power, and low power consumption sometimes these specs can be compromised for other needed specifications. Some of those topics include when a designer needs a higher gain and/or system linearity and is willing to trade off power consumption or even NF achieve that design goal. The point that hopefully is getting across is that this design is not powerful enough to meet all the many mixer design specifications demanded by the communication industry.

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[1] Skander Douss, Farid Touati, Mourad Loulou. “An RF-LO current-bleeding doubly balanced mixer for IEEE 802.15.3a UWBMB-OFDM standard receivers,” *International Journal of Electronics and Communications,* vol. 62, no. 7, pp.490-495, Aug.2008.

[2] V. Vidojkovic, J.D van der Tang, A. Leeuwenburgh, A. van Roermund, “Mixer Topology Selection for a Multi-Standard High Image-Reject Front-End,” in *Prorisc Proceedings,* 2002, pp.526-530.

CHAPTER 3: SINGLE BALANCE CHARGE INJECTION MIXER

As explained previously, in the SB Gilbert cell mixer only moderate CG and linearity can be reached at a particular LO power. One possible method to improve this area of concern is to increase the LO power. The problem that occurs with this method is due to the mixers smaller topology. If the SB Gilbert cell mixers LO power is too high it will cause the function of the mixer to perform improperly, jeopardizing the CG and linearity specifications, and overall affecting the mixers performance. Another method is to figure out a way to separate the strong bond between CG and linearity in a Gilbert cell mixer design. A solution to this problematic area of concern is called charge injection or current bleeding design. The charge injection technique can achieve what was deemed impossible in the conventional Gilbert cell mixer; improve simultaneously the CG and IIP3. The proposed mixer topology injects the driver stage bias current using a current source, while also being considered part of the driver stage. Using this method not only improved the CG and linearity of the circuit, but also improves all the other mixer design specifications using the same LO power from the conventional SB Gilbert cell design.

How Charge Injection technique works

Schematic diagrams are depicted below in figure 3 and figure 4. These figures are CMOS based SB mixer without and with charge injection respectively. Figure 4 shows that the injection of the current allows the control of the DC currents in both of the switching transistor I_{D5} and I_{D6} separately from the driver stage current I_{D4}.

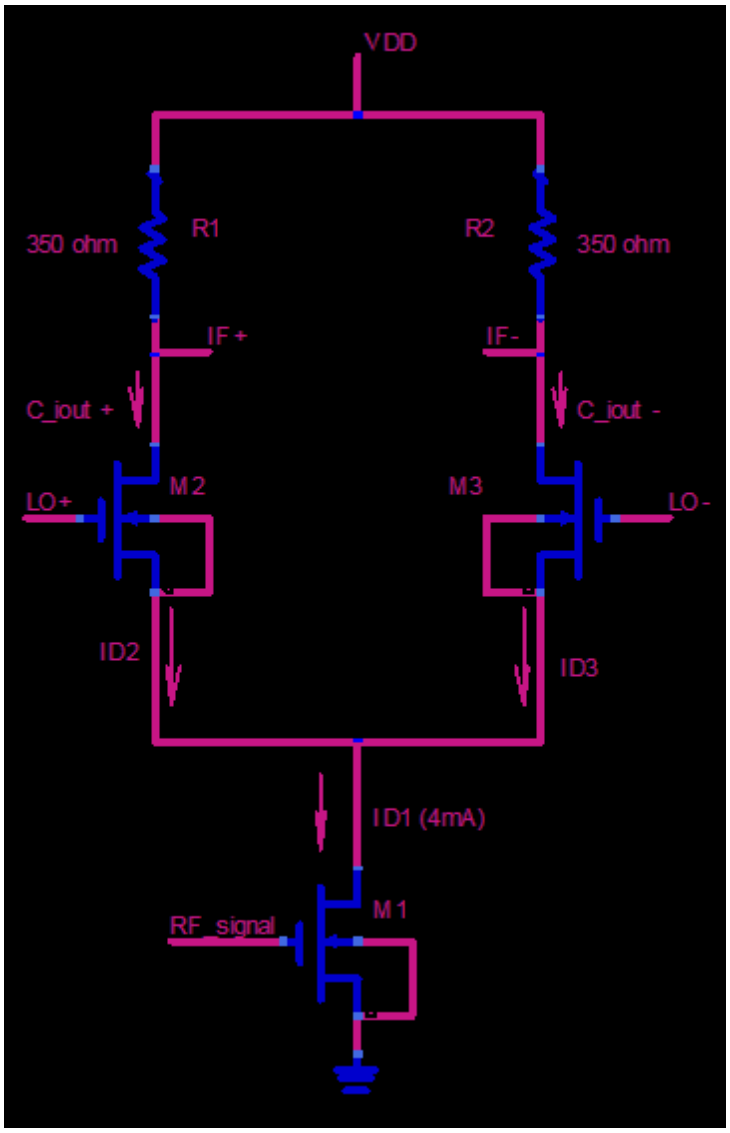

Figure 3: Schematic of Conventional SB Gilbert Cell Mixer

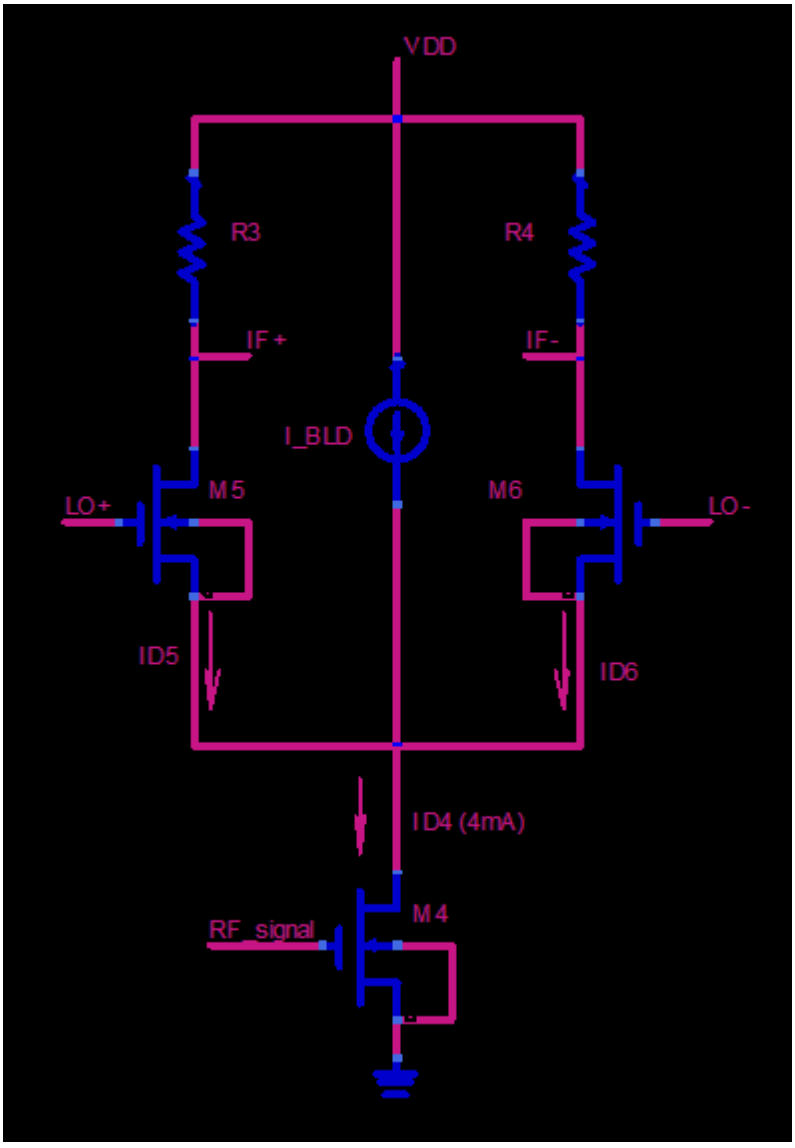

Figure 4: Schematic of SB Gilbert Cell Mixer with Charge Injection

This means that in charge injection it is possible for the summation of the two switching transistors DC currents (I_{D5} &I_{D6}) to become greater than the DC driver stage current I_{D4}. This differs from the conventional mixer that states the summation of I_{D2} and I_{D3} is equivalent to I_{D1}, as explained in [1].

Charge Injection Technique Mixer Design Improved Specifications

As stated from the previous chapter CG is directly proportional to the driver stage bias current and load resistance, while the mixers linearity is directly proportional to the driver stage bias current. In the charge injection technique both the driver stage bias current may become increased while the resistive loads, R_3 and R_4 do not affect the DC switching currents. In achieving this, charge injection increases the CG by raising the driver current I_{D4} without forcing the resistive loads to be lowered to maintain the switching transistors bias conditions. Linearity is also improved, because of the increase of current in the driver stage (I_{D4}) without varying the drain source currents in the switching stage (I_{D5} &I_{D6}). The charge injection technique has found a solution to a potentially problematic tradeoff in the conventional mixer design between the CG and linearity, but it does not stop here.

Figure 5 shows the SB mixer charge injection with the implementation of a p-channel transistor. This figure is shown to better explain the relationship between charge injection and the increase in mixer design specifications. The NF is reduced, because the charge injection source is made part of the driver stage. This increases the driver biasing current; therefore, raising the overall transconductance and increasing the NF.

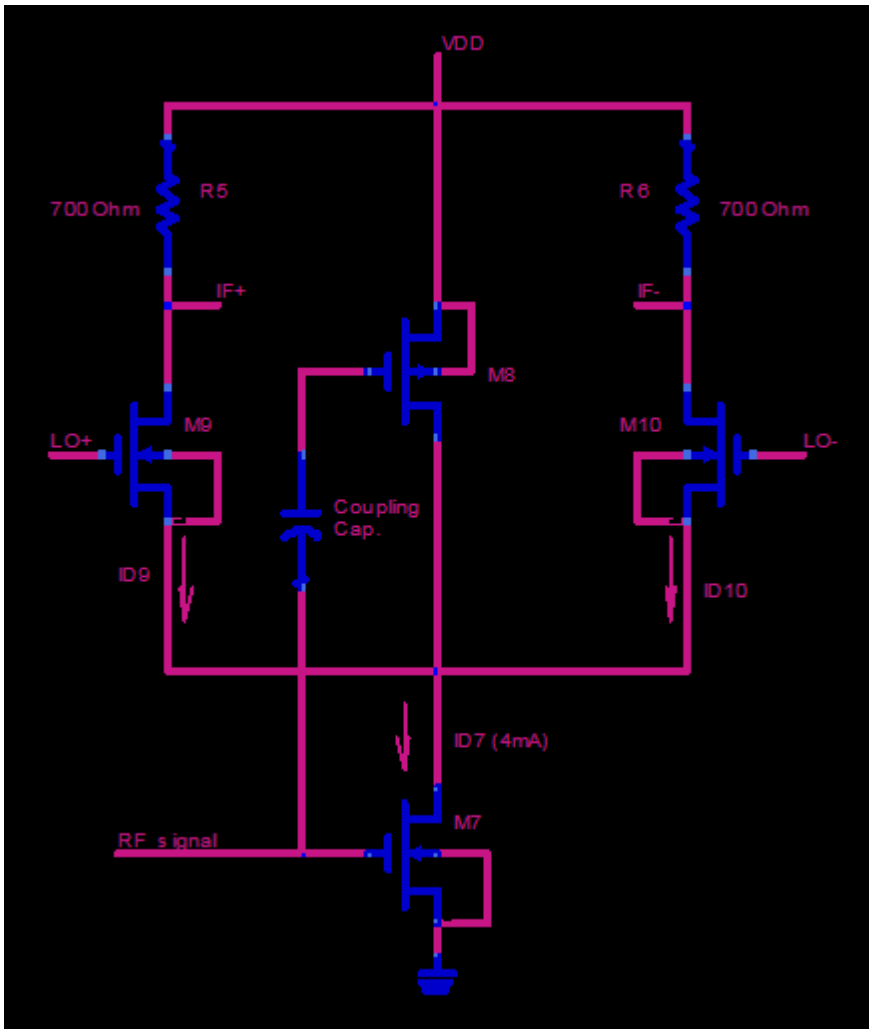

Figure 5: Schematic of SB Charge Injection GC Mixer with implemented PMOS

Charge injection also improves the port isolations as well. An example is given in [1], showing a better LO-IF port isolation. Assuming ideal LO switching and using the long channel device expressions for drain current in a MOSFET, the differential output currents of both the conventional and charge injection mixers are given by

$$i_{OUT,conv} = i^{+}_{OUT,conv} - i^{-}_{OUT,conv} \tag{3.1}$$

$$= \frac{4I_{D1}}{\pi}\cos\omega_{LO}t + \frac{2g_{mn1}v_{RF}}{\pi}\cos(\omega_{LO} \pm \omega_{RF})t + higher\ order\ terms$$

and

$$i_{OUT,bld} = i^{+}_{OUT,bld} - i^{-}_{OUT,bld} \tag{3.2}$$

$$= \frac{4(I_{D7}-I_{D8})+(\beta_{n7}-\beta_{n8})v^2_{RF}}{\pi}\cos\omega_{LO}t + \frac{2(g_{mn7}+g_{mn8})v_{RF}}{\pi}\cos(\omega_{LO} \pm \omega_{RF})t\ + higher\ order\ terms$$

respectively, and where g_{mn1}= g_{mn7}, g_{mn8} are the transconductance of M_1, M_7, and M_8. β_{n7} and β_{n8} are part of the KP·W/L of M7 and M8 are the transconductance parameters, channel width and channel length of the MOSFET's. V_{RF} is the amplitude of the input RF signal, and ω_{LO} and ω_{RF} are the LO and RF signal frequencies respectively. From equation 3.2 shows that the charge injection mixer gives complete LO isolation at the output if

$$4(I_{D7} - I_{D8}) + (\beta_{n7} - \beta_{p8})v^2_{RF} = 0 \tag{3.3}$$

This shows that for a small V_{RF}, it is possible that the LO signal at the output can be cancelled by making I_{D7}=I_{D8}. When this is achieved the switching pair operate like a passive mixer, but since this is an active mixer only partial LO cancellation occurs (I_{D7}>I_{D8}) in term is better than its conventional counterpart. The ratio amount between both I_{D7} and I_{D8} currents depend on the size of the implemented p-channel transistor. This in turn, determines how well port isolation occurs. The results section will show the

data that proves that the charge injection technique is more advanced design then the SB Gilbert cell design.

Charge Injection Design Issues

There are mainly two down falls with this design, considering it was created to improve mixer definitions in other design topologies. One is that the charge injection technique can degrade the high frequency performance of the driver stage due to having higher output impedance. This is due to the smaller available DC currents that reduce the transconductance in the switching transistor stage. The other is that there are more noise signals added into the system, due to the charge injection, but this can be reduced based on what is chosen as the implemented injection device.

References

[1] S.-G Lee, J.-K. Choi. “Current reuse bleeding mixer.” (IEEE Journal of IET Electronic Letters) vol. 36, no. 8 (April 2000): pp. 696-697.

CHAPTER 4: DOUBLE BALANCE GILBERT CELL MIXER

Even though the SB Gilbert cell mixer is a solid design and may achieve the goals for some design systems, it may not be sufficient for designs that call for increased mixer specifications. This is where the Double Balance (DB) Gilbert cell mixer can meet those requirements. DB Gilbert cell mixer is the most commonly used active mixer architecture, and contains improvements over other designs including the CB Gilbert cell mixer. The DB mixer can achieve higher mixer specifications in the area of CG, linearity, and port isolation at the cost of a small increase in NF and overall designs power consumption. A summary of the DB topology and how its specifications are calculated are shown in the continuance of this chapter.

DB Mixer Topology Overview

The DB design consists of basically two SB mixers placed together. Figure 6 illustrates the circuit of the proposed mixer, and is summarized from [1]. One of the first things that may stand out is the current source called I_{ss} located at the bottom of the diagram. This is called source degeneration and is used to assist in the linearity and stability of the mixer. Another change is the differential RF input in the transconductance stage. The DB design still contains one transconductance stage and one switching stage, but now the bottom stage has two transistors while the switching operations consist of two pairs or four total transistors. Each time the switches change position the small signal current changes directions through the load resistors, and mixes with the

LO signal, converting the current into a voltage. The differential output is then measured for gain and other mixer definitions.

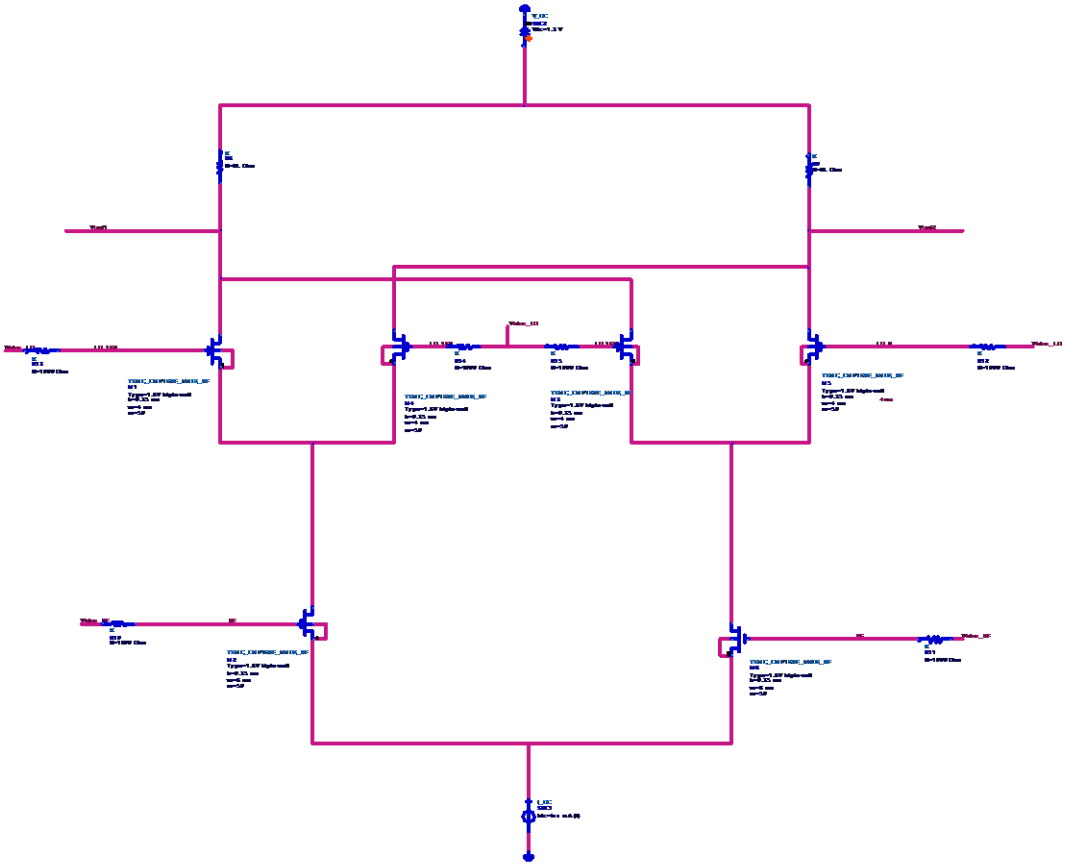

Figure 6: DB Gilbert Cell Architecture

DB Mixer Design Merits

The mixer equations for the DB Gilbert cell mixer design have the same relationships as the SB mixer, but are not identical. The DB Gilbert cell mixers design equations are given below as shown in [2].

$$G_c = \frac{2}{\pi} R_L \sqrt{\mu_n C_{OX} \frac{W_1}{L_1} I_{ss}} \quad (4.1)$$

or if using square wave switching CG can be shown as

$$G_c = \frac{2}{\pi} \frac{g_m R_L}{2} \quad (4.2)$$

$$IIP_3 = \sqrt{\frac{32}{3} \frac{I_{ss}}{\mu_n C_{OX} {}^{W_1}/_{L_1}}} \quad (4.3)$$

$$NF = \frac{\pi^2}{4} \left(1 + \frac{2\gamma}{g_{m\_RF} R_S} + \frac{2}{g_{m\_RF} R_S R_{load}}\right) \quad (4.4)$$

Where R_s and R_{load} are the source and load resistance. The equations consist of the CG, linearity, and NF respectively, while the port isolation is found using the same equation shown in an earlier chapter.

DB and SB Gilbert Cell Mixer Comparisons

When it comes to the mixer definitions, the DB Gilbert cell mixer is better in most areas compared to the SB mixer design. The CG is better in DB because it has the capacity to maintain a higher transconductance. As for linearity, in the DB Gilbert cell the ports suppress the input frequencies better than the SB mixer allowing better control over harmonic products. In the area of port isolation the DB architecture is higher due to

the transistor stacking and schematic setup. This provides better isolation between the input and output ports. The cost of gaining these improvements comes with the cost of higher NF and power consumption. The NF is typically higher in the DB design, because there are more transistors. Also the design has a higher probability of noise being created by non ideal switching transistors. Another sacrifice is a higher power consumption that occurs from an increased supply voltage. This voltage raise is needed to properly operate the multiple transistors that are needed to build the larger DB design.

References

[1] L.A NacEachern, Y. Manku, “A Charge- Injection Method for Gilbert Cell Biasing,” in *Electrical and Computer Engineering Canadian Conference*, 1998, pp. 365-368.

[2] World Academy of Science Engineering and Technology, “A Low Voltage High Linearity CMOS Gilbert Cell Using Charge Injection Method,” 2008, http://www.waset.org

CHAPTER 5: SWITCH TRANSCONDUCTANCE MIXER

As time passes technology advances and microelectronics improves are made. One of the primary goals for future MOSFET advancement is to decrease the overall size of the device. As the MOSFET's size is lowered the supply voltage that turns on the MOSFET's must decrease as well or there will be device malfunctions. This may become a bit of a nuisance for different mixer designs, and their ability to switch properly during the mixers multiplication process, creating lower design specifications. A newer design topology called the switch transconductance (SW) mixer was created to operate on par with the standard mixer design specifications like the Gilbert Cell mixer. Other benefits include less voltage headroom for LO switching and avoiding gate oxide reliability problems, meanwhile achieving a lower operation voltage meaning decrease in power consumption.

Switching problems

In an RF mixer, frequency translation is achieved in the multiplication stage where the input RF signal and the LO signal are mixed. In the operation of common mixers this is done using hard switching in the switching stage. A functional representation of the Single Balance active MOSFET mixer without the load network is shown in figure 8a. This figure is used for a better understanding on the switching stage. The two switching transistors shown as LO and LO (not) act as cascade devices for the transconductance stage in order to improve output resistance and linearity of the

system, and they operate in saturation mode to achieve these goals. In the figure further below the transconductance stage is modeled as a voltage controlled current source with a large signal I(V), a small signal transconductance g_m, and a input bias voltage with the input RF voltage (V_B+V_{RF}).

In a low supply voltage situation in order to achieve a low noise figure and a decent conservation gain and linearity, the transistor in the transconductance stage is biased in strong inversion and the saturation region. In addition if one wanted to use a degeneration approach for higher system linearity even more voltage headroom is needed in the transconductance stage. With this being said typically the minimum voltage for the switching gates are well above the low supply voltage range of approximately 1 volt. In order for the mixer switching to operate at such a low supply voltage other driver circuits need to be implemented to drive the switching transistor gates. One problem that presents itself is major gate oxide reliability issues. This arises due to the further reduction of transistors size that will eventually cause failure and a lower operation life of the transistors in the switching stage. Another problem that will happen if the oxide holds out is the reduction of the conventional mixers conversion gain design parameter. Because of the switching transistors needing so much voltage headroom to operate, the voltage headroom needed for the load stage is reduced limiting the mixers yet gain. There are different solutions that have been presented to remedy these issues, but at the cost of bandwidth, large chip area, or degradation of the mixers overall design parameters. The SW transconductor mixer proposes a solution to

large voltage headroom and future oxide reliability issues without raising chip area or greatly compromising mixer design parameters.

How Switch Transconductance Mixer Operates

In the SW transconductor mixer the design parameters are reached in a different manner than the conventional mixer. A device that is already well known in digital logic has a low ohmic switch that reduces voltage headroom, and also does not have the oxide reliability issues stated in the above section. The device is called the inverter and is the vital key to this specific topology, due to the ability to avoid a requiring conductive channel between the V_{DD} and V_{SS} voltage supplies. The SW transconductor method implements the inverter concept into a RF mixer design. Figures 7 and figure 8 show the transformation concept of a single balance conventional mixer to a switched transconductor mixer. Figure 9 shows the SW transconductor mixer CMOS implementation from ADS. As can be seen from fig.7, there are two matched transconductor g_{m1} and g_{m2} which are being alternated by the switching of the inverters connected to only V_{DD} and V_{SS} voltages. This operation is creating the same similar multiplication function as used in the conventional mixer figure.

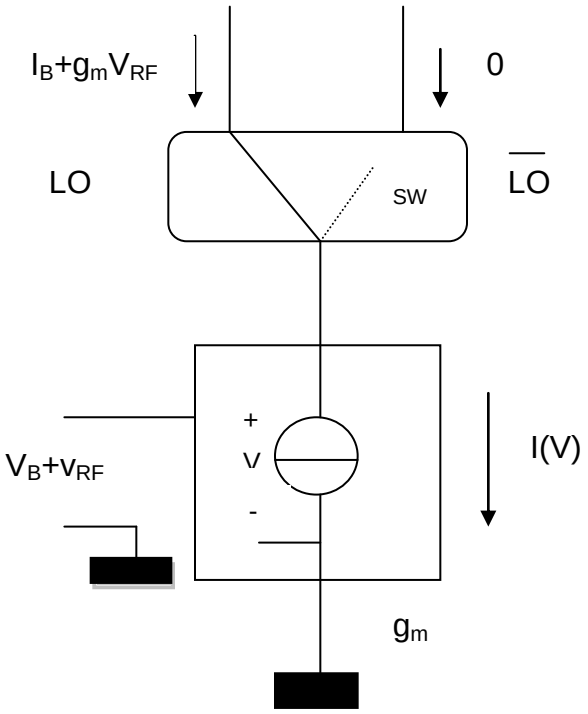

Figure 7: Conventional Mixer Concept

In figure 7b the transconductors have a non linear I(V) characteristic with a transconductance g_m around a bias point V_B and I_B just like the conventional mixer. One of the matched transconductors is switched on to the bias point by the switch to V_{DD} and switched off by V_{SS} and vice versa for the other transconductor; therefore, when g_{m1} is on, g_{m2} is off. When there are matched transconductors and ideal instantaneous switching, I_{o1} or I_{o2} is equal to $I_B + g_m v_{RF}$, and the other current is equal to zero, same as in a conventional mixer design.

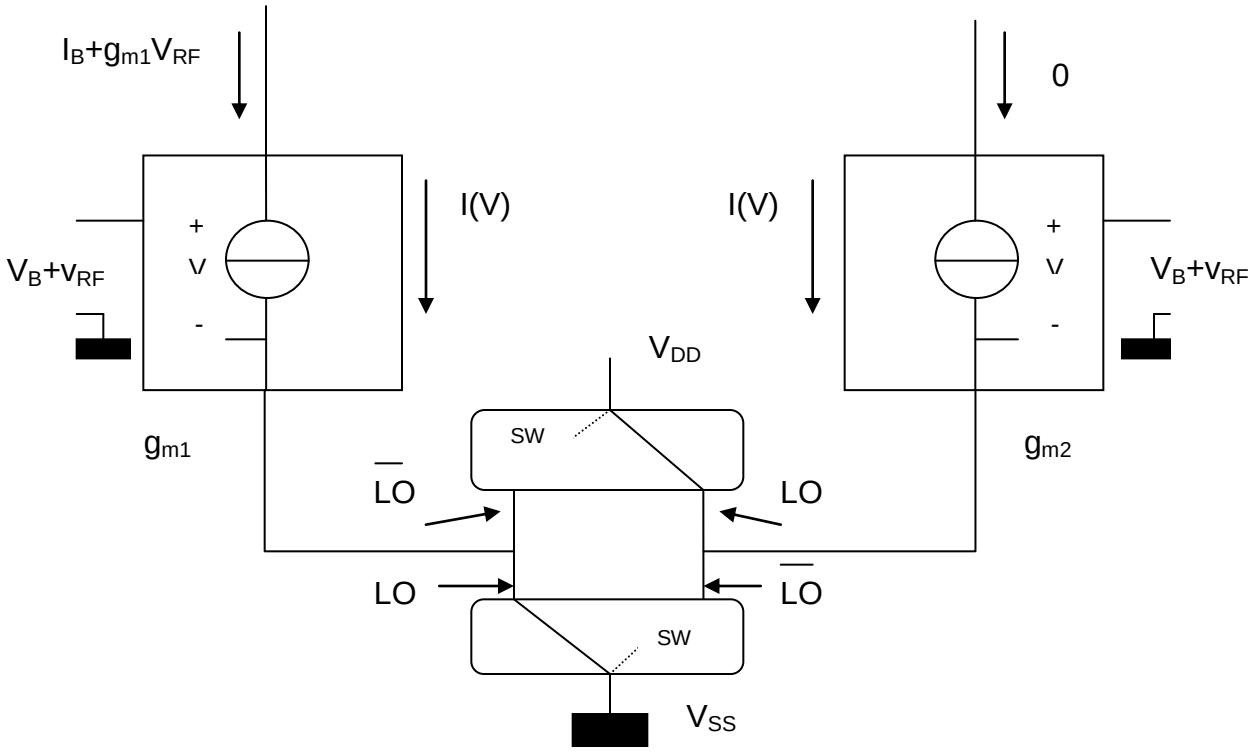

Figure 8: Switched Transconductor Concept

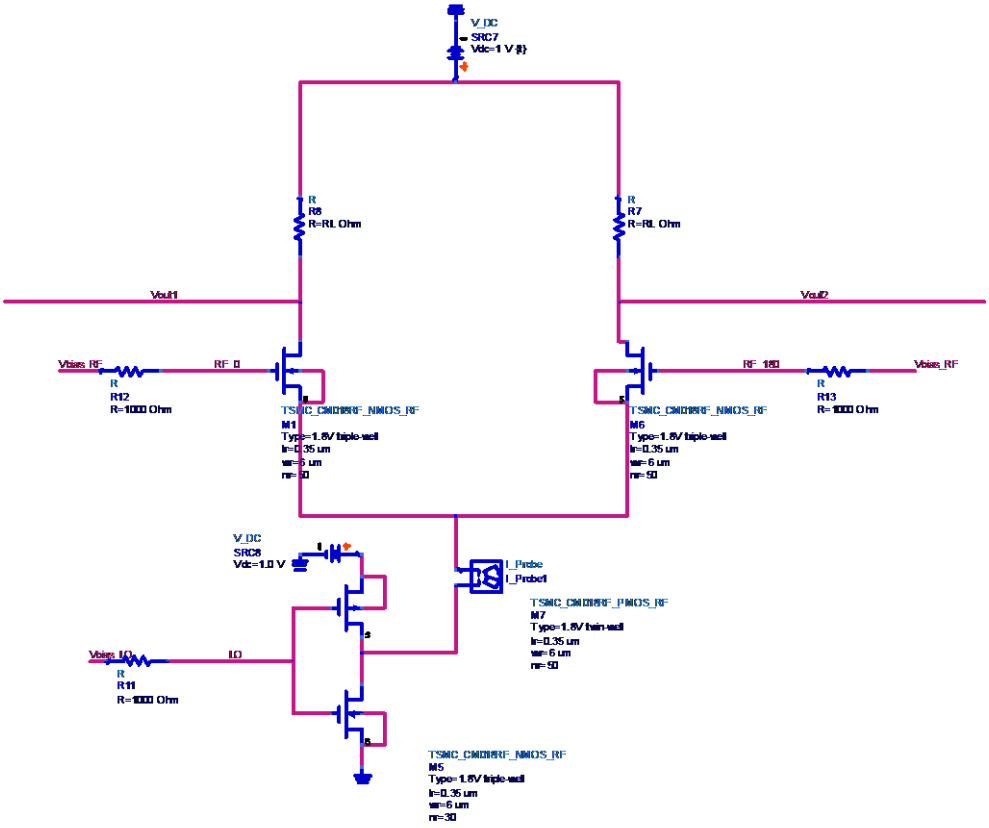

Figure 9: Switched Transconductor Mixer NMOS Implementation

A closer look into the SW transconductor mixer design will be explained below using the double balanced version to verify that both design implementations achieve the same goals as the conventional mixers even though the topologies are different.

Analysis between Switched transconductor and Conventional DB Mixer

This method is not limited to only single balance mixers, but to double balance mixers as well. Single balance mixers tend to have a strong output signal at the LO

frequency, but this can be canceled in the double balanced mixer version depicted below in figure 10. The SW double balance mixer checks to operate the same as the conventional double balance mixer, and the CG for the SW double mixer is the same as its SW single balance counterpart due to the RF voltage being divided over two transconductors. This is explained in further detail below.

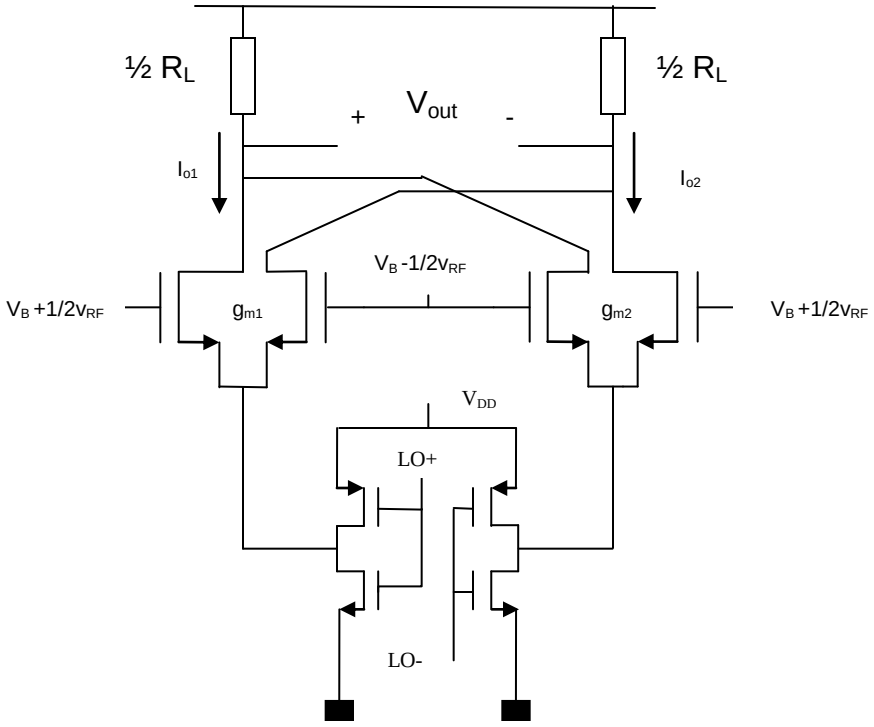

Figure 10: Switched Transconductor Double Balanced NMOS implementation

In the SW transconductor double balance mixer above shows the two differential pairs operating as g_{m1} and g_{m2}, and two anti-phase CMOS inverters that are used as the LO switches. Lets first focus on the left half of the mixer that has the transconductor of

gm1 to make a point of how the CG stays the same. If the capacitive effects are neglected and there is a low ON-resistance the differential transconductor can be subdivided into two independent transconductors. The output current I_{o1gm1} is a function of both an instantaneous LO voltage and the RF input voltage, $V_{LO}(t)$ & $V_B + 1/2v_{RF}$. This simply states that the output of the mixers current after multiplication is dependent on both the two input signals, and MOSFET biasing, obtained from [1,2]. Equation 5.1 shows this relationship.

$$I_{O1,gm1} = F\left(V_{LO}(t),\ V_B + \frac{1}{2}v_{RF}\right) \tag{5.1}$$

The v_{RF} is small; therefore a first order Taylor expansion is used to further approximate the equation 5.1 above:

$$I_{O1gm1} \cong F(V_{LO}(t), V_B) + \frac{\partial F(V_{LO}(t), V_B)}{\partial V_B} \times \frac{1}{2}v_{RF} \tag{5.2}$$

and is also written as

$$I_{O1gm1} = I_{B1}(t) + g_{m1}(t) \times \frac{1}{2}v_{RF} \tag{5.3}$$

where $I_{B1}(t)$ is the time-variant bias current of the transconductor gm, and $g_{m1}(t)$ is the time-variant transconductance of the individual transistors from the mixers operation. The same analysis can be applied to the anti phase RF signal path by dint of g_{m1} to the output current I_{O2} furnished

$$I_{O2gm1} = I_{B1}(t) - g_{m1}(t) \times \frac{1}{2} v_{RF}. \quad (5.4)$$

Then the differential output current for $I_{O,gm1}$ is shown in the below equation:

$$I_{O,gm1} = I_{O,gm1} - I_{O,gm2} = g_{m1}(t) \times v_{RF}. \quad (5.5)$$

As shown in the last equation $g_{m1}(t)$ determines the conversion transconductance. Now assuming ideal instantaneous switching, a square wave transconductance function is used to better explain switching time dependency. The square wave has a period T_{LO} that is switching from zero to an ON value of g_{mO}. The ON value is determined primarily by the I(V) characteristic of g_{m1}devices and the biasing voltage V_B. Note that if the switches have non-negligible series resistance compared to $1/g_{mO}$, the conversion transconductance will be lower than ideal. A similar derivation, as was given in g_{m1}, can be achieved of g_{m2} and is given as

$$I_{O,gm2} = g_{m2}(t) \times v_{RF} \quad (5.6)$$

where g_{m2} will be activated by the inverse switch of the LO signal. Assuming a 50% duty cycle the time-variant transconductor g_{m2} is given as

$$g_{m2}(t) = g_{m1}\left(t + \frac{T_{LO}}{2}\right). \quad (5.7)$$

The overall differential output current is now given in equation 5.8

$$I_o = I_{O,gm1} - I_{O,gm2} = \big(g_{m1}(t) - g_{m2}(t)\big) \times v_{RF} = g_{eff}(t) \times v_{RF} \qquad (5.8)$$

The differential output transconductance is then converted into a voltage output when the current (I_O) is introduced to the two load resistors. If the resistor values are $R_L/2$, the output voltage is then

$$V_{out} = -\frac{R_L}{2}\big(I_{o,gm1} - I_{o,gm2}\big) = -g_{eff}(t) \times \frac{R_L}{2} \times v_{RF}\ . \qquad (5.9)$$

At low LO frequencies, the CG is approximately equal to equation 5.10.

$$CG = \frac{2}{\pi} g_{mo} \frac{R_L}{2} \qquad (5.10)$$

This equation is the same conversion gain that is used for a conventional double balance mixer. Please note that even though the CG of both mixer topologies is shared and the signal transfers are equal as well, the mixers functionalities are implemented differently. The SW transconductor mixer uses time-variant I-V conversions in a way that the transconductance [$g_{m1}(t)$ & $g_{m2}(t)$] are alternately multiplied by g_{mo} and 0, but the time is shifted by $T_{LO}/2$. In a conventional mixer the I-V conversion is time-invariant and the resulting currents are multiplied by + 1 and -1.

As for the other mixer design parameters, they are on par with the conventional mixer design. The NF of the SW transconductor mixer has the potential of being slightly

lower than the conventional mixer because of a lesser effect on thermal and flicker noise. Thermal noise is reduced in the double balanced SW transconductor mixer , because the noise current that is introduced by switching devices results in a common mode output noise current, and cancels in the differential voltage output. This action can also reduce port isolation at the LO and IF ports. In the conventional mixer there is a direct noise current path between the output terminals during the time when both LO nodes are operating at the same time contributing noise at the IF frequency. Flicker noise is typically a bit higher in the double balance SW mixer, because of the multiple transconductance devices. These two types of noise contributions mentioned can be reduced by degeneration techniques if needed, but typically does not significantly affect the overall NF. The linearity of the double balanced SW transconductor mixer is in line with the conventional mixer. This fluctuates with the MOSFET internal properties due to biasing, and the switching of the LO amplitude.

Reference

[1] E. A. M. Klumperink, S. M. Louwsma, G. J. M. Wienk, and B. Nauta, “A Switched Transconductor Mixer,” *IEEE Journal of Solid State Circuits*, vol. 39, no. 8, pp.1231-1240, Aug 2004.

[2] L. Jin, H. Min, “A Low Noise High Linearity CMOS Upconversion Mixer,” in *ASICON ‘07 7th International Conference,* 2007, pp. 431-434.

CHAPTHER SIX: RESULTS

In the result section the ADS software was used in order to analysis and run circuit simulations for each of the mixer designs explained in the above sections. The simulation uses the TSMC 0.18 µm library. The MOSFET's that were used in the simulations are the 1.5 volt triple well RF n-channel MOSFET (nMOSFET) and RF p-channel MOSFET (pMOSFET). The sizes of the devices have a wide range of channel length and width, and are manipulated to achieve proper functionality. The selected resistances and capacitance that are used for these simulations are from the component library and are standard issue.

Single Balance Gilbert Cell Mixer Component Analysis

In order to verify how different component parameters affect a mixers design operation, the SB mixer was created given specific specifications given below in the table 1.

Table 1: SB Mixer Basic Parameter Specifications

Basic Parameter Specifications	**Values**
Biasing Voltage	VRF & VLO: 0.65 Volts and 0.69 Volts
RF Power	-40 dBm
LO Power	0 dBm
Supply Voltage	1.0 Volts
RF Frequency	900 MHz
LO frequency	1 GHz
Base Temp.	27° C

The basic mixer parameters that were modified are displayed above. Their various affects on the mixer design specifications (CG, Linearity, Port Isolation, and NF) will be shown in the following tables below.

Table 2: Mixer Specification with Change in Substrate Body

Parameters	**Original base b4 parameter change**	**VB=0**	**VB=1**	**VB=-1**
Gain	0.138	0.869	2.710	-16.232
IIP3 & OIP3	3.760/-20.377	3.766/-20.261	23.953/-19.533	-11.029/-23.374
LO/IF	-11.886	-11.846	-13.007	-15.890
RF/LO	-22.604	-22.833	-25.384	-22.476
RF/IF	3.079	2.648	-3.890	6.183
NF(DSB)	17.694	17.640	22.906	4.740

Table 3: Mixer Specification with Change in Supply Voltage

VDD	**1 Volts**	**2 Volts**
Gain	-1.170	3.659
IIP3 & OIP3	24.330/-21.165	23.721/-17.950
LO/IF	-16.842	-10.205
RF/LO	-27.010	-23.944
RF/IF	-3.046	-19.613
NF(DSB)	26.094	20.643

Table 4: Mixer Specification with Change in LO Power

LO power	**-5 dBm**	**5 dBm**
Gain	-25.200	5.330
IIP3 & OIP3	9.344/-33.418	5.359/-19.044
LO/IF	-23.357	-10.723
RF/LO	-33.533	-25.343
RF/IF	-20.895	7.708
NF(DSB)	20.121	22.605

Table 5: Mixer Specification with Change in RF Power

RF power	**-50 dBm**	**-30 dBm**
Gain	12.751	-7.420
IIP3 & OIP3	23.953/-19.533	23.953/-19.533
LO/IF	-13.007	-13.009
RF/LO	-17.273	-31.094
RF/IF	5.894	-13.066
NF(DSB)	22.906	22.891

Table 6: Mixer Specification with Change in RF Frequency

Freq	**RF=0.5 GHz**	**RF=5GHz**
Gain	2.562	-18.469
IIP3 & OIP3	24.237/-20.277	25.002/-18.713
LO/IF	-12.774	-18.023
RF/LO	-28.798	-24.836
RF/IF	-8.562	-32.639
NF(DSB)	22.985	19.827

Table 7: Mixer Specification with Change in Operation Temperature

Temp	**-40°C**	**125°C**
Gain	4.216	-2.541
IIP3 & OIP3	23.886/-19.249	7.988/-24.312
LO/IF	-12.142	-14.410
RF/LO	-20.188	-30.336
RF/IF	-11.666	-3.812
NF(DSB)	22.555	23.927

In summary, the above charts it was noted that the mixer design specifications are affected by these basic component changes. The information in these charts was verified using the single balance mixer design parameters equations shown in chapter two. Graphs outputs were also created in the simulator to show how each primary mixer parameter reacts as a function. The process aided in focusing on what particular section in the SB mixer affected the mixer design parameters via variable basic parameter sweeps. The sweep ranges were plus/minus 30 percent of the stated parameters values shown in Table 1.The functional graphs are given in the figures 11 - 44 below. For the RF and LO parameter sweeps, the specified percentage range is not large enough to collect data; therefore, the linearity functional graph for those sections are not shown.

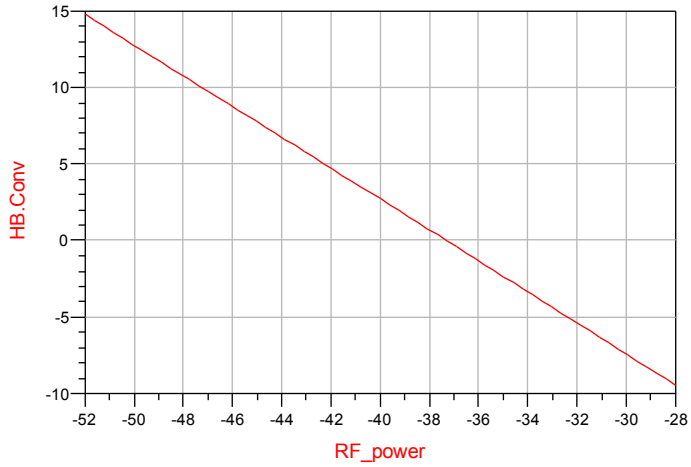

Figure 11: Conversion Gain as a function of RF Power sweep

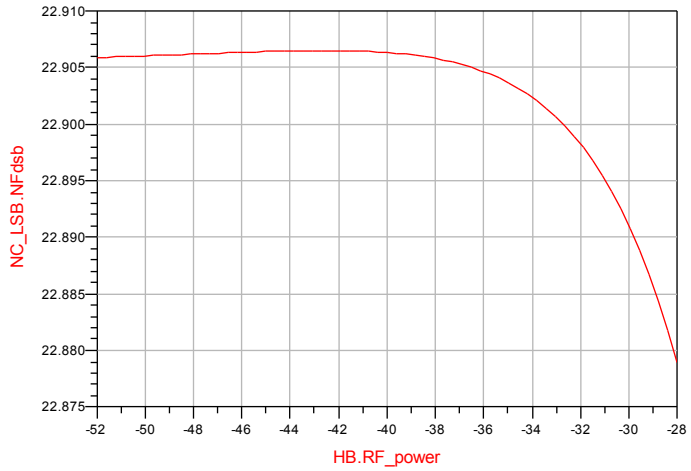

Figure 12: Noise figure as a function of RF Power sweep

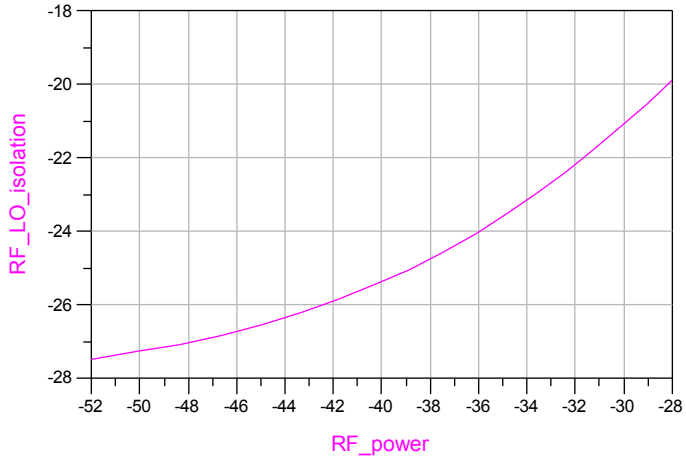

Figure 13: RF_LO port isolation as a function of RF Power sweep

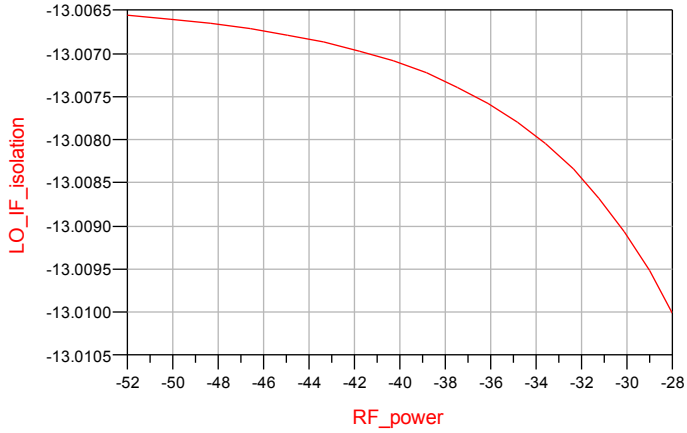

Figure 14: LO_IF port isolation as a function of RF Power sweep

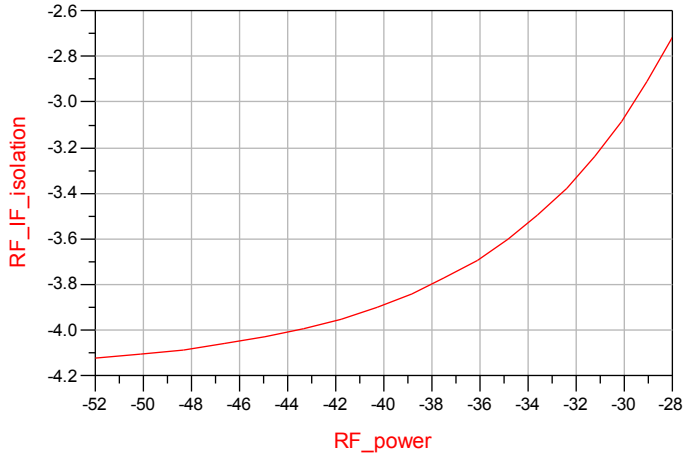

Figure 15: RF_IF port isolation as a function of RF Power sweep

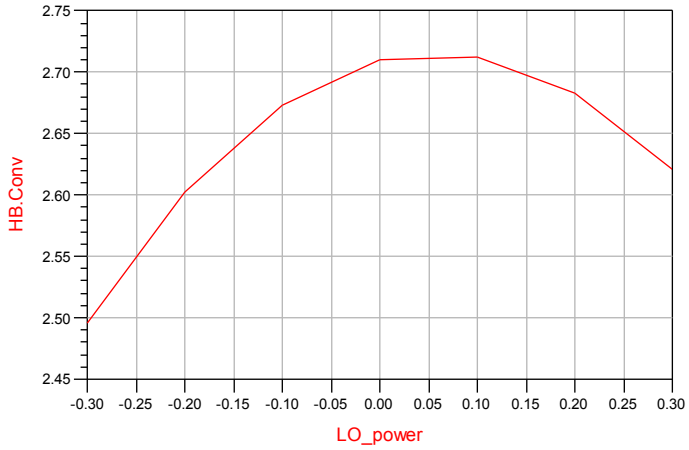

Figure 16: Conversion gain as a function of LO Power sweep

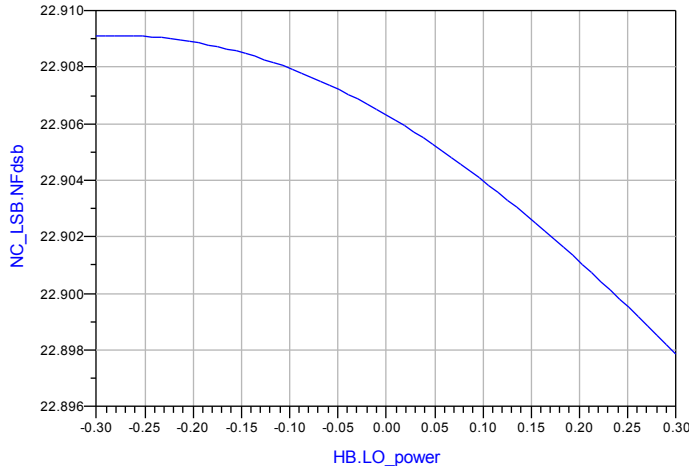

Figure 17: Noise figure as a function of LO Power sweep

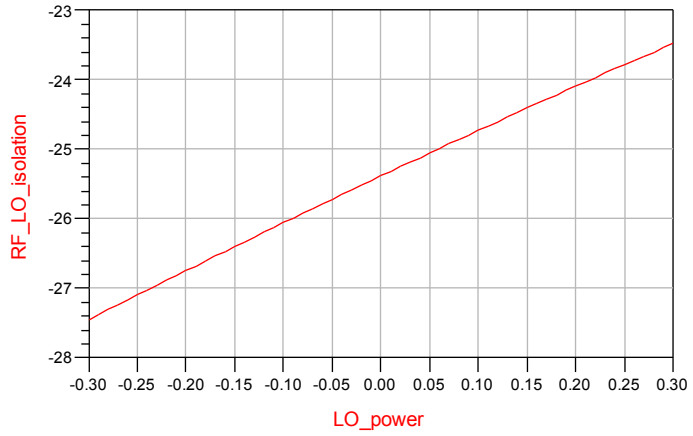

Figure 18: RF_LO as a function of LO Power sweep

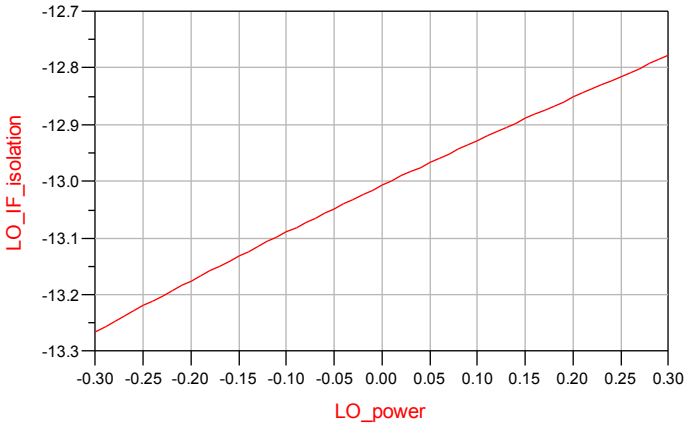

Figure 19: LO_IF as a function of LO Power sweep

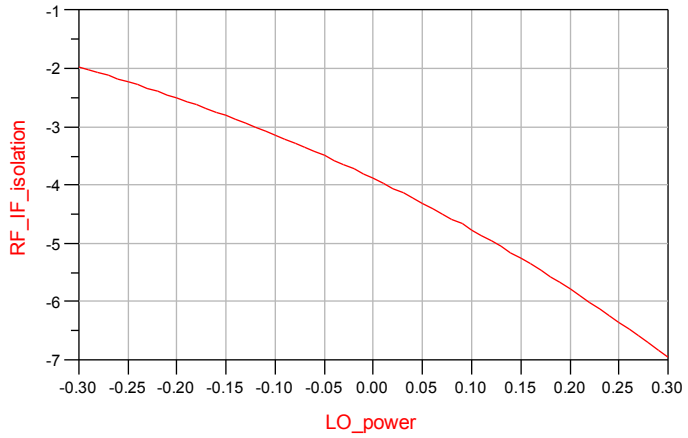

Figure 20: RF_IF as a function of LO Power sweep

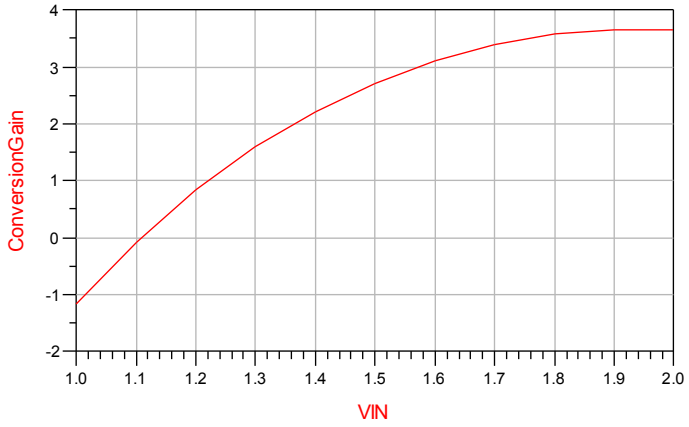

Figure 21: Conversion gain as a function of supply voltage

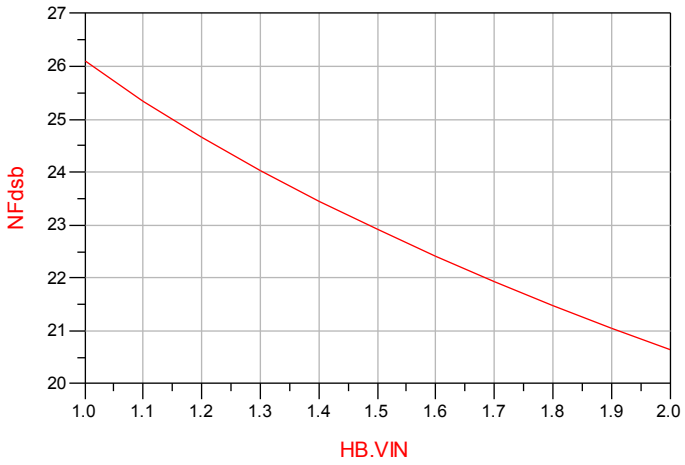

Figure 22: Noise figure as a function of supply voltage

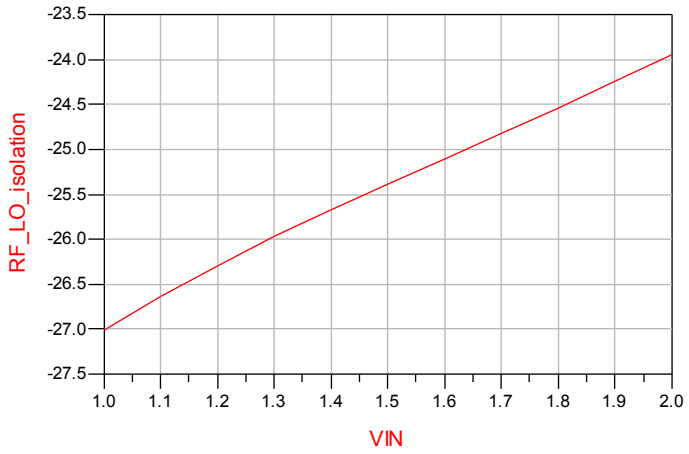

Figure 23: RF_LO port isolation as a function of supply voltage

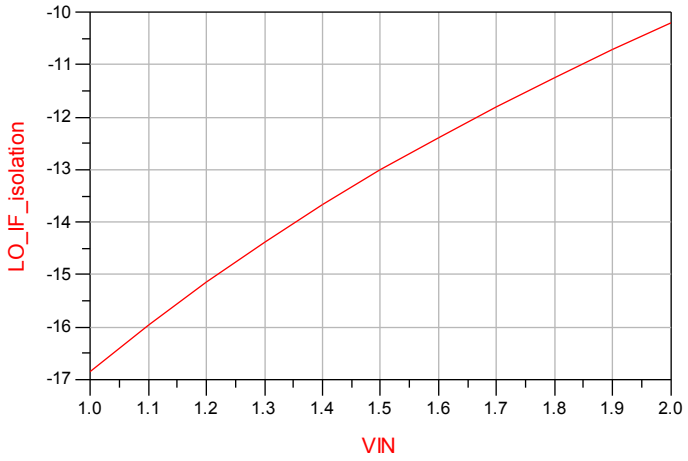

Figure 24: LO_IF port isolation as a function of supply voltage

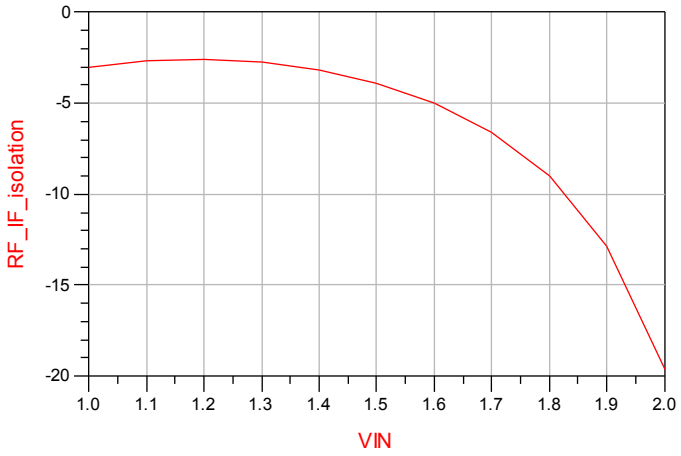

Figure 25: RF_IF port isolation as a function of supply voltage

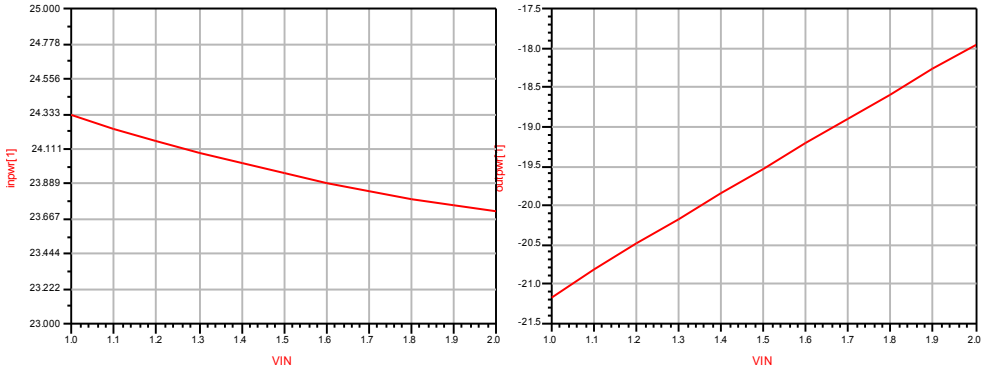

Figure 26: IIP3 & OIP3 as a function of supply voltage

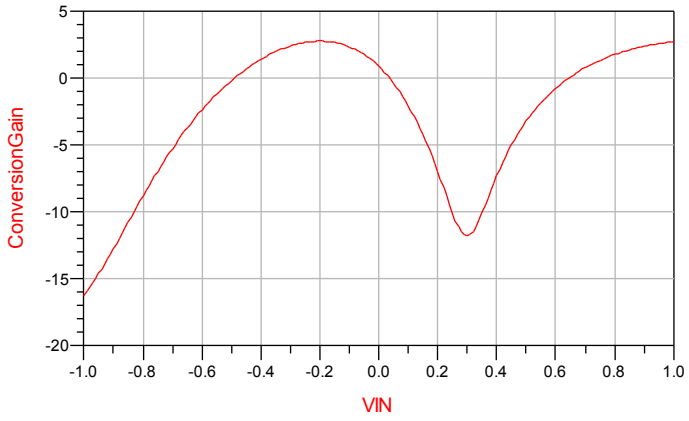

Figure 27: Conversion gain as a function of substrate biasing

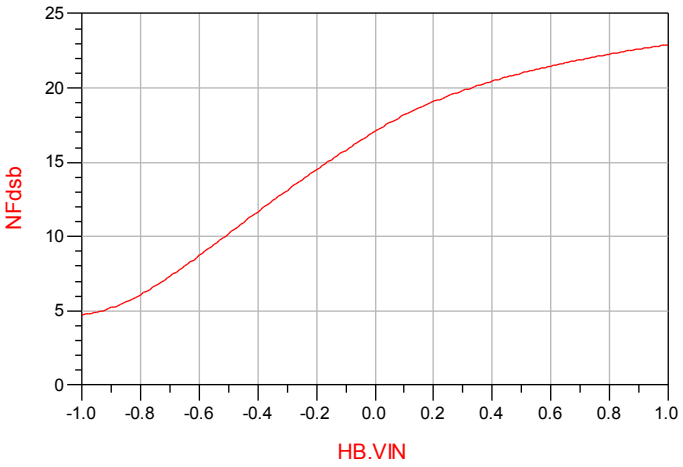

Figure 28: Noise figure as a function of substrate biasing

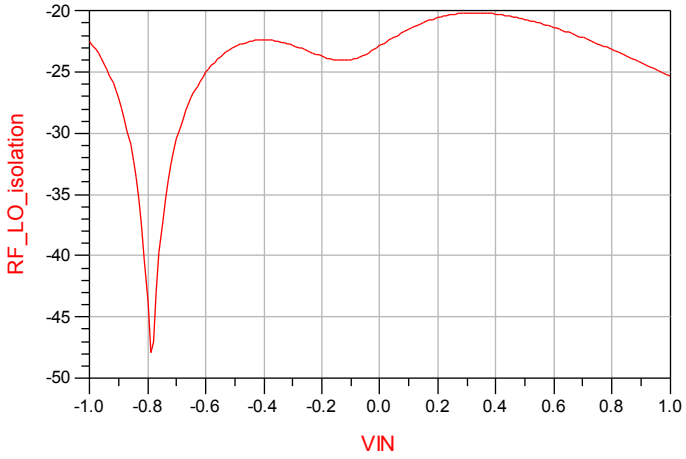

Figure 29: RF_LO as a function of substrate biasing

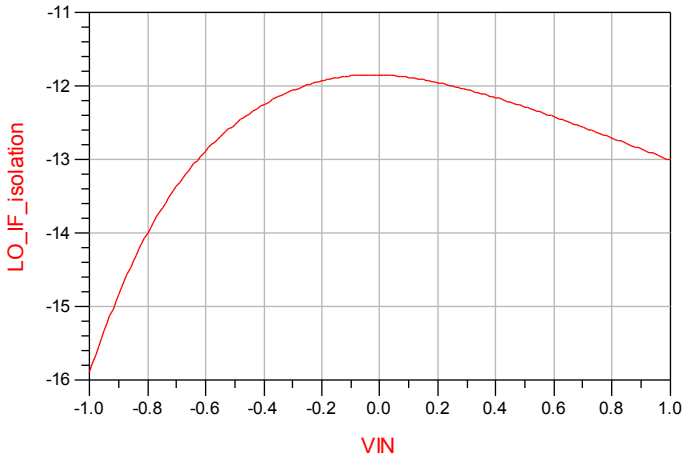

Figure 30: LO_IF as a function of substrate biasing

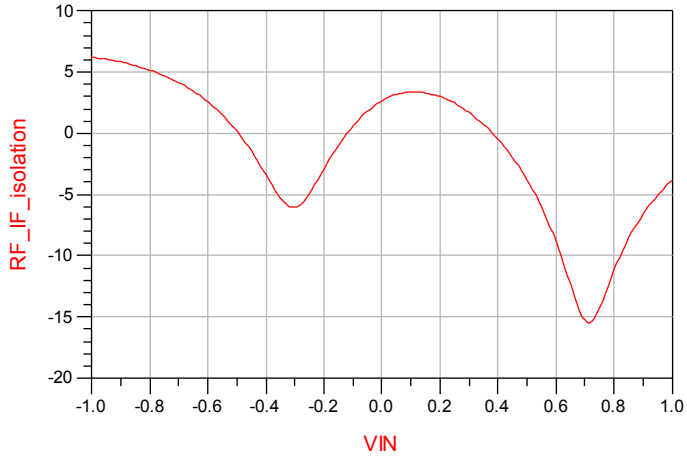

Figure 31: RF_IF as a function of substrate biasing

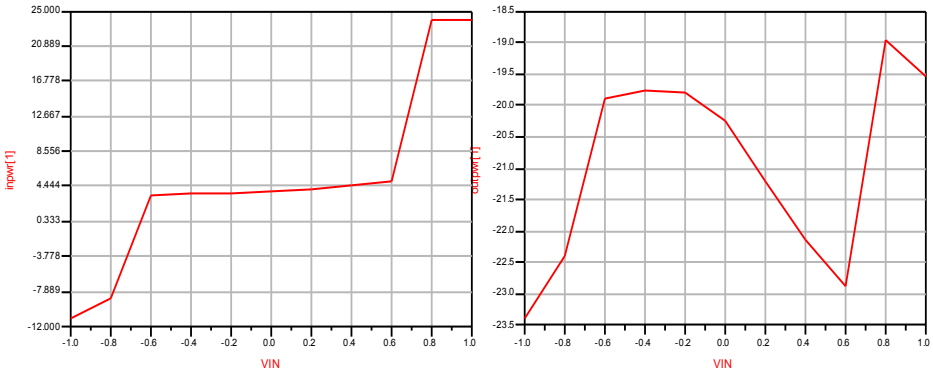

Figure 32: IIP3 & OIP3 as a function of substrate biasing

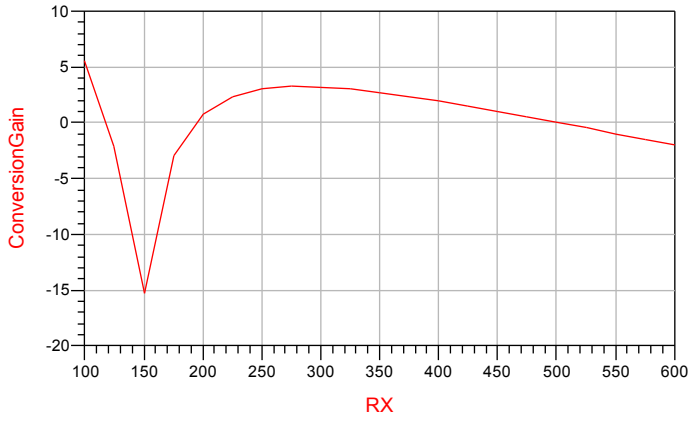

Figure 33: Conversion gain as a function of the load resistance

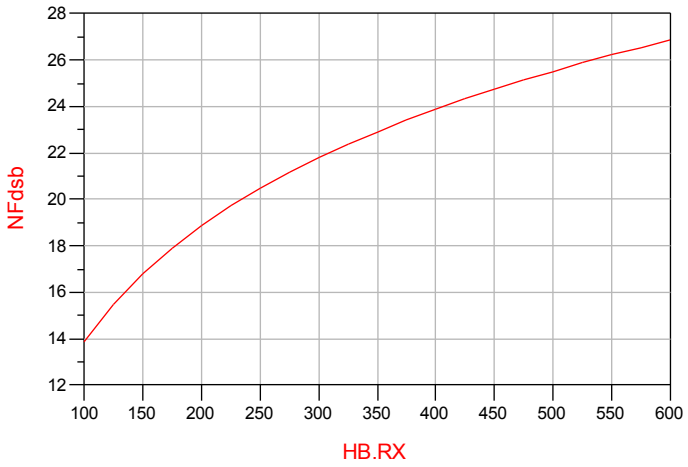

Figure 34: Noise figure as a function of the load resistance

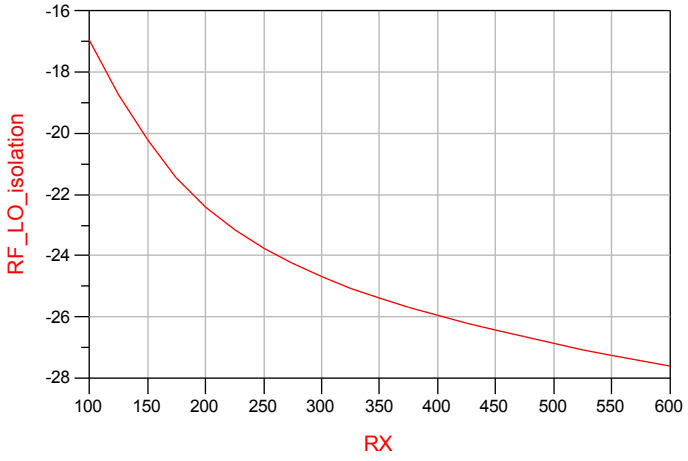

Figure 35: RF_LO as a function of the load resistance

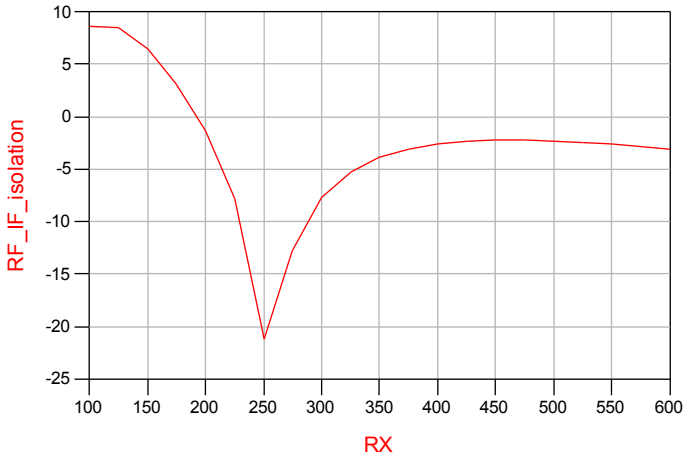

Figure 36: RF_IF as a function of the load resistance

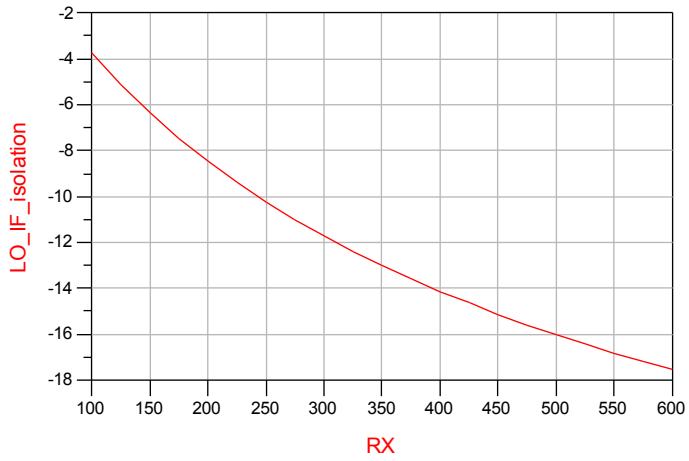

Figure 37: LO_IF as a function of the load resistance

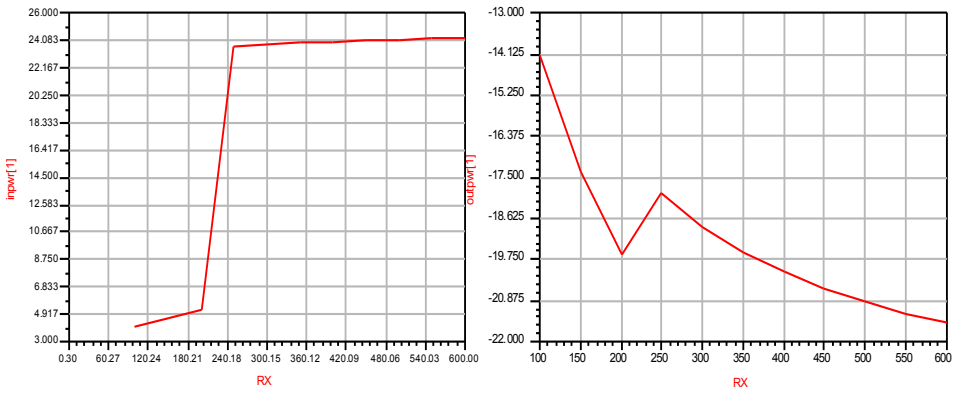

Figure 38: IIP3 & OIP3 as a function of the load resistance

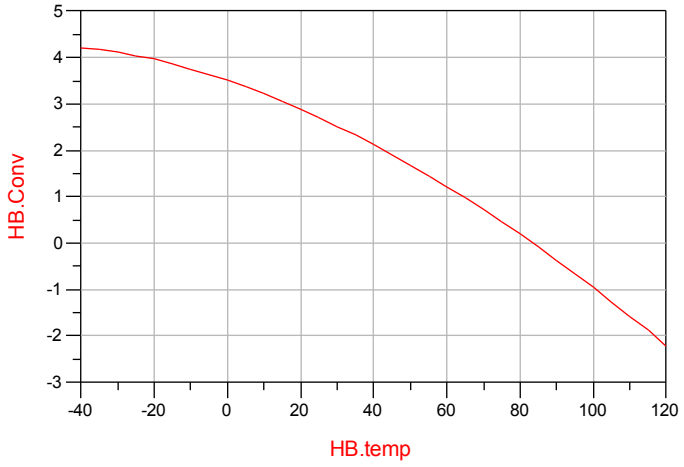

Figure 39: Conversion gain as a function of the operation temperature

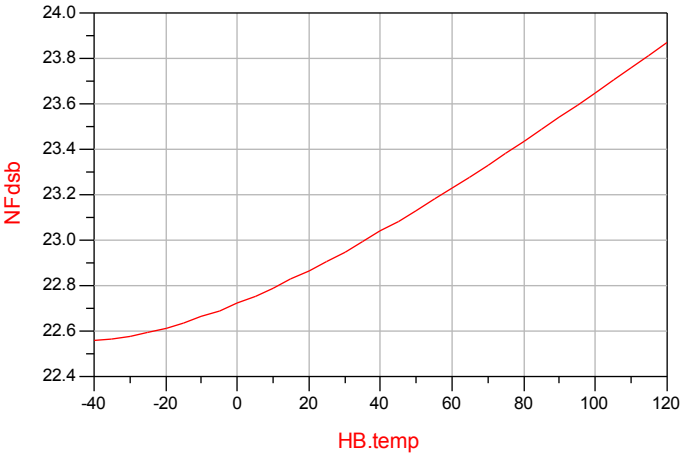

Figure 40: Noise figure as a function of the operation temperature

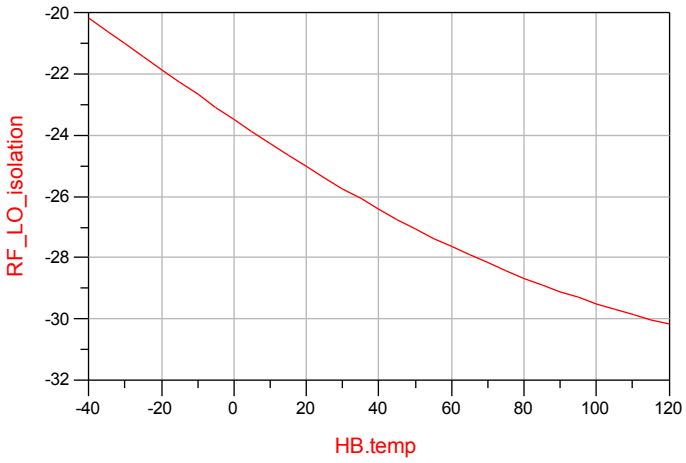

Figure 41: RF_LO as a function of the operation temperature

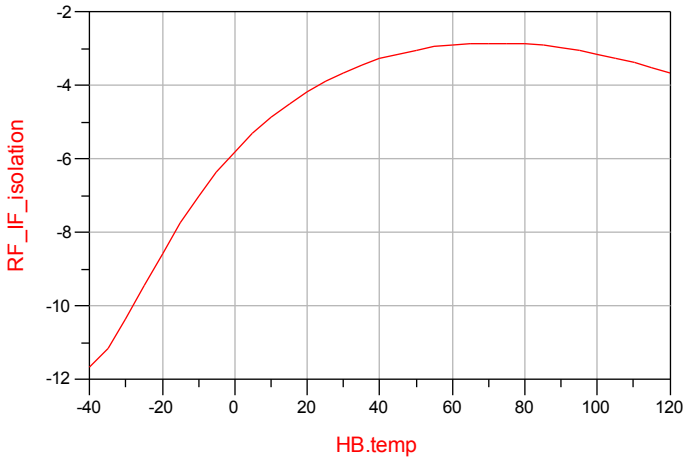

Figure 42: RF_IF as a function of the operation temperature

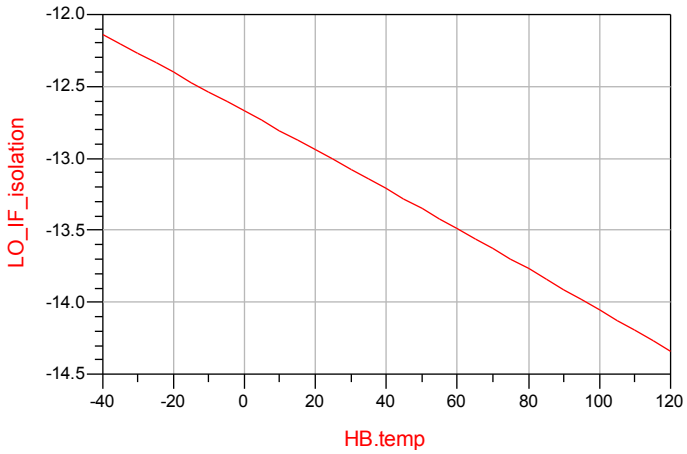

Figure 43: LO_IF as a function of the operation temperature

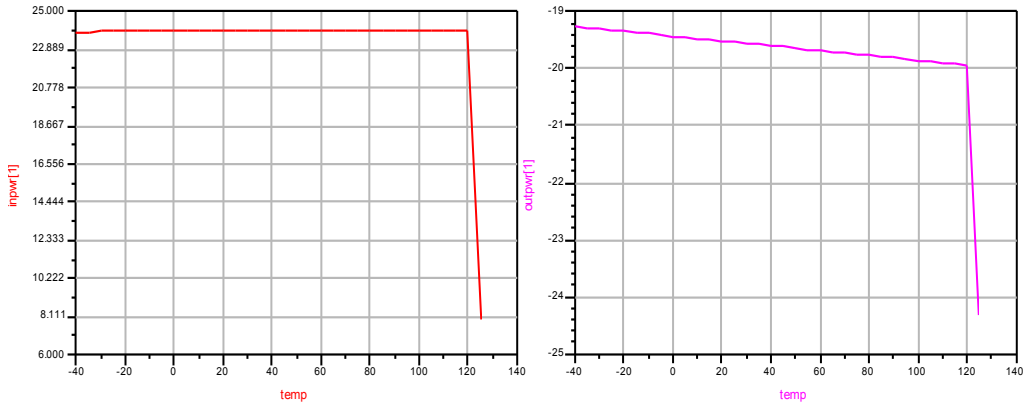

Figure 44: IIP3 & OIP3 as a function of the operation temperature

Single Balance Gilbert Cell Mixer Design Parameters Simulated Results

In the simulated mixer picture shown from chapter 2, the nMOSFET channel length was 0.35 µm and its channel width was 300 µm. The load resistances were 350 Ω, and the other specifications are the same as was labeled earlier. After deciphering how the SB down conversion mixer operates, the design specifications from the simulation were found in relation to the data based on the driver current from [1]. A summary of the ADS simulated mixer design parameters in respect to important components in the mixers design are shown in the following graphs and the values are summarized in table 8.

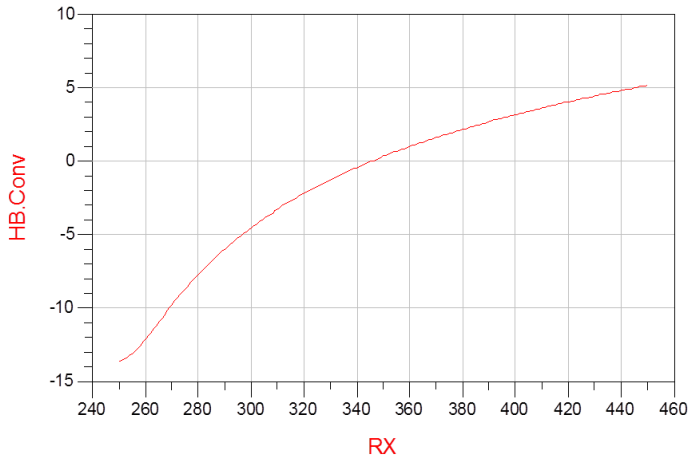

Figure 45: SB Gilbert Cell Mixer-Conversion Gain vs. Load resistance

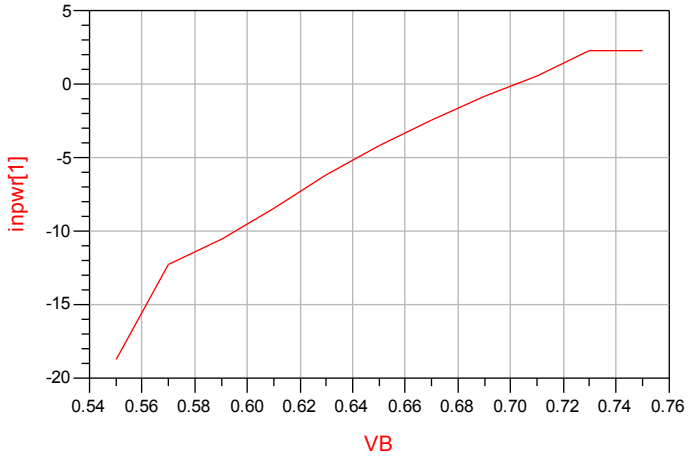

Figure 46: SB Gilbert Cell Mixer-IIP3 vs. Gate voltage

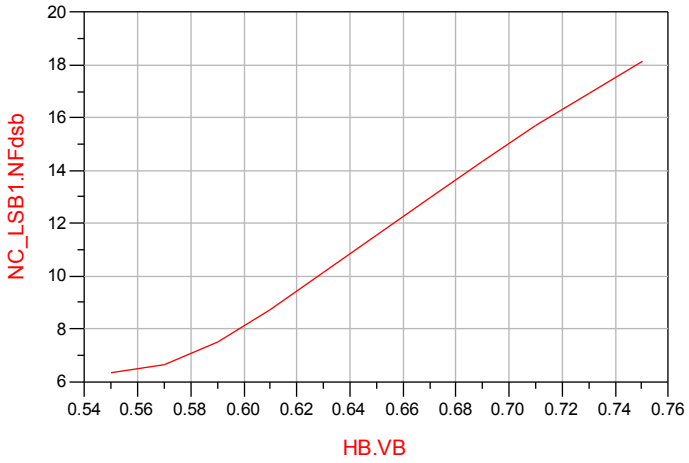

Figure 47: SB Gilbert Cell Mixer-Noise Figure vs. Gate voltage

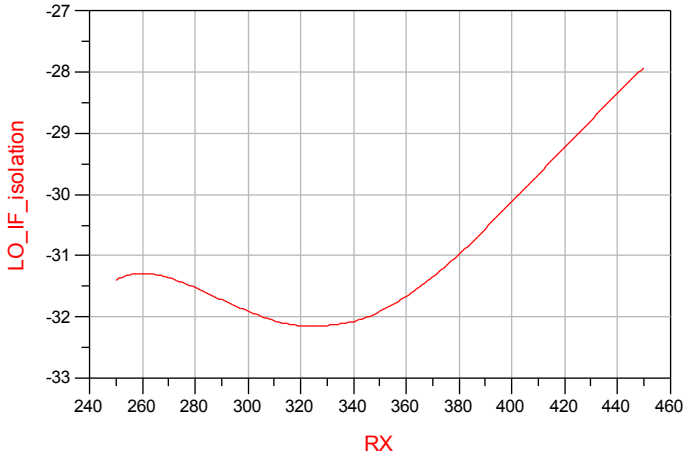

Figure 48: SB Gilbert Cell Mixer-LO/IF isolation vs. Load resistance

Table 8: SB Gilbert Cell Mixer Simulated Data

Design Parameters	**Simulated Values**
Driver Current	4.002 mA
Conversion Gain	0.337 dB
IIP3	-4.189 dBm
Noise Figure	11.547 dB
LO/IF Isolation	-31.912 dBm
Power Consumption	4.002 m

Single Balance Charge Injection Mixer Parameters Simulated Results

This design consisted of the injected current pMOSFETs channel length and width of 0.35µm and 64µm. The load stage resistance value is 700Ω, while the

nMOSFETs and basic parameters are the same as given in the SB Gilbert cell design. In the charge injection design due to the implemented current in the mixer the CG, linearity, and NF were all improved while using approximately the same power. The port isolation is a bit lower, because the ratio between the driving current and injected current is only 40.45%, and not equal in value. The charge injection mixer parameters figures, and summation chart are shown below.

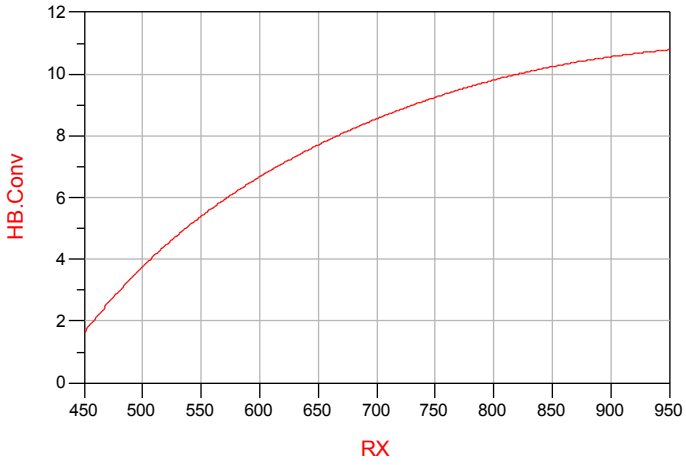

Figure 49: SB Charge Injection Mixer-Conversion Gain vs. Load resistance

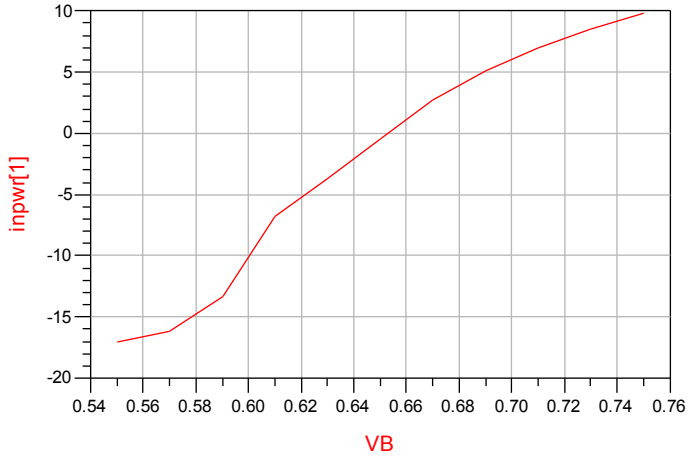

Figure 50: SB Charge Injection Mixer-IIP3 vs. Gate voltage

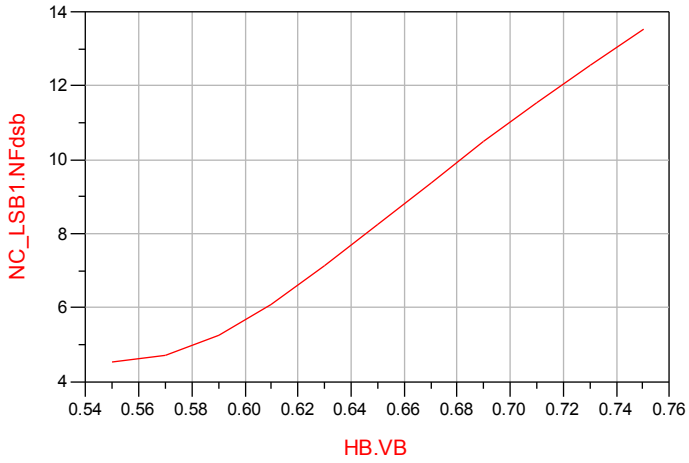

Figure 51: SB Charge Injection Mixer-Noise Figure vs. Gate voltage

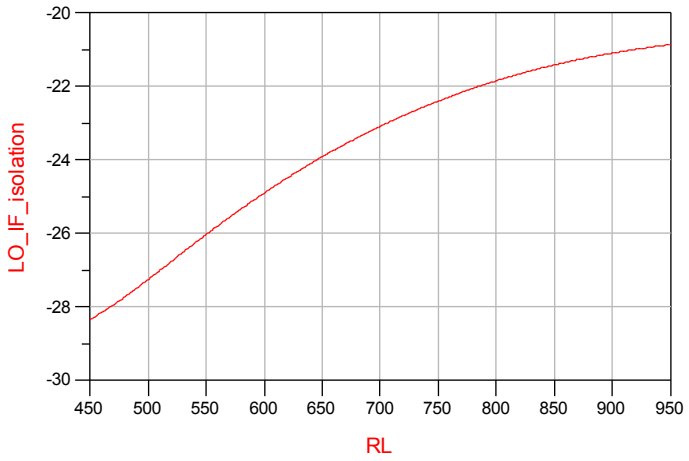

Figure 52: SB Charge Injection Mixer-LO/IF isolation vs. Load resistance

Table 9: SB Charge Injection Mixer Simulated Data

Design Parameters	**Simulated Values**
Driver Current / Injected Current	4.0 mA / 1.618 mA
Conversion Gain	8.552 dB
IIP3	-0.458 dBm
Noise Figure	8.244 dB
LO/IF Isolation	-23.090 dBm
Power Consumption	4.0 mW

Double Balance Gilbert Cell Mixer Design Parameters Simulated Results

In the DB mixer design there shows a higher CG, linearity, and port isolation then the SB mixer. The tradeoff is having a higher NF and power consumption, because of

the increase of transistors and a higher supply voltage. In this mixer design the transistors sizes in both the switching and driving stages are 0.35µm / 200µm and 0.35µm / 300µm respectfully. The load stage resistance is 300Ω, while the supply voltage is 1.3 Volts. The other basic specifications are the same as previously stated in the first table. In figure 53 one can see the trade off of gain due to an increase in load resistance.

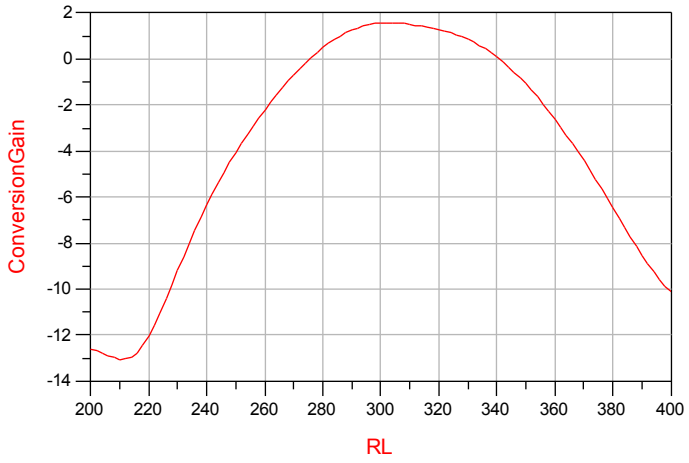

Figure 53: DB Gilbert Cell Mixer-Conversion Gain vs. Load resistance

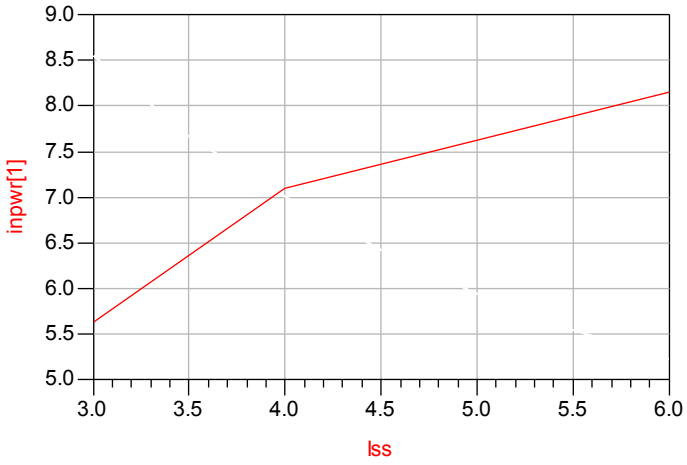

Figure 54: DB Gilbert Cell Mixer-IIP3 vs. Biasing current

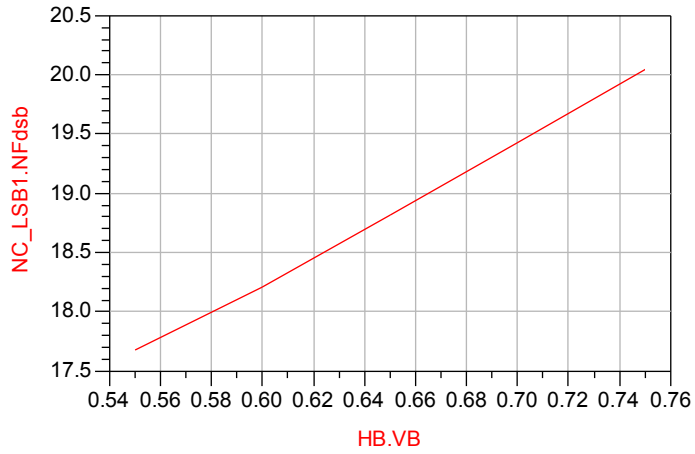

Figure 55: DB Gilbert Cell Mixer-Noise Figure vs. Gate voltage

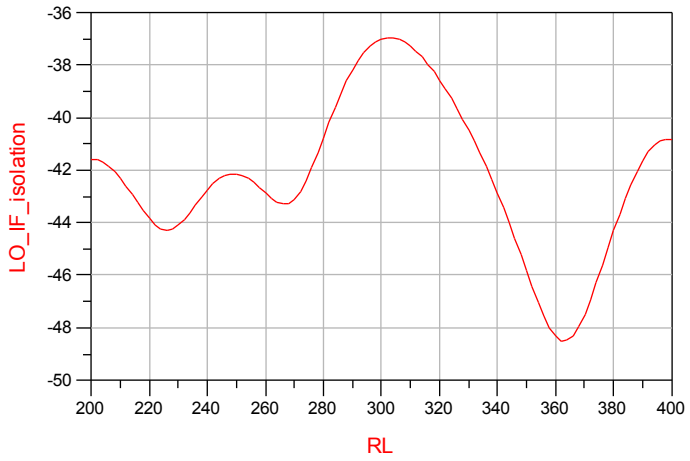

Figure 56: DB Gilbert Cell Mixer-LO/IF isolation vs. Load resistance

Table 10: DB Gilbert Cell Mixer Simulated Data

Design Parameters	**Simulated Values**
Driver Current	4.0 mA
Conversion Gain	1.564 dB
IIP3	7.004 dBm
Noise Figure	19.028 dB
LO/IF Isolation	-36.565 dBm
Power Consumption	5.2 mW

SB Switched Transconductance Mixer Design Parameters Simulated Results

In the SW mixer the inverter length and width sizes are 0.35µm / 300µm for the PMOS, and 0.35µm / 180µm for the NMOS. The driver stage NMOS transistors size are same size as the inverters PMOS. The load stage resistance is given as 700Ω, while

the basic mixer parameters remained the same. In the graphs below it is shown that the SW mixer curves follow the curves of the SB Gilbert Cell, because this technique was applied to the SB design. In the area for the NF, there is a slight steep curve, because the switching is non-ideal, and many parameters were kept the same to show a fair comparison between the mixer topologies.

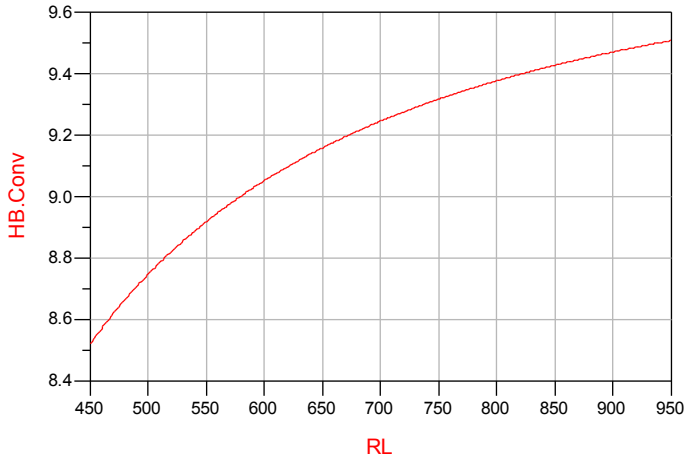

Figure 57: SB Switched Transconductance Mixer-Conversion Gain vs. Load resistance

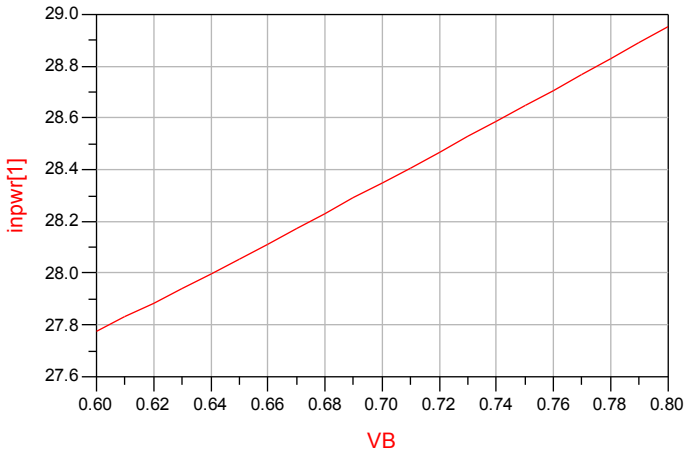

Figure 58: SB Switched Transconductance Mixer-IIP3 vs. Gate voltage

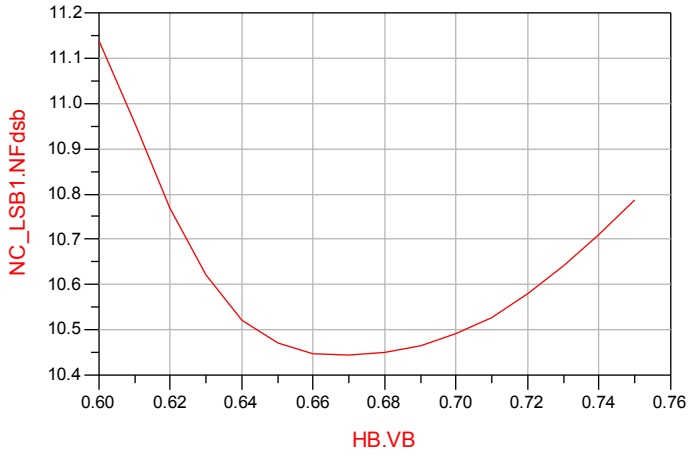

Figure 59: SB Switched Transconductance Mixer-Noise Figure vs. Gate voltage

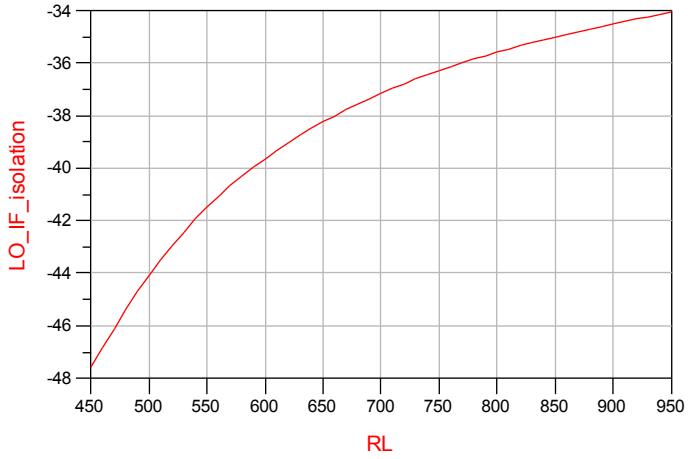

Figure 60: SB Switched Transconductance Mixer-LO/IF isolation vs. Load resistance

Table 11: SB Switched Transconductance Mixer Simulated Data

Design Parameters	**Simulated Values**
Driver Current	1.084 mA
Conversion Gain	9.246 dB
IIP3	28.074 dBm
Noise Figure	10.431 dB
LO/IF Isolation	-37.153 dBm
Power Consumption	1.084 mW

Mixer design topology overall results

The table below shows all the mixer topologies with their respective important design specifications. After viewing this, one can make the conclusion that the switched transconductor design is the best design. It has the best CG, linearity, port isolation and power consumption while having a competitive NF. The primary reason why this

topology is the best design is, because the mixer was created to have competitive results that operate at a lower supply voltage using a digital and analog (mixed) setup.

Table 12: Overall Mixer Design Topologies Results

Topology	**Gain**	**IIP3**	**Noise Figure**	**LO/IF Isolation**	**Power Consumption**
Single Balance	0.337 dB	-4.189 dBm	11.547 dB	-31.912 dBm	4.002 mW
SB Charge Injection	8.552 dB	-0.458 dBm	8.244 dB	-23.090 dBm	4.0 mW
Double Balance	1.564 dB	7.004 dBm	19.028 dB	-36.565 dBm	5.21 mW
Switched Transconductance	9.246 dB	28.074 dBm	10.431 dB	-37.153 dBm	1.084 mW

CHAPTHER SEVEN: CONCLUSION

In this passage the CMOS active RF mixer has been studied, analyzed, and simulated using four different design topologies. These designs were constructed using ADS software using basic setup specifications. In the SB Gilbert cell the basic parameters values were ranged to better understand how the mixer reacts to changes in the three main stages: transconductance or driver stage, switching stage, and load stage. The second design used an injected method, while the third design used a double balanced. In the last design a more modern method was applied to compensate for the decrease in transistors size, as the demand of CMOS technology advances. These mixers important mixer design specifications were then simulated and checked to the appropriate analytical equations and design operations. After this the mixer specifications were taken and compared.