SYNCHRONOUS COMMUNICATION SYSTEM FOR SAW SENSOR INTERROGATION

by

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ABSTRACT

During past two decades a variety of SAW based wireless sensors were invented and research is still in progress. As different frequencies, varied bandwidths, coding techniques and constantly changing post processing algorithms are being implemented, there is a constant need for a universal and adjustable synchronous communication system able to interrogate new generations of SAW sensors.

This thesis presents the design of a multiple FPGA based communication system with an operational frequency range of 450MHz-2.2GHz capable of producing user programmed modulated signal. The synchronous receiver is designed to have interchangeable chip, replacement of which would allow adjustment of the receiver's bandwidth. Within this paper the performance of the system is only evaluated at 915MHz centered 20MHz bandwidth region.

An OFC temperature sensor was interrogated. Post-processing algorithms, measurement results, and proposals for the future use of the system are presented. Detailed overview of the structure and performance of every functional block along with design considerations are analyzed. Previously designed Matlab based software was adapted for post processing of the received signal. New software with simplified GUI was designed for programming of the desired signal.

ACKNOWLEDGMENTS

First I would like to thank my adviser Dr. Malocha for his continuous support and patience. I am grateful to him for allowing me to pursue the topic of research that I have always wanted to be a part of. His guidance and encouragements gave me every opportunity for success in my graduate studies at University of Central Florida.

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Finally, my endless gratitude goes to my mother and the rest of my family for their love and support. It has been a long road and they supported me through the best and the worst of time.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS

ADC	—	Analog to Digital Converter
CMOS	—	Complimentary Metal-Oxide Semiconductor
DDS	—	Direct Digital Synthesizer
DSP	—	Digital Signal Processing
DUT	—	Device Under Test
EPROM	—	Erasable Programmable Read Only Memory
FCC	—	Federal Communication Commission
FPGA	—	Field-Programmable Gate Array
GUI	—	Graphical User Interface
HEX	—	Hexadecimal numbering system
ISM915	—	Industrial Scientific Medical 915MHz
IF	—	Intermediate Frequency
LO	—	Local Oscillator
MSPS	—	Mega Samples Per Second
QSS	—	Quantization Step Size
NF	—	Noise Figure
OFC	—	Orthogonal Frequency Coding
PA	—	Power Amplifier
PCB	—	Printed Circuit Board
PLL	—	Phase-Locked Loop
RF	—	Radio Frequency

SAW	—	Surface Acoustic Wave
SMA	—	Sub-Miniature connector version A
SNR	—	Signal-to-Noise Ratio
SPI	—	Serial Peripheral Interface
TCXO	—	Temperature Compensated Crystal Oscillator
VCO	—	Voltage Controlled Oscillator
USB	—	Universal Serial Bus

CHAPTER 1: INTRODUCTION

As a system designer, engineer has to solve complex task consisting of analysis of required functionality of final product and finding the best cost effective design solution. To simplify the task, the system can be broken into smaller functional blocks (Figure 1) and then studied further.

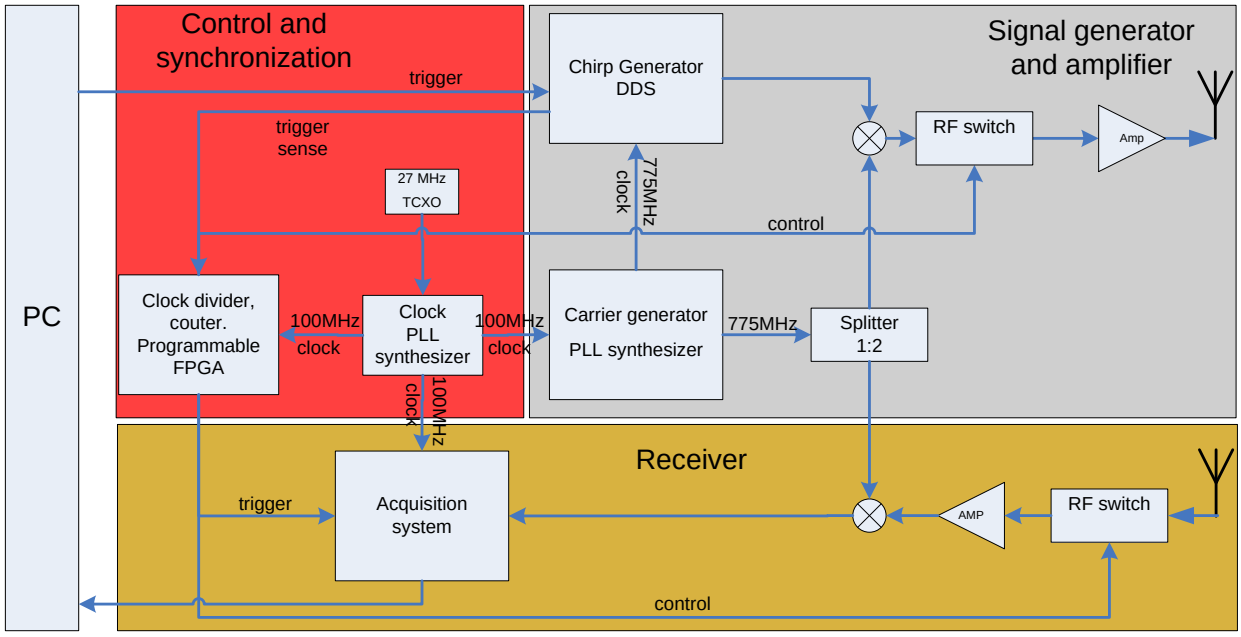


Figure 1: Simplified block diagram of the designed communication system

Detailed overview of the system will be given in Chapter 2. Results of the measurements of the signal will be presented alone with its mathematical simulation at every stage where transformation of the signal occurs. Every functional block of the system, as in Figure 1, will be described in a separate chapter in this thesis.

Design of the signal generator and amplifier will be given in Chapter 3. Details of digital frequency generation and resulting signal imperfections will be studied. Separate section at the end of the chapter will contain information on compliance with chosen radio band FCC regulations.

Chapter 4 covers the design of the system clock and the synchronization system. Proper synchronization of operation of the transmitter with the receiver has a tremendous effect on post processing results. A timing diagram will be presented and various system delays will be calculated and explained. Worst case scenario synchronization error will be estimated.

Chapter5 will describe the receiver. Minimum detectable signal will be calculated and maximization of the range of operation and signal-to-noise ratio will be discussed. Chapter 5 also contains the details of operation of the IC and its effect on post processing of the received signal.

In Chapter 6, an overview of the nature of the measurements and methods of digital signal processing will be provided.

After analysis of the experimental results in Chapter 7, recommendations for system modification and a conclusion will be given in Chapter 8.

Every design decision within this thesis was influenced by two key factors: available time and budget as illustrated on Figure 2.

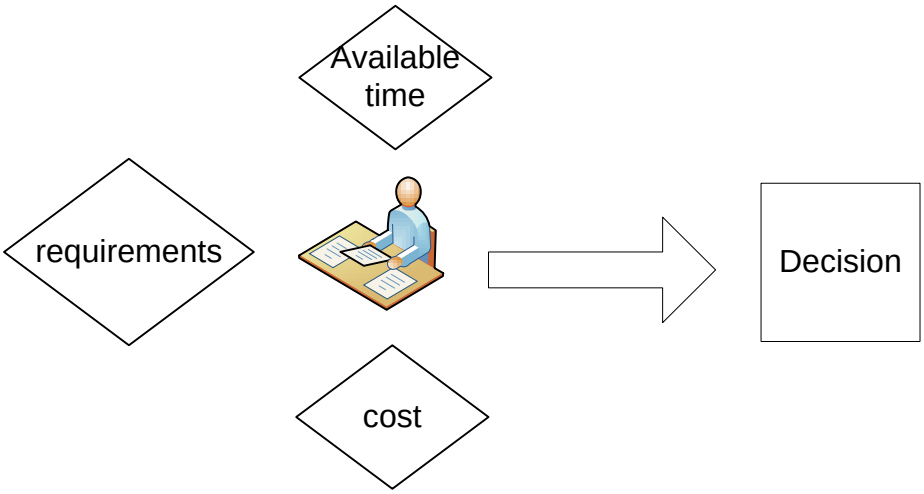


Figure 2: Illustration of the decision making process.

A quick overview of available technology is given in the sections where the author had to choose certain part over another.

CHAPTER 2: SYSTEM OVERVIEW

The communication system was designed to operate on the center frequency of 915MHz and a bandwidth of 20MHz. The maximum output power of the transmitter was limited to below 1W to qualify to Federal Communication Commission (FCC) ISM915 regulations. The system was equipped with an internal power supply and USB connector for data transmission and packaged into a shielded case, allowing the interrogator to be a mobile plug-n-play device. The communication system was designed to have an adjustable frequency. The system, composed of multiple functional blocks, contains five boards equipped with USB-to-SPI interface, allowing for easy reprogramming. All filters used in the system were equipped with standard SMA connectors for minimum hardware interaction if change is necessary. Within this thesis, the performance of the system will only be evaluated over center frequency 915MHz and bandwidth of 20MHz.

The transmitter center frequency is 915MHz with a 26MHz bandwidth, generating a linearly frequency modulated signal (stepped up chirp) with the peak output power of +26dBm. Frequency modulation is performed using a fast frequency hopping direct digital synthesizer (DDS). The DDS outputs a 140MHz centered up-chirp signal with the bandwidth of 36MHz. There are total of 7 chips, each having a bandwidth of 5.382MHz and individual chip lengths τ_{dwell} of 186ns. The entire chirp length is given by the number of chips times the chip length, yielding a pulse with a 1.3us duration. The frequency modulated signal is intentionally designed to be wider in frequency and longer in time than is needed, due to hardware constrains. SAW filters are used to limit the time and the bandwidth of the chirped output signal. The signal is then mixed with a 775MHz local oscillator (LO) frequency, generated with the phase lock loop

(PLL) frequency synthesizer yielding output signal with a center frequency of 915MHz and bandwidth of 36MHz. Two series ISM915 SAW filters with center frequency of 915MHz and bandwidth of 26 MHz filter the chirp signal within the ISM915 band. The signal is input to five cascaded amplifiers, delivering a total of 48dB of gain with a maximum output power of +26.5 dBm. A patch antenna with approximately 2dB of gain was used for the project. A block diagram of the transmitter within the system is presented on Figure 3.

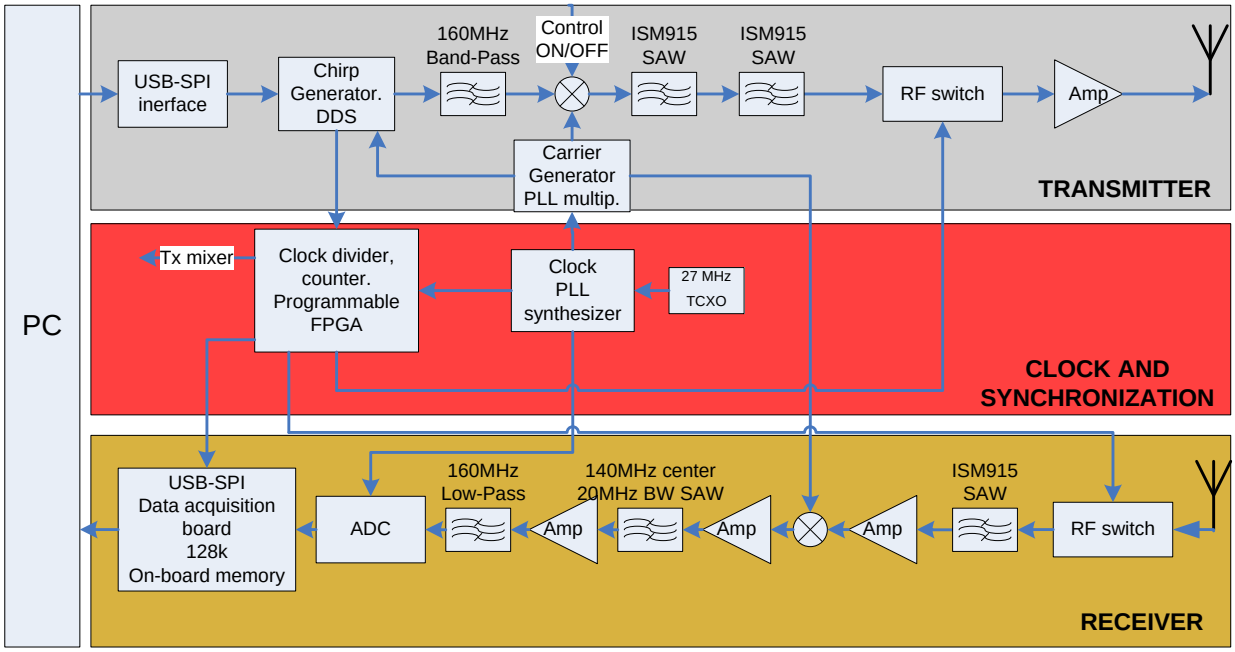


Figure 3: Detailed block diagram of the designed communication system.

The transmit interval, which is approximately 1usec long, is followed by the receive interval, with a short delay consisting primarily of system delay. Two antennas are used since they provide for better isolation for Rx from Tx operation. The communication system

transmitter and receiver are time duplexed, one is operating while the other is disabled, and vice versa, the communication system oprates in a switching mode.

The synchronization system, in Figure 3, uses a common clock providing all the circuitry with clock signal for timing and counting. The clock is derived from the 27MHz temperature controlled crystal oscillator and multiplied on the PLL frequency generator to output 80MHz. Obtained master clock is supplied to the Rx ADC, control system, and PLL frequency synthesizer for further multiplication. A carrier generator, PLL frequency synthesizer is deriving 775MHz signal from the master clock. Carrier frequency is used to mix the signal up from the intermediate frequency and to mix the signal back to the IF on the receiver. The carrier signal is also used as a clock signal for the DDS.

An FPGA based control system provides synchronous switching by dividing a common clock frequency supplied to the chip. The control system is triggered by the signal ‘begin frequency sweep’ coming from the DDS. The transmitter mixer is then turned ON by applying a digital ‘1’ to the appropriate pin of the mixer-IC. The Tx switch goes ON within one clock cycle when the frequency sweep of the DDS is at the desired frequency. A SAW filter propagation delay was measured and included into calculations of the switching time diagram. Both mixer and Tx switch triggers go OFF at the end of transmission interval. The timing diagram is displayed on the Figure 4 and discussed in more details in Chapter 4.

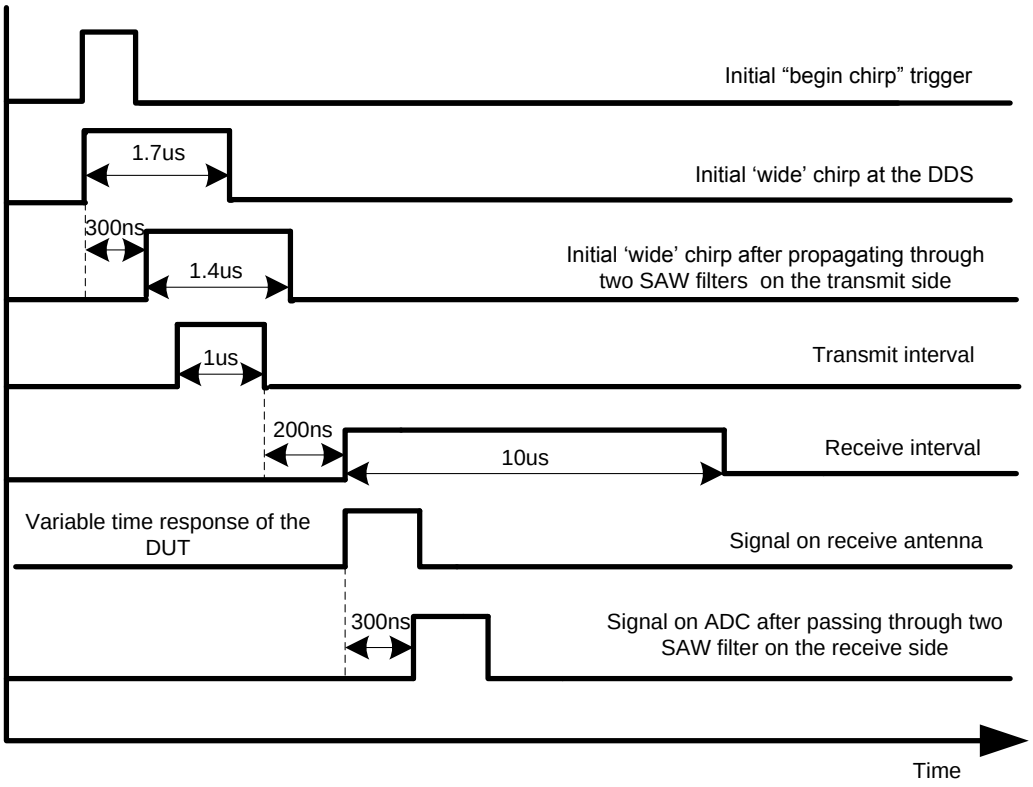


Figure 4: Switching and timing diagram of the designed system.

Transmission is followed by a pause, needed for possible oscillation to fade away on the Tx side. The receive interval is then triggered. The Rx switch is turned ON first. The propagation delay of two SAW filters on the Rx side was measured and included into the time switching diagram. The signal triggering the ADC to start sampling is turned ON next. At the end of the Rx period both triggers are turned OFF. Rx cycle is followed by a pause needed for triple transit or any possible oscillations to fade away. The Tx-Rx cycle is then repeated.

The device under test (DUT) – a wide band, 915MHz centered, orthogonal frequency coded (OFC) temperature sensor, was used as a measurement device. The tag’s frequency

response, code and other parameters are known. The temperature sensor modulates the received signal and transmits it back to the interrogation unit via an attached patch antenna.

A sensor response is received by the system with the antenna similar to the one used on the transmitter side. A signal passes through the ISM915 SAW filter before it is supplied to the first cascade of an amplifier shown in Figure 3. The filtered and amplified signal is then supplied to the down-mixer, where it is mixed down to the intermediate frequency (IF) with the same LO signal of 775MHz that was used for up-conversion. A produced IF signal is amplified and filtered two more times before it is supplied to the analog-to-digital converter (ADC). After filtering, the signal has a center frequency of 140MHz and the bandwidth of 20MHz. The maximum sampling rate of the chosen ADC is 145 mega samples per second (MSPS), therefore, to satisfy the Nyquist criteria, the band-pass sampling (or under-sampling) algorithm is implemented. The sampling rate of 80MHz (or MSPS) was chosen to yield aliasing-free conditions for the received signal.

A sampled signal is captured by the ADC, the data is sent over the bus to the computer, and the data file is processed with the Matlab mathematical software. The received signal data is reconstructed and de-convolved with the down-chirp simulated signal. The product of convolution is then correlated against a theoretically derived matched filter in order to extract the temperature readings from the sensor. Software was previously developed and adapted for use with the new system and is not a portion of this thesis.

New hardware GUI's and data acquisition software was designed for easy user reconfiguration of the operational frequency of the system and for programming the desired modulation of the signal.

CHAPTER 3: TRANSMITTER

The transmitter has been designed to satisfy the following requirements:

- To have an adjustable, programmable frequency without hardware modification
- To allow fast frequency hopping and to allow radar chirp generation
- To be synchronized with the rest of the circuitry i.e. operate on the same clock
- To output up to 1W of power
- To comply with FCC ISM915 regulations

The following chapter is a technological trade study conducted with the intent to find the best design solution. This chapter will explain the operational and technical characteristics of the device as it is currently configured.

3.1 Signal generator

Generally, digital frequency synthesizers can be divided in three groups:

- Direct.

Direct synthesizers are composed of logical gates, and utilize digital algorithms to generate lower frequencies with fine frequency increments. The output bandwidth is usually limited to ½ or often to ¼ of the clock's frequency. With current technology, in order to generate a 915MHz signal, the operational frequency of the DDS would have to be between 2GHz and 4GHz, making the production of such a device prohibitively expensive, bulky and power inefficient. Direct digital synthesizers (DDS) are available for output frequencies up to 1GHz.

- Indirect.

Indirect synthesizers utilize a phase-locked loop technique (see section 3.1.2) to multiply an input signal. On the current market there are chips with an output of up to 10GHz. However, because it takes up to 200 clock cycles for typical PLL chip to "lock" on a frequency, frequency hopping speeds are inadequate.

- Hybrid.

Hybrid frequency synthesizers employ both of the above techniques but are very costly. Therefore they are primarily built for specific applications. The output frequencies of hybrid devices can reach up to 40GHz.

For reasonable price, and with the intent to imitate a cellular phone communication system, I chose to use a DDS for an IF synthesis and PLL synthesizer for a carrier generation.

3.1.1 IF generator

With extreme miniaturization of the digital IC, it is often difficult, if not impossible, to lay out a double layered PCB for laboratory fabrication. An evaluation board with AD9956, advanced DDS from Analog Devices was purchased for the project. The generator DDS does not have an EEPROM memory, therefore the IC's memory has to be written every time upon power-up. Communication with the chip is accomplished via USP-to-SPI interface. The software, necessary for programming of the part, was designed based on the Visual Basic source code provided by manufacturer. The software is compiled in one executable file, which, once launched, independently updates all registries of the DDS with preprogrammed information. If

generation of the frequency or the waveform different than discussed in this thesis is desired, the user can program it via GUI.

Figure 4 presents a simplified principle of operation of the DDS used for this system.

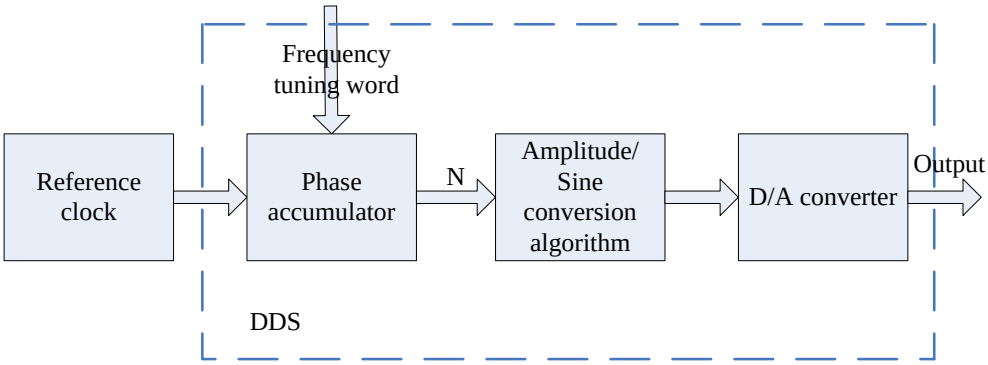


Figure 5: Principle of operation of DDS frequency synthesizer.

Where N is the frequency tuning word resolution. Any frequency can then be generated as

$$0 \leq f \leq \frac{f_{clock}}{2} - \left(\frac{f_{clock}}{N}\right) * X \qquad (1)$$

where X is a programmable integer number. The fastest speed, with which the synthesizer can hop from frequency to frequency, is limited to the supplied clock divided by four. Communication with the device is realized via USB-SPI interface, therefore the frequency setting number needs to be converted to HEX. SPI IC is programmed to convert HEX to binary decimal for writing to the DDS registry. The DDS registry's length is a limiting factor in the frequency resolution; therefore there is a certain minimum step between numbers that can be written into the registry. Conversion calculations will not be covered in this thesis. Further

references to the minimum programmable frequency or time step will be called Quantization Step Size (QSS).

Some other hardware features of the chip can be found in Table 1.

Table 1: Hardware features of the DDS frequency synthesizer used for the project.

Maximum clock speed	400MHz
Frequency tuning word N	2^{48}, 48-bit
Power requirements	External 1.8 and 3.3V
Internal clock divider	1,2,4,8 factors, programmable
DAC resolution	14-bit
Programming software source file	Yes
Output power	0dBm

3.1.2 Carrier generator

Since fast frequency hopping is not imperative for the carrier generator, an inexpensive PLL frequency synthesizer ADF4360-7 from Analog Devices was chosen. This device is offered in an ultra-miniature package: 4x4mm which was not possible to solder onto the PCB under laboratory conditions, therefore an evaluation board had to be purchased. A USB-to-SPI interface and the software for programming of the device were included.

The principle of operation of the PLL frequency synthesizer can be summarized by the diagram on Figure 6.

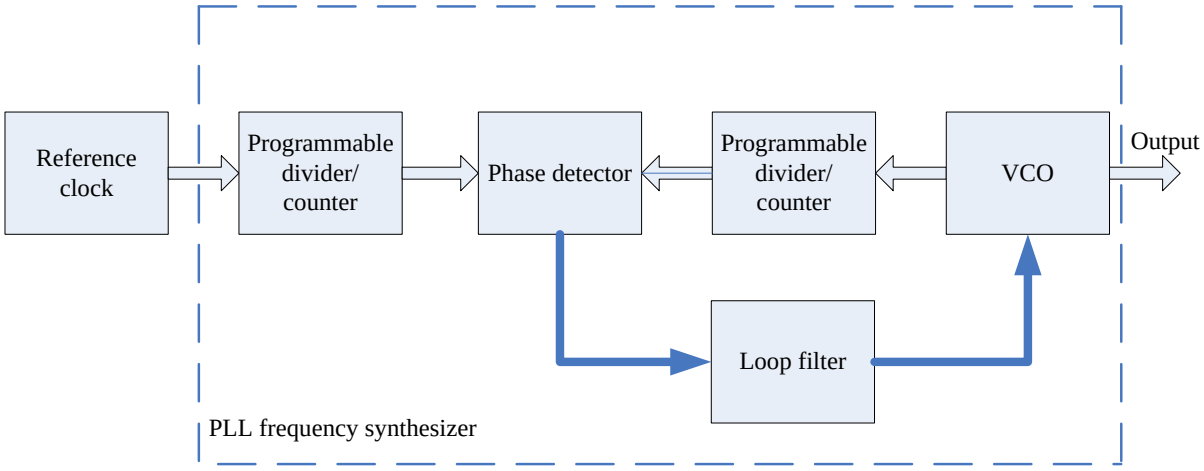


Figure 6: Principle of operation of PLL frequency synthesizer.

PLL frequency synthesizers can be as finely tuned as DDS, but during frequency-hopping, it takes several loops (sometimes up to 200) for the device to lock on to the correct frequency. PLL synthesizers are generally smaller in size as they do not require as much computation resources as DDS and are also cheaper than DDS. As the input clock was used only as a reference and the generated frequency is a product of adjustment of an internal VCO, there is no need to have a high clock speed.

An evaluation board was reconfigured to accept the external clock signal instead of the onboard crystal oscillator. The IC's output stage was matched with lumped elements to output 775MHz. An overview of key device's features is given in Table 2.

Table 2: Hardware features of PLL frequency synthesizer used for the project.

Output frequency range	350MHz to 1800MHz
Power supply	Derived from USB 5V
Output power	0dBm
Software source file	No
Compile software provided	Yes
Clock frequency	10MHz to 500MHz

3.2 Mixer

In choosing a mixer, the parameters that are of most significance are:

- Low noise figure
- High output compression point,
- Small size and small price.

To achieve better isolation of TX from RX, the mixer needs to be turned off during the receive interval. Therefore, short power-on and power-off times were essential. Because of this requirement, a MAX2660 up-converting mixer with a two microseconds delay CMOS logic shutdown control mode was chosen (Figure 6).

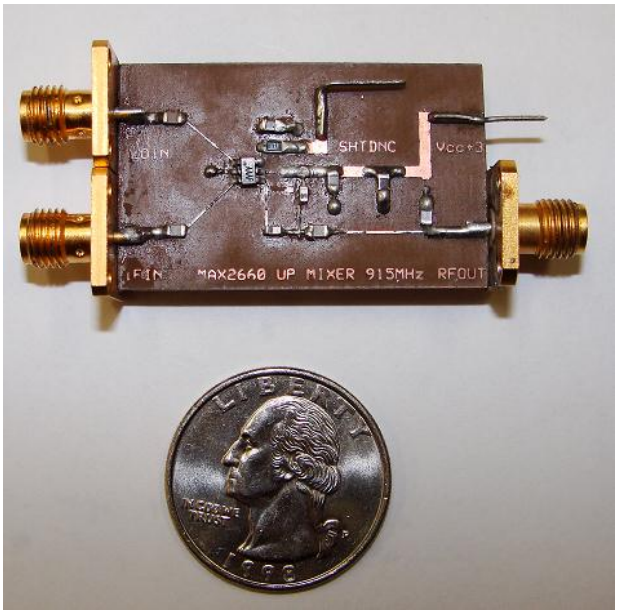


Figure 7: Up-mixer PCB layout.

Due to the mixer's output 1dB compression point at approximately -10dBm, the input powers of LO and IF were reduced from 0dBm to -6dBm, which allowed operation in the linear region of the component. An output matching network was designed according to the datasheet for best matching at 915MHz.

According to the datasheet, the mixer's noise figure should be 10dBm. It was assumed that it is as specified. The following table lists reported characteristics of the component versus measured.

Table 3: Hardware features of the mixer user for the project.

Parameter	Reported	Measured
Output 1dB compression point	-10dBm	-10dBm
Noise figure	10dB	N/A
LO feed through	-22dBm	-18dBm
Turn ON/OFF time	2us	2us
Conversion gain	-7dB	-8dB

By definition, the mixer outputs sum and difference of the LO and IF inputs with multiple harmonics of the mixed frequencies, as shown on Figure 8.

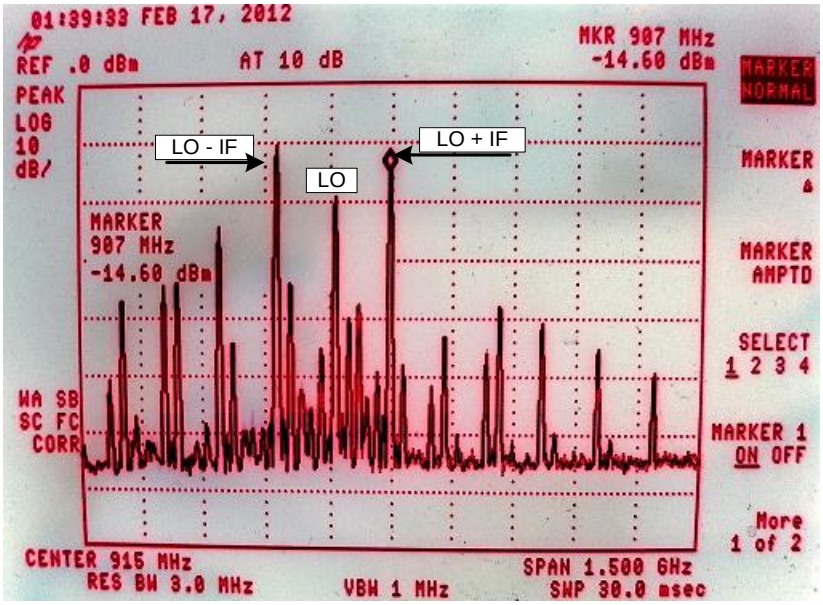


Figure 8: Snap shot of the measured mixer output screen on the spectrum analyzer. The LO supplied to the mixer is 775MHz, IF is 140MHz. LO feed-through, product of summation, subtraction and multiple harmonics is seen.

In order to comply with FCC regulations [1] any harmonics outside of ISM interval need to be filtered. A SAW ISM915 filter, shown in Figure 9, was mounted on a separate PCB and

equipped with SMA connectors to maintain the desired frequency and bandwidth flexibility of the system.

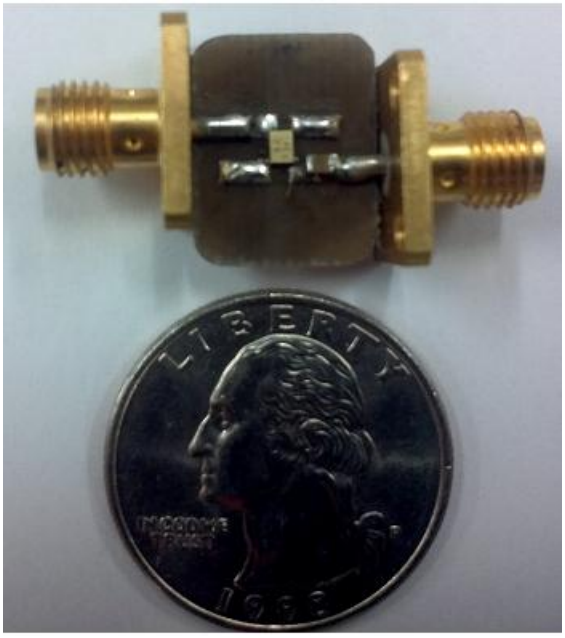
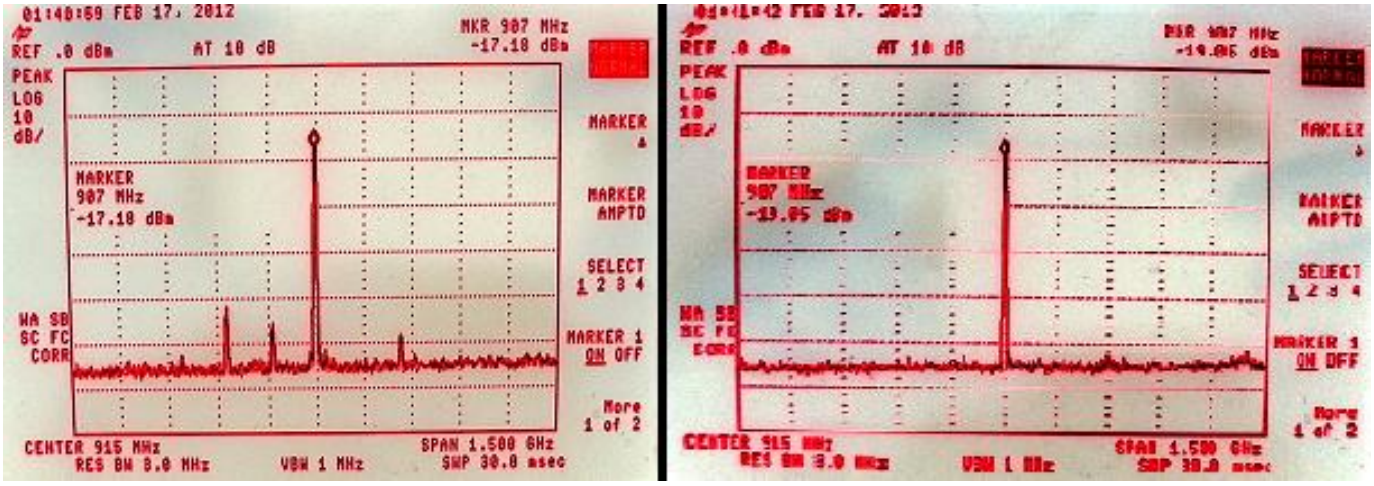


Figure 9: SAW ISM915 filter mounted on separate PCB. DC blocking capacitor added to protect miniature part from the DC voltage damage.

The filter provided 35 dB out-of-band attenuation, which was not enough to completely attenuate unwanted spurious signals (Figure 9- a)). Staging two filters in series allowed for complete suppression of all harmonics on out of band-pass frequencies. (Figure 9-b)).



a) b)

Figure 10: Snap shot of the screen of the spectrum analyzer. An output of the mixer with LO equal to 775MHz and IF of 140MHz. a) with one SAW filter b) with two SAW filters in series.

3.3 Chirp simulation and measurements

Linearly frequency swept signal can be written as:

$$chirp(t) = \begin{cases} \sum_{n=0}^{4} \sin\left(2\pi * f_{c_n} * t\right), & \tau_{bottom_n} \leq t < \tau_{top_n} \\ 0, & \tau_{bottom_n} \geq t \geq \tau_{top_n} \end{cases} \qquad (2)$$

where $\tau_{increment}$ is the dwell time on each individual frequency, $\tau_{bottom} = n * \tau_{increment}$, and $\tau_{top} = (n+1) * \tau_{increment}$

To generate an orthogonal frequency coded radar chirp that could be used for sensor interrogation purposes, several considerations need to be taken to account If the frequency increment occurs while an output sinusoid is not at zero, the DDS will stop signal generation, drop the output to zero and wait until the next rising edge of the clock to generate a new

frequency increment from zero. The resulting chirp would contain phase discontinuities and would not be recognizable on the receiver's side. In order to generate a continuous chirp such as one displayed on Figure 11, with frequencies changing while sinusoid is at zero and to avoid delays between the increments, values $\tau_{increment}$, and $f_{increment}$ need to be chosen such as

$$\tau_{increment} * (f_{begin} + f_{increment} * k) = n \quad (3)$$

where f_{begin} is the bottom frequency of the chirp and k and n are integers for any $\tau_{increment}$ and $f_{increment}$. If the Equation 3 is true, then the chirp length τ can be calculated as

$$\tau = m * \tau_{increment} \quad (4)$$

where m is found as

$$\left(\frac{B}{f_{increment}}\right) = m + 2 \quad (5)$$

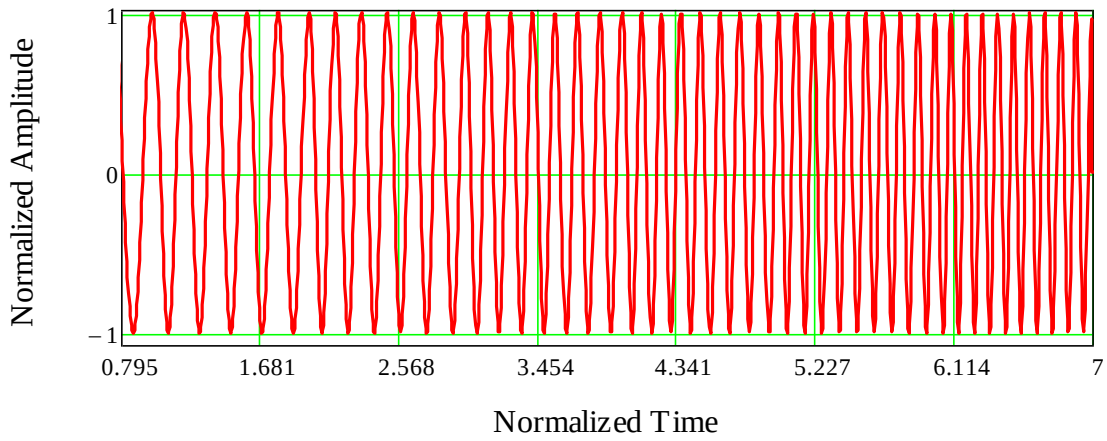


Figure 11: Simulation of linear frequency sweep. An up-chirp is demonstrated.

To make sure that the whole frequency band of an interest is covered and that no information is missed, the phase spectrum of the transmitted signal needs to be as flat as possible. Transmission outside of ISM915 diapason was strictly prohibited. To satisfy both requirements, it was decided to generate a signal with wider spectrum and then shape it down with filters before transmission occurs. The transfer function of the used SAW filters can be written as

$$SAW\_filter(f) = \begin{cases} 1, & f_{min} \leq f < f_{max} \\ -30dB, & f_{min} \geq f \geq f_{max} \end{cases} \quad (6)$$

Simulated signal, shown on the Figure 12, was sampled at the same sampling rate as was set for the hardware.

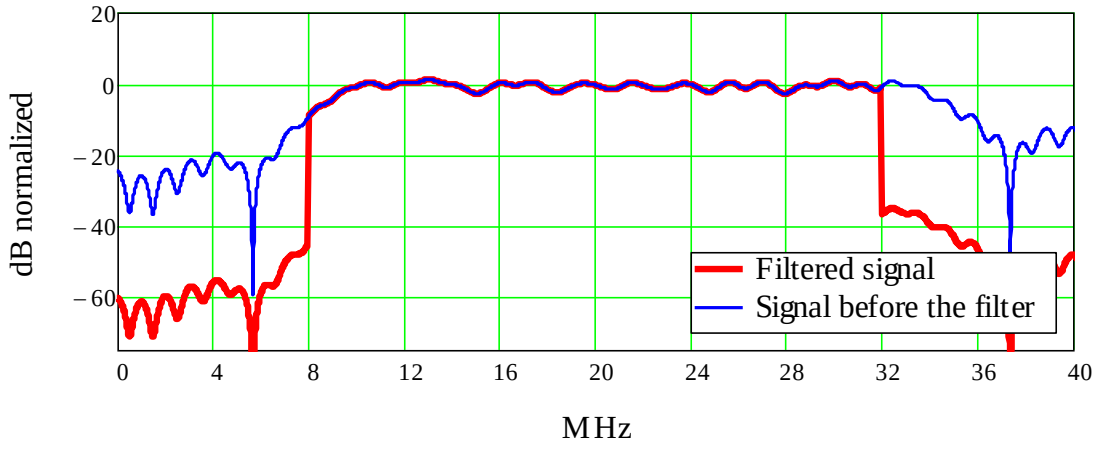


Figure 12: Simulation of the effect of the SAW filter on the simulated frequency swept signal.

The generated chirp was mixed with the carrier, filtered with two SAW filters and then supplied to a receiver substation. Both signals were under-sampled at 80MHz and a Fourier

Transform was then performed on the sampled data. Figure 13 shows a frequency domain plot of the simulated signal versus an experimental data.

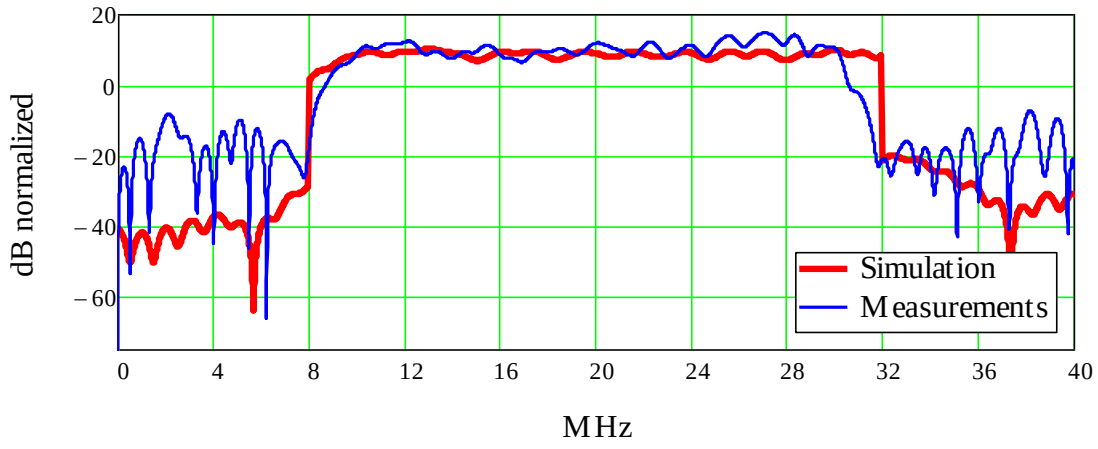


Figure 13: Simulation versus measurement of the produced chirp.

The measured signal is narrower than simulated because it is being shaped-down with an additional SAW filter built in into receiver IC. As Figure 13 shows, the experimentally obtained data closely follows the simulated signal. Broadcasted frequencies are strictly within ISM915 diapason.

3.4 Amplifier

After the insertion of the two SAW filters, the power of the signal on the output of the mixer was measured to be-13dBm. To stay within FCC regulations it is necessary to transmit an output power of less than +30dBm (approximately 1W). The amplifier should then have a total of 45-50dB of gain to account for losses in the connection cables. Such a powerful amplifier needs to

be composed of approximately four or five cascades. To avoid distortions, ringing and damage to the parts, every stage needs to be

- Tuned to the operating frequency
- Operate below 1dB compression point
- Input power needs to be well below absolute maximum values specified for the part
- Output noise figure needs to be as low as possible

While there could be a number of design variations, the design used for the final version of the system was chosen due to its simplicity. Today's market offers many advanced amplifiers, both capable of producing significant gain and outputting high power. The PCB layout for such devices could be rather complex and multilayered PCB is often required to avoid RF coupling between internal cascades. Several components, required designing complicated matching networks, did not meet the specifications due to measured frequency nonlinearities.

3.4.1 First cascade

A low power monolithic amplifier ERA-33SM from Mini-Circuits was chosen for its robust design. Internally matched for 50Ohm, this component demonstrated the exact performance that was specified by its datasheet. The amplifier also showed uniform gain over a wide range of tested frequencies from 200MHz to 1.1GHz. Table 4 contains predicted versus measured characteristics.

Table 4: Amplifier characterization. ERA-33SM datasheet s versus measured parameters.

Parameter	Reported	Measured
Gain	18dB	17dB
1dB compression point	+11dBm	+11dBm
Noise figure	4dB	5dB

Noise figure measurements were performed on N8975A Noise Figure Analyzer (Figure 13).

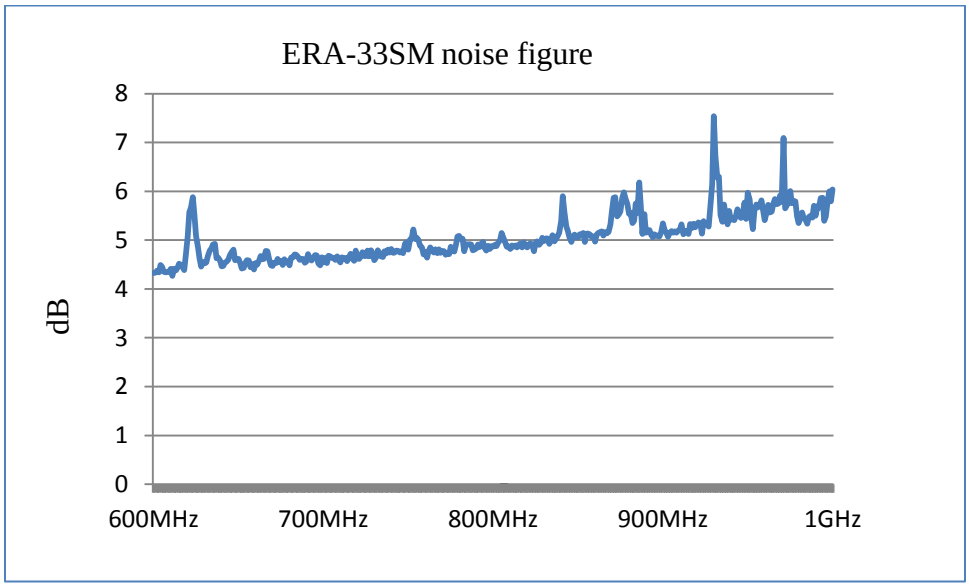


Figure 14: Plot of the noise figure measurements of ERA-33SM amplifier.

The ERA-33SM was cascaded providing a total of 34dB. A 10dB attenuator was installed between the amplifiers to lower gain to below 1dB compression point operation.

3.4.2 Second cascade

A high power amplifier usually produces relatively small gain and dissipates a very significant amount of energy as heat, what makes it inefficient for use with moderate power signals. To bring the signal from +11dBm to the PA on final stage, there needed to be an intermediate amplifier. An MMH3111NT1 from Freescale Semiconductors offered a relatively small gain of 11dB, a low noise figure of 3dB, had little power consumption and was available at low cost. A PCB board was fabricated according to the manufacturer datasheet but fine adjustment of the output matching was necessary for better gain. Table 5 contains measurement results.

Table 5: Amplifier parameters for MMH3111NT1 versus measured parameters.

Parameter	Data Sheet	Measured
Gain	11dB	8dB
1dB compression point	+22.5dBm	+20dBm
Noise figure	3.2dB	6.1dB

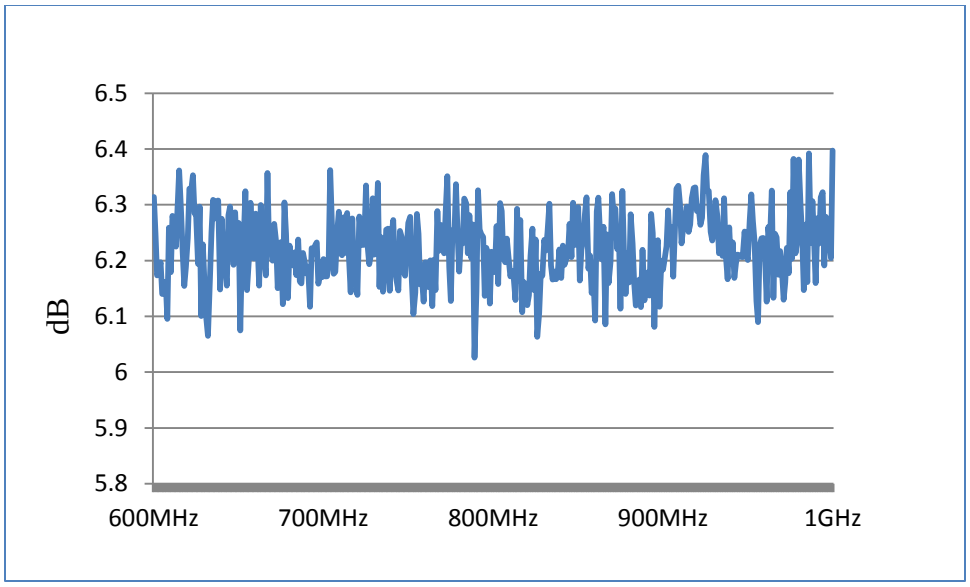


Figure 15: Plot of the noise figure measurements of MMH3111NT1 amplifier.

The measured noise figure was within acceptable limits; however it was significantly larger then reported by the manufacturer. The noise can be reduced with certain layout techniques, but it was decided such work would be beyond the scope of this thesis. To dissipate excessive heat, the component was mounted on a solder slug penetrating the PCB.

3.4.3 Third cascade

After testing, the first and second cascades brought the signal to +17dBm. The gains of the amplifiers cannot be simply added together because of existence of input reflection. An input of both amplifiers should be matched to 50Ohms however imperfections of layout produce a level of input reflection. As long as such reflections stay at a minimum level and do not cause

oscillations within the structure, they can be ignored, but care must be taken to try to avoid input-output mismatch.

A high-power linear monolithic amplifier HELA-10B from Mini-Circuits satisfied input power requirements and could provide up to 1W of an output power. Several PCB layouts were tried to improve output gain, but the best obtained result was 7.5 dB comparable to minimum of 9.5 specified in the datasheet. The HELA-10B was then cascaded and mounted on a single PCB-penetrating solder slug for heat dissipation. An additional cooling fan was installed on the back of the structure (Figure 15). The datasheet noise figure is 3.5dB; an actual NF was not measured.

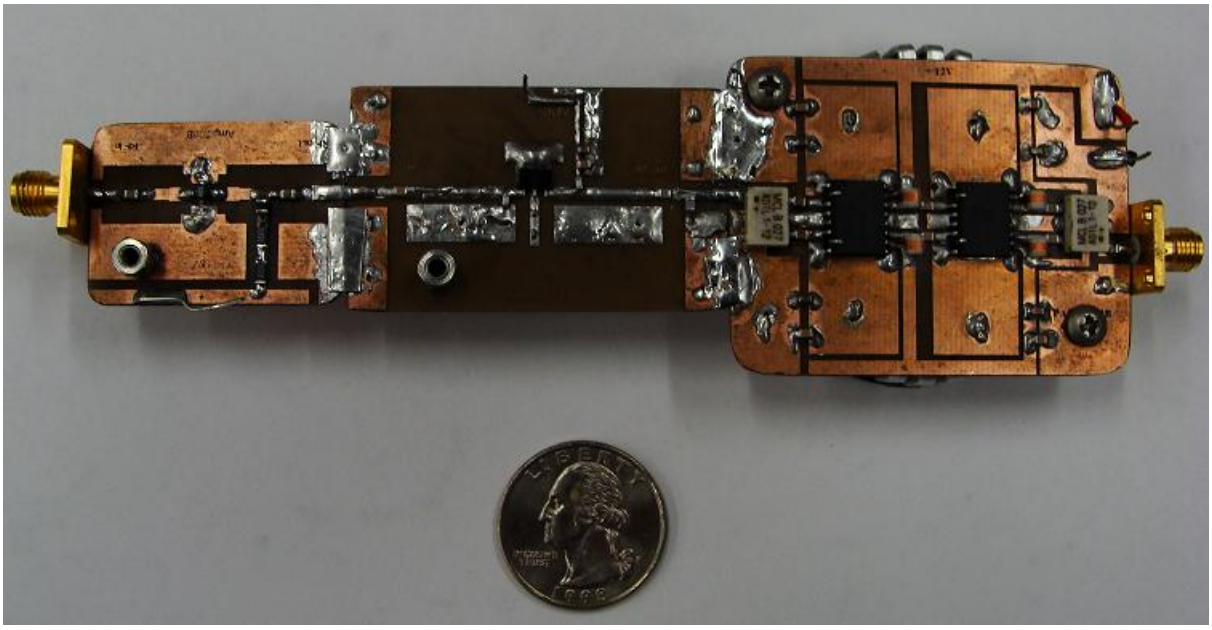


Figure 16: Four cascades of an amplifier. Fifth cascade is not included. A cooling fan is installed on the back of the PCB.

All cascades of the amplifier provided 47dB of gain with approximately +27.5dBm maximum power output. The cumulative noise figure of the cascaded amplifier can be found according to the Friis equation:

$$NF = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 * G_2} + \frac{NF_4 - 1}{G_1 * G_2 * G_3} + \frac{NF_5 - 1}{G_1 * G_2 * G_3 * G_4} \ldots \qquad (7)$$

Substituting the numbers, the noise figure of the cascaded amplifier was determined to be 4.5dB.

3.5 RF switch

Despite the fact that the mixer could be turned off during the receive cycle, the design called for a high speed RF switch between the antenna and the signal generator, as on Figure 17, to make sure no signal is transmitted during mixer shut-down time (2us).

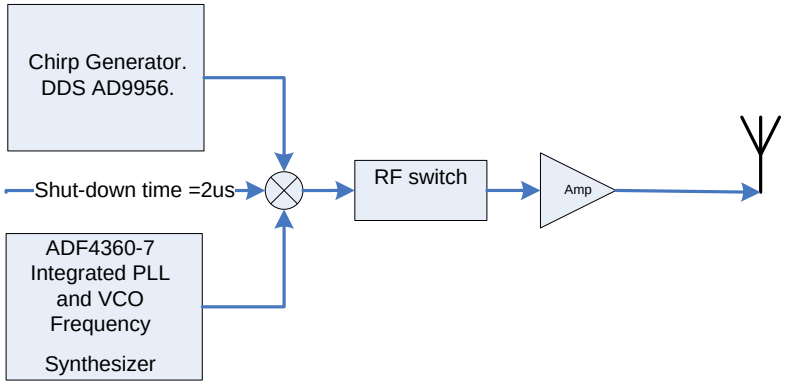


Figure 17: Block diagram of the placement of the RF switch.

When choosing an RF switch, high isolation is usually a trade-off for high operating power. The ADG902, single pole single throw reflective switch from Analog Devices, offered excellent isolation - up to 40dB in the off position and had a fast switching time - 4ns. The highest input signal of the switch is +11dBm, which was acceptable since the device was placed before the amplifier. Measured results matched datasheet values.

3.6 Antenna

A folded dipole patch antenna with a center frequency of 912MHz, a fractional bandwidth of 10% and an approximate gain of 2dB [2] was used for both the transmitter and receiver (Figure 17)

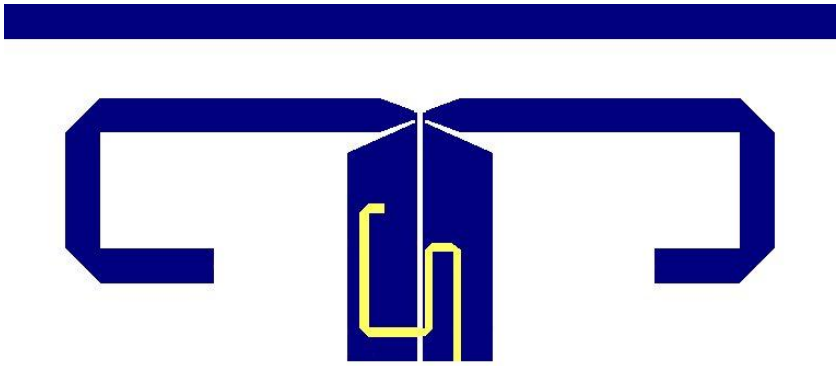


Figure 18: An image of folded dipole antenna. Blue – top PCB layer, yellow – bottom PCB layer.

The SAW sensor was mounted on a similar type of antenna which was adjusted for better matching with the packaged device. In the absence of an anechoic chamber for antenna characterization, it was best to use antennas of the same type, so they could be positioned in the same way to match their radiation patterns.

3.7 ISM regulations

According to FCC ISM915 regulations, the bandwidth of the interrogator transmitter should not exceed 26MHz (902-928MHz) and the maximum output power cannot be more than

+30dBm. To make sure that system can meet all requirements, the output power of the system under design was limited to +27dBm. Even higher power output could be used if the system were to satisfy the fast frequency hopping condition (section 15.247 in FCC regulations). Specific techniques, which will be discussed in chapter four, need to be implemented for generation of an interrogation signal. Whether or not the system may be qualified for the specific FCC condition for higher power output, will not be discussed in this thesis and, perhaps, research of that topic may benefit further development of the OFC SAW passive sensor technology.

CHAPTER 4: CONTROL AND SYNCHRONIZATION SYSTEM

Synchronous switching is vital to the stable operation of the coherent receiver-transmitter communication system. Not only does switching within the system need to be precise and constant pulse-to-pulse, but the phase of every transmitted signal needs to be matched. This chapter will describe how synchronization is achieved in the designed system. The system delay and switching time diagram will be presented.

4.1 Common system clock

The control and synchronization system consists of counters, dividers and frequency multipliers using the common master clock for its operation. The common clock is derived from 27MHz temperature controlled crystal oscillator (TCXO) with programmable PLL clock frequency synthesizer CDCEL913 from Texas Instruments. The master clock generator IC has three programmable outputs configured to output the same synchronous 80MHz clock. An evaluation board with USB-to-SPI interface was used for the project with the purpose to deliver a system with an easily adjustable center clock frequency.CDCEL913 clock generator IC contains a block of nonvolatile memory, uses to save the configured frequency settings, eliminating the need to program the IC on the power-up The produced 80MHz system clock is then supplied to the FPGA for further division, to ADC to be used as a sampling rate and to the PLL frequency synthesizer for multiplication as in Figure 19.

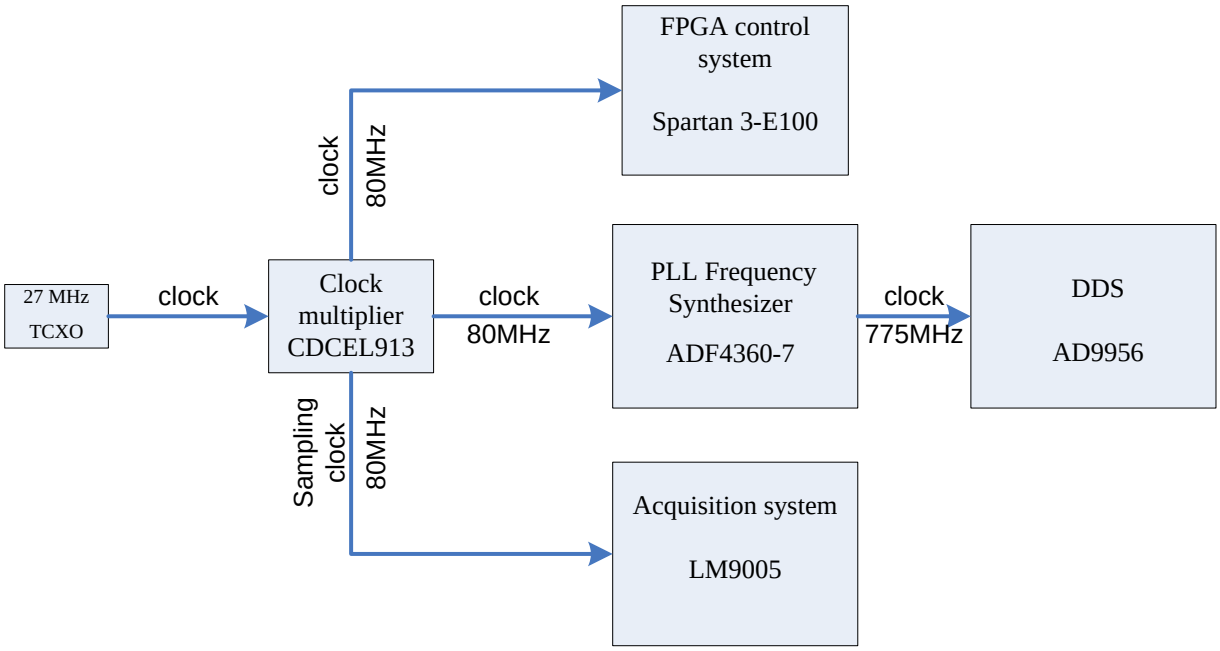


Figure 19: Block diagram of the clock distribution within the system.

The ADF4360-7 PLL frequency synthesizer, described in section 3.1.2, employs a system of counters to synchronize the signal, produced on an internal VCO, with the common system clock. Produced frequency of 775MHz is multiplied with a power splitter 1:2 with 0º phase shift from Mini-Circuits. The signal is then used as a carrier on the up-mixer on the transmitter side, and on the down-mixer on the receiver side. The same frequency is used as a clock for the chirp generating DDS.

4.2 FPGA based control system

An 80MHz master clock is used as a clock signal for the control FPGA. An evaluation board with a USB-to-SPI interface on it, allowing for programming of the FPGA, was used for the project. The chip is programmed with the Xilinx programming package using Verilog programming language.

A block diagram showing principles of operation of the control system can be found in Figure 20.

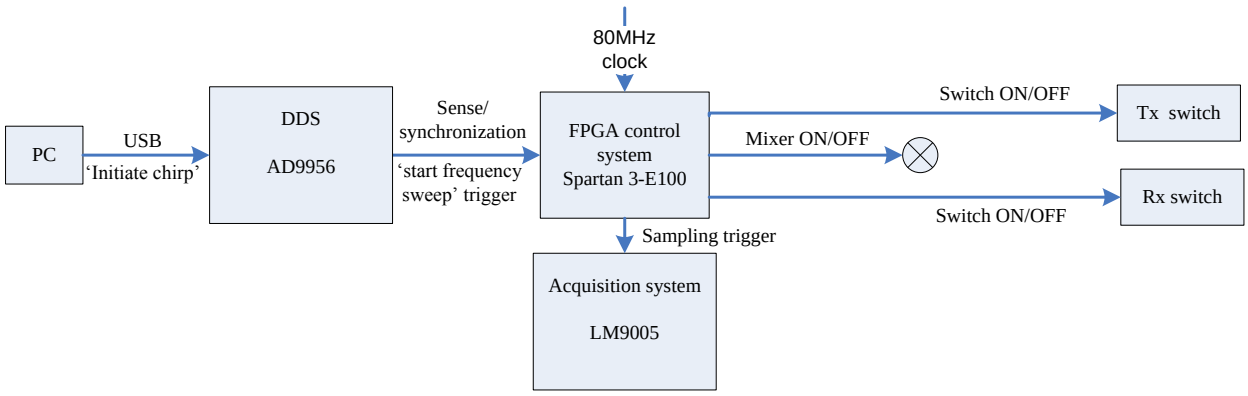


Figure 20: Block diagram of functionality of the FPGA-based control system.

The trigger to start a new transmission cycle comes from the computer based software. As the signal from the computer comes onto the USB-to-SPI interface IC of the AD9956 evaluation board, a digital '1' is written to the appropriate pin of the DDS. A 'start frequency sweep' pin of the DDS is directly wired to one of the input pins of the FPGA, which senses the change of the state of its input on the next rising edge of its (FPGA's) clock. The FPGA is programmed to start a counter of every rising edge of the clock upon the change of the state of its 'sense' input. The

control chip then drives the circuitry shown on Figure 20 according to the switching diagram presented on Figure 21

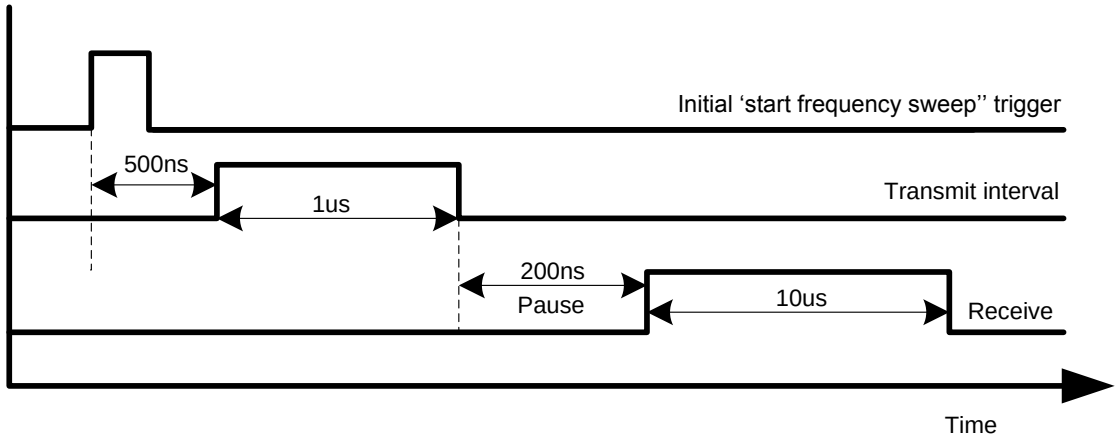


Figure 21: Switching time diagram of the control system.

The internal triggering mechanism of the FPGA recognizes a rising edge of the clock at the $1/\sqrt{3}$ of the clock’s maximum value. A clock generator IC CDCEL913 outputs a nearly ideal sinusoidal signal. Knowing that two consecutive switching periods might be started with the first at the very beginning of the clock oscillation period, and the second at the very end of it, the maximum synchronization error can be found as

$$\Delta t_{sync\_error\_max} < 2 * \frac{1}{f_{clock}} * \frac{1}{\sqrt{3}} = 17.7ns \qquad (8)$$

The chance of maximum synchronization error occurrence is very small because the execution of the ‘begin chirp’ command starts on the next rising clock edge of the DDS and DDS clock is derived from the same signal that the FPGA uses for its operation.

An FPGA evaluation board used for the project contains an EPROM memory, eliminating the necessity to program the device on each power-up.

4.3 Propagation delay characterization.

Although it does not affect the functionality of the system, it is important to understand the nature of all of the system delays and have those delays characterized for proper post processing of the obtained measurement data.

An internal DDS execution delay combined with propagation delay of two SAW filters on the receive side was measured to be approximately 300ns as displayed on Figure 21. The transmit switch is open for 1 microsecond at the time when DDS conducts the sweep on the frequencies of interest. A receiver-IC internal hardware delay, combined with the propagation delay of the two SAW filters on the receive side, was measured to be approximately 300ns as displayed on Figure 22.

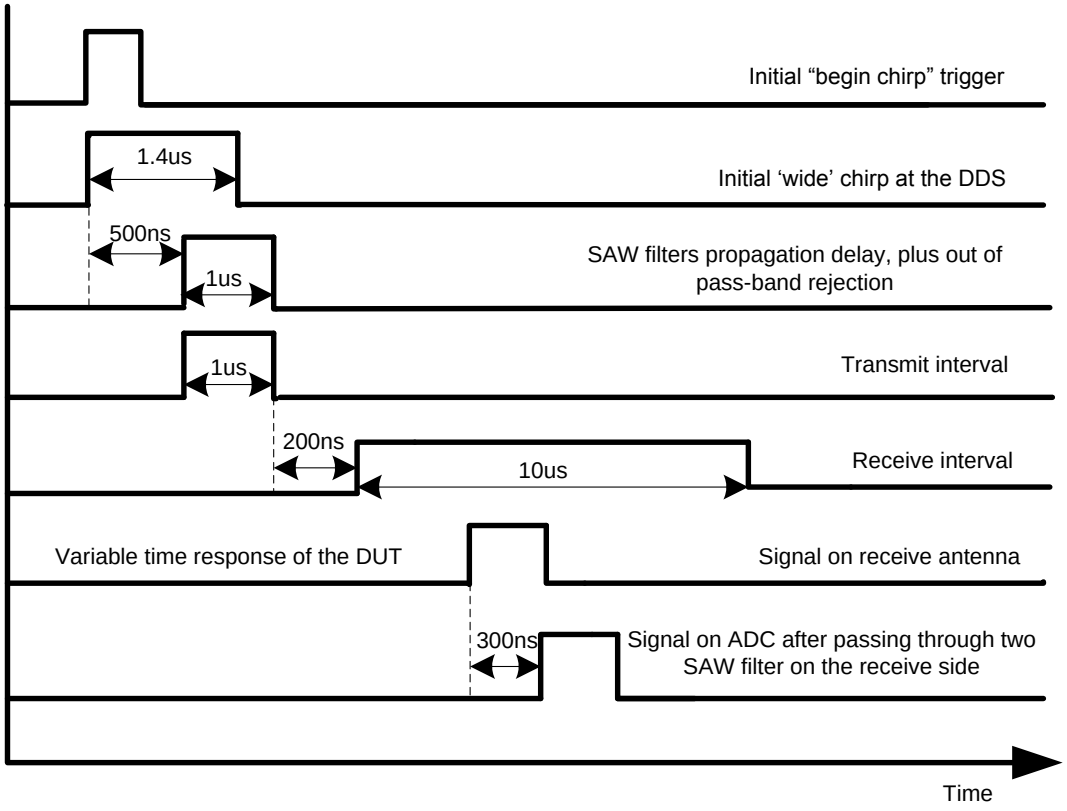


Figure 22: Timing diagram of the designed communication system. By decreasing the bandwidth of the chirp, the SAW filters are shrinking the length of the signal in time.

The provided timing diagram can be used for proper characterization of the time response of the interrogated target.

CHAPTER 5: RECEIVER

Synchronous receivers for wireless sensor readings were previously built and tested [3]. Prices for such devices were high and, in the case of the PCI card as ADC, required internal computer hardware installation. This prevented the communication system from being a "plug-n-play" device. Recently released for sale (November 2011) inexpensive and fully integrated IF-sampling receiver subsystem on single chip from Linear Technology showed very attractive qualities and needed to be evaluated. Since only preliminary datasheet has been released, testing was needed in order to determine the performance of the part. The following chapter will cover the theory of operation of an IC. Hardware limitations and USB communication with the IC will be examined.

5.1 Principles of operation

A block diagram, showing the internal structure of the receiver subsystem IC from Linear Technology, is presented on Figure 20.

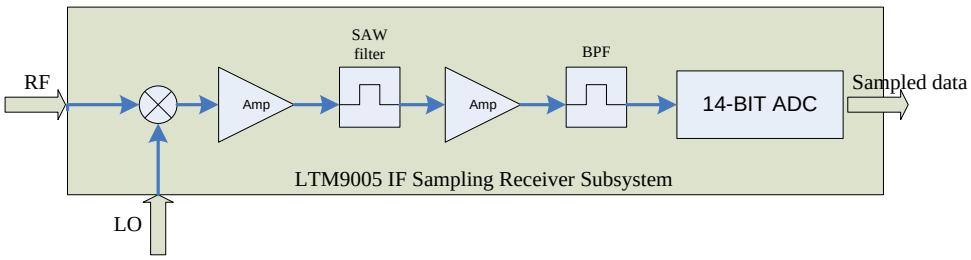


Figure 23: Principle of operation of the receiver-IC.

An RF signal is mixed down to IF on the internal mixer. The resulting IF signal is then amplified on the low noise amplifier (LNA). A SAW filter with a center frequency of 140MHz and bandwidth of 20MHz attenuates any frequencies outside of the band of interest. The band-limited signal is then amplified on a second LNA and filtered once again on a low-pass filter. The amplified and filtered signal is supplied to the 14-bit ADC. A brief summary of useful information on the IC's features is given in Table 6

Table 6: List of receiver-IC features.

RF frequency range	400MHz-3.8GHz
Internal IF SAW filter center frequency	140MHz
IF bandwidth	20MHz
ADC resolution	14-bit
Highest sampling rate	125MSPS
Noise figure	16dB
Power consumption	1.2W
External voltage levels required for operation	1.2V, 1.8V, 2.5V, 3.3V, 5V
Average SNR	67dB
Internal gain	17dB adjustable

5.2 Receiver subsystem characterization and tuning

The integration of the whole system onto one chip eliminated the necessity to create matching networks and complex RF isolation for the receiver's PCB layout. An RF input is internally matched to the signal on 1.6GHz-2.3GHz, but for 915MHz an external shunt capacitor 3.9pF was added to improve return loss. For better LO input matching, an external 2.7pF shunt capacitor was added on corresponding pin of the IC (Figure 24).

Figure 24: Integrated receiver subsystem. Matching is shown with the arrows.

A 6dB improvement of an output gain observed after RF and LO matching was performed. The same amplitude and frequency signals were applied on RF and LO inputs of the IC for the s "before" and "after" measurements.

As shown in Table 6, the receiver requires four external voltage levels and a USB 5V supply. It is necessary to provide maximum RF isolation over the power supply wires. Voltage conversion circuitry, built for the project, consisted of four buck converters. All voltage levels were derived from the 5V output of standard computer power supply. Every wire was routed to the receiver at the maximum allowable distance from the transmitter to avoid induced coupling of the transmitted signal to the receiver. Decoupling capacitors and RF chokes were placed on every voltage conversion circuit to discharge or block possible RF leakage of the transmitter signal through the power supply.

5.3 Minimum detectable signal and signal-to-noise ratio.

Minimum detectable signal (MDS) can be estimated as

$$MDS = 10log_{10}(\kappa T * BW) + NF_r \quad (9)$$

where κT is the thermal noise, NF_r is the noise figure of the receiver and BW is the bandwidth of the received signal [4]. Substituting the values in the formula with numbers from Table 6, Equation 9 can be rewritten as

$$MDS = -99.531dBm + 16dB = -83.531dBm \quad (10)$$

As all of the receiver's and transmitter's parameters are known, the signal-to-noise ratio of the whole system can now be estimated. The signal can be found as [5]

$$S = E_{IRP} * G_{RX} * [G_{SAW} * PL] * PG * {N_{sum}}^2 \quad (11)$$

where G_{RX} is total gain from antenna to ADC, G_{SAW} DUT gain, PL path loss, PG signal processing gain of the system N_{sum} number of synchronous integrations in ADC. E_{IRP} equivalent isotropic radiated power can be found as

$$E_{IRP} = G_{AMP} * G_{TX} \quad (12)$$

where G_{TX} is the gain of transmitter's antenna and G_{AMP} is the total gain of the transmit amplifier. The term $E_{IRP} * [G_{RX} * [G_{SAW} * PL] * PG]$ is limited by maximum allowable full-scale power level that can be applied to an analog input of an ADC.

Noise can be found as

$$N = kT * BW * NF_r \quad (13)$$

5.4 Range of measurement characterization

The dynamic range of the measurements is set by the maximum RF input power level that the receiver can accept without damage to the hardware. The dynamic range of the receiver, in turn, determines the minimum and maximum distances to the interrogation target. To increase the maximum range of measurements, the received signal was pre-amplified before it was supplied to the receiver-IC. A monolithic amplifier ERA-33SM, described in Chapter 3, was used. The PCB layout, shown on Figure 26, was optimized and ISM915 SAW filter was added to improve the noise figure.

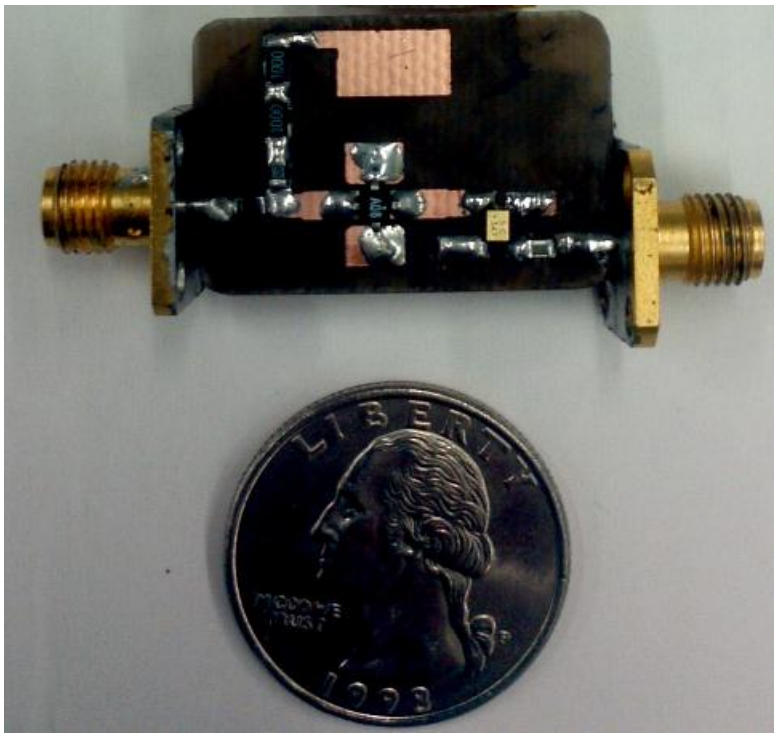


Figure 25: ERA-33SM optimized for low-noise figure PCB layout. SAW filter for out-of-band noise suppression.

The noise figure of the receiver was calculated according to Y-factor method [6]. The receiver's noise figure can be found as

$$NF_{dB} = ENR_{dB} - 10\log(Y - 1) \qquad (14)$$

where ENR is the excess noise ration of the used noise source. Noise was measured on the output of the noise amplifier, as displayed don Figure 26, and showed to be 46dB above the noise floor, therefore $ENR = 46dB$. $Y$is found as

$$Y = \frac{N_h}{N_c} \qquad (15)$$

where N_h and N_c are powers of noise as displayed on Figure 26.

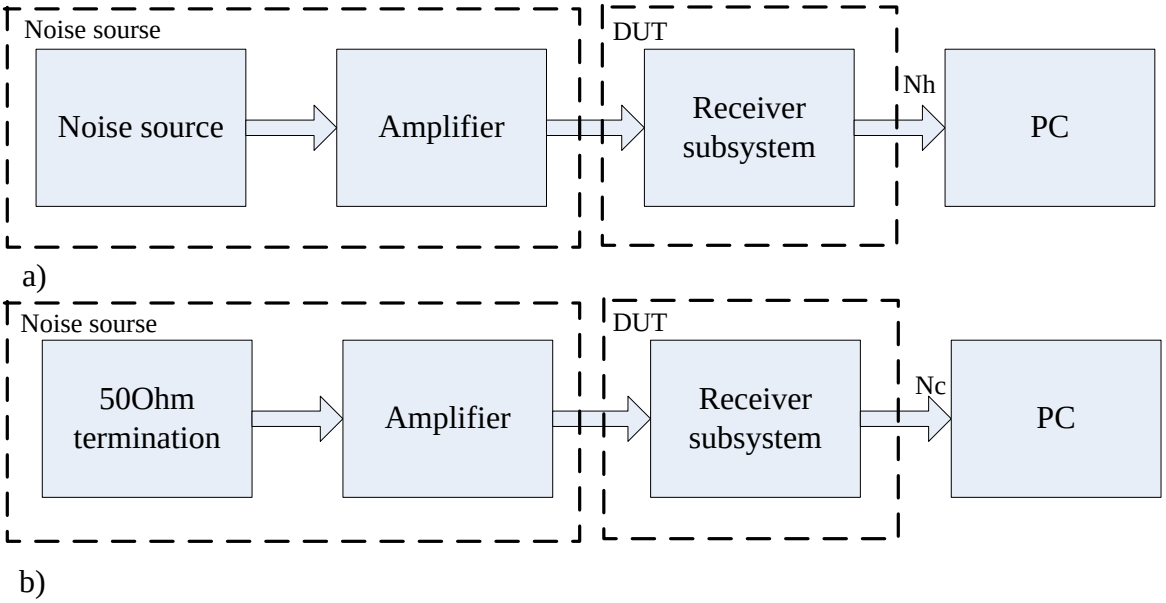


Figure 26: Noise figure measurements of the receiver. a) noise source is connected to the receiver, b) receiver is terminated with 50Ohm.

The noise was averaged over 600 merging points and plotted as on Figure 27.

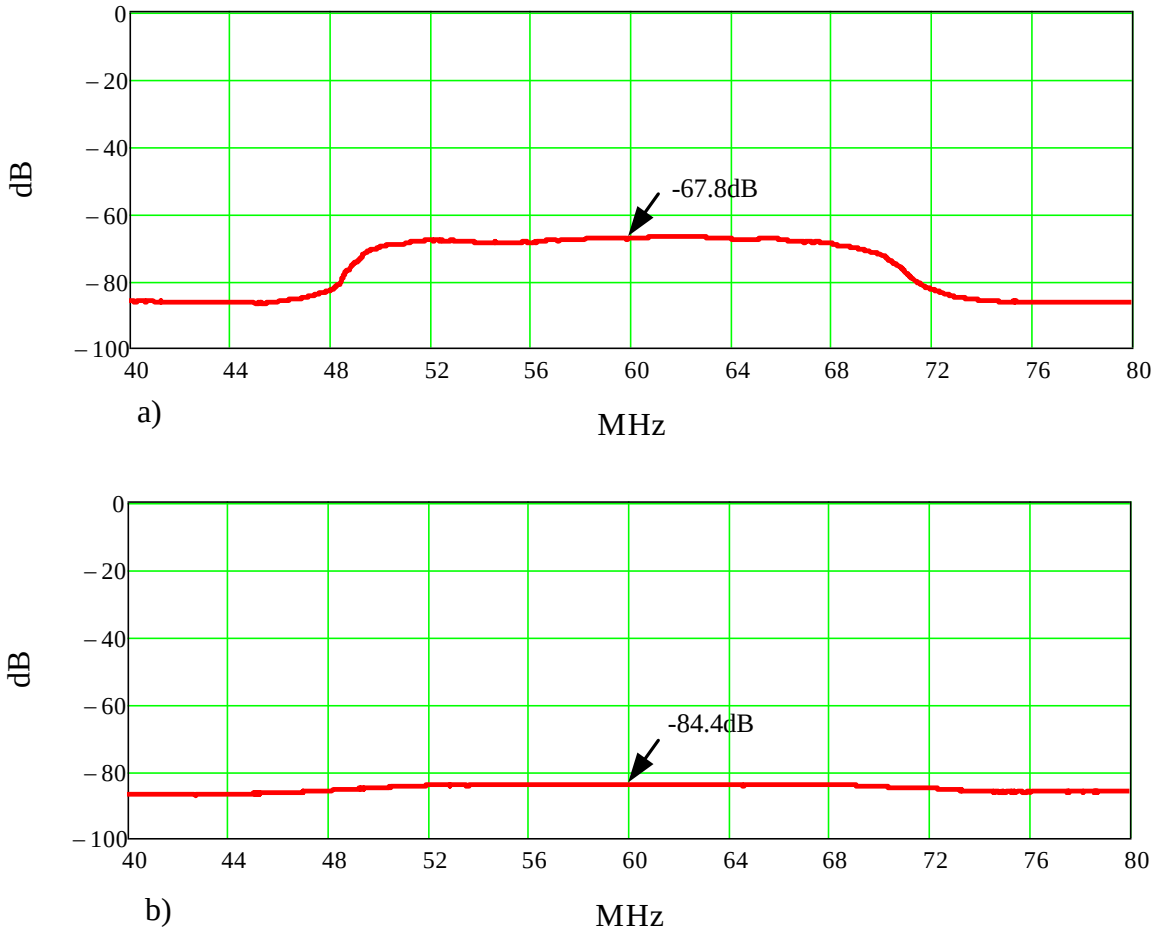


Figure 27: Plot of data measured for noise figure calculation of the receiver. a) noise source is connected to the receiver, b) receiver is terminated with 50Ohm.

The parameter Y then can be found as

$$Y_{dB} = (-67.8 - -84.4) = 16.6dB \qquad (16)$$

According to equation 14

$$NF_{dB} = ENR - dB(Y_{linear} - 1) = 15.9dB \qquad (17)$$

The minimum detectable signal can now be found as

$$MDS = -99.531dBm + 15.9dB = -83.631dBm \quad (18)$$

The receiver IC has integrated variable gain adjustment circuitry which was set up for maximum gain. It should be noted, that the receiver's performance can be improved if the receiving amplifier were to be substituted with a low noise prototype.

An antenna used for the experiments [2] has a radiation pattern that can be approximated to be ideal isotropic for simplicity of calculations. The free-space path loss equation for an ideal isotropic antenna is [7]

$$PL = \left[\frac{4*\pi*d}{\lambda}\right]^2 \quad (19)$$

As the wave travels two ways, the Equation 16 can be rewritten as

$$PL = \left[\frac{4*\pi*d}{\lambda}\right]^4 \quad (20)$$

The propagation loss of the interrogation device is approximately 15dB. The receiver-IC has a maximum no damage RF power limit $P_{max} = -12dB$. An additional amplifier with the gain $G_{add} = 17dB$, raised the maximum RF input power to -30dBm. The range of the allowable measurement power can be written as

$$MDS - G_{add} \leq P \leq P_{max} - G_{add} \quad (21)$$

or, numerically, as

$$-100.631dBm \leq P \leq -29dBm \qquad (22)$$

Knowing that the transmitter outputs $P_t = +25dBm$ and propagation loss of the SAW sensor tag is 22dB, the dependence of range of the measurement on the power of the signal at the receiver can be plotted as on Figure 28.

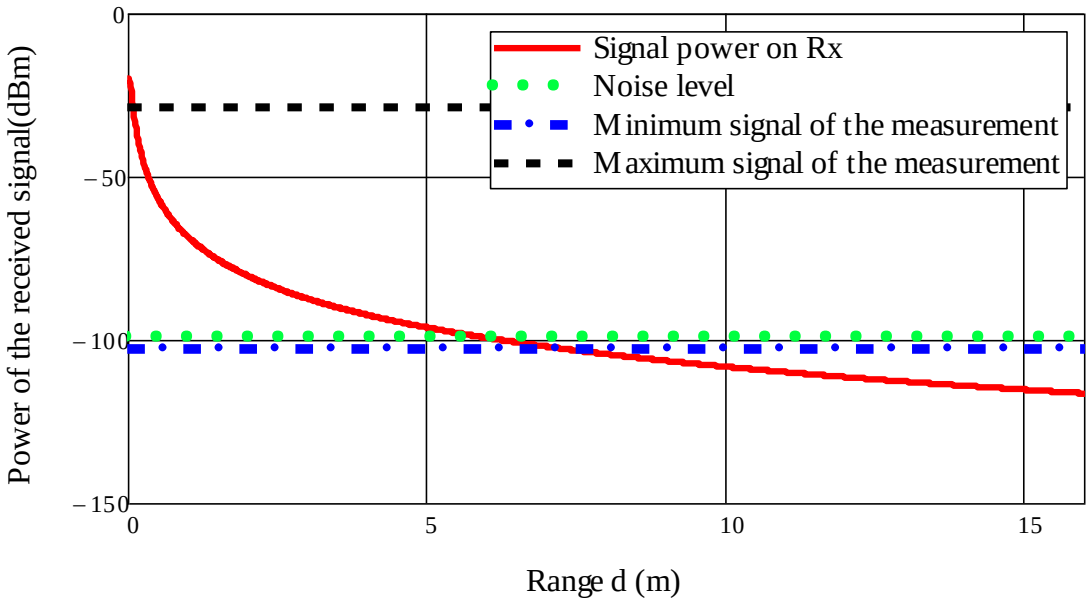


Figure 28: Dependence of power of the received signal on the range of the measurement. In ideal environment the recovery of the data based on one pulse can be achieved on the distance from 0.2m till 6m. Employing coherent integration, the range can be extended to 8m based on current configuration.

The noise level on the Figure 28 is the thermal noise found as

$$N_T = kT * BW = -99.531dBm \quad (23)$$

Previous analysis assumed all ideal conditions and can serve the purpose of estimating the actual behavior of the system. The noise floor within ISM915 band is considerable higher than just the thermal noise. A variety of devices use this frequency for communication and additional research of possible interference with such devices is necessary to determine the true noise floor on the frequency of operation of the system. The system's internal circuitry blocks are well isolated from interfering Tx-Rx, however, the assumption that there is no Tx-Rx feed through can only hold true to a certain extent.

5.5 Data transmission characterization

An evaluation data acquisition board DC718C from Linear Technology (Figure 29) was used to provide USB communication with the receiver.

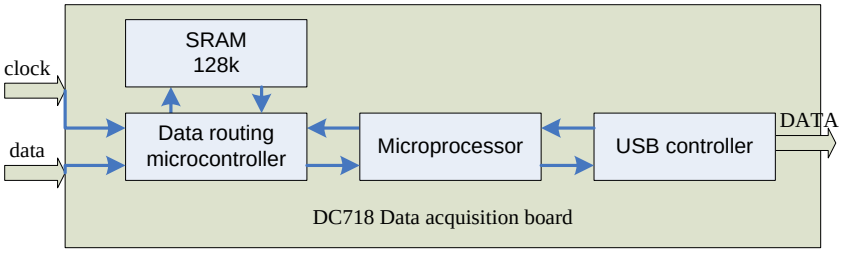


Figure 29: Block diagram of principle of operation of the data acquisition board DC718C.

Due to the specific of the design of the data acquisition board, continuous sampling is not possible. Once a request to begin a sampling cycle is sent, the data from the ADC begins

streaming into the SRAM. Upon reaching the limits of the memory, sampling ends and transmission to the USB controller takes place. A fixer number (131072) of samples is written into 128k of memory every sampling period. The user has control over how many samples he wants to read before they are overwritten during the next sampling period. A new sampling cycle cannot be started until reading from the memory is completed. The minimum inter-sampling period had to be determined experimentally and proved to be 15ms. The sampling period depends on the provided clock signal as

$$T_{sampling} = ISP + \tau_{clock} * N \qquad (24)$$

where N is a fixed number equal to 131072, and ISP was experimentally found to be 15ms. The user has control over the total time interval that can be obtained from the single measurement. The value of $\tau_{clock} * N$ can be changed with the change of the clock frequency. Following a review of the nature of the measurements, the suggestions for optimum sampling frequency and acquisition repetition interval will be made in Chapter 6.

CHAPTER 6: POST PROCESSING AND METHODS

To increase the range and precision of the measurements there are variety of DSP techniques that can be implemented. The capability of modern computers and the software used for signal post processing place certain limits on the speed with which the acquired data can be managed. Since the signal to begin chirp is initiated on the same computer used for post processing, care must be taken in order to avoid overloading a processor and a bus used for communication with the device. Exceeding hardware limitation can cause random lagging of the used software, which in turn may cause synchronization instability. This instability will result in missing data and further deviation from proper operation. Software used for chirp generation and post processing of the data, Matlab and Visual Basic, are both high level languages. A significant increase in operation speed could be achieved simply by describing the existing algorithms in a lower level language such as C. Although rewriting the software is beyond the scope of this thesis, a study of the factors affecting the processing speed will be made. The range and precision of the measurements are directly dependent on the post processing algorithms. Algorithms themselves need to be understood thoroughly before we can proceed further. In order use the optimum DSP technique, it is necessary to have some prior knowledge of the expected signal. This chapter will cover basic concepts of operation of DUT, and then post processing algorithms will be discussed.

6.1 SAW reflection mechanism overview

Surface acoustic wave can be generated by an alternating voltage applied to the electrodes on the surface of the piezoelectric material as on Figure 30.

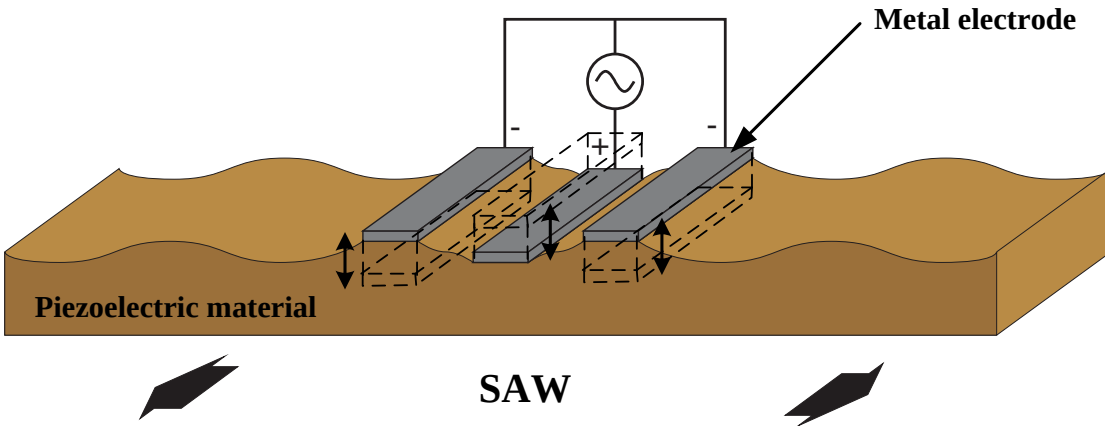


Figure 30: Illustration of the mechanism of generation of the surface acoustic wave.

Positive potential (with regards to the neighboring electrodes) causes the electrode to rise up, while negative potential causes it to lower down. A surface acoustic wave launched on the electrode-structure, called an inter-digital transducer (IDT) (Figure 31), then propagates on the surface of the piezoelectric material [8] .

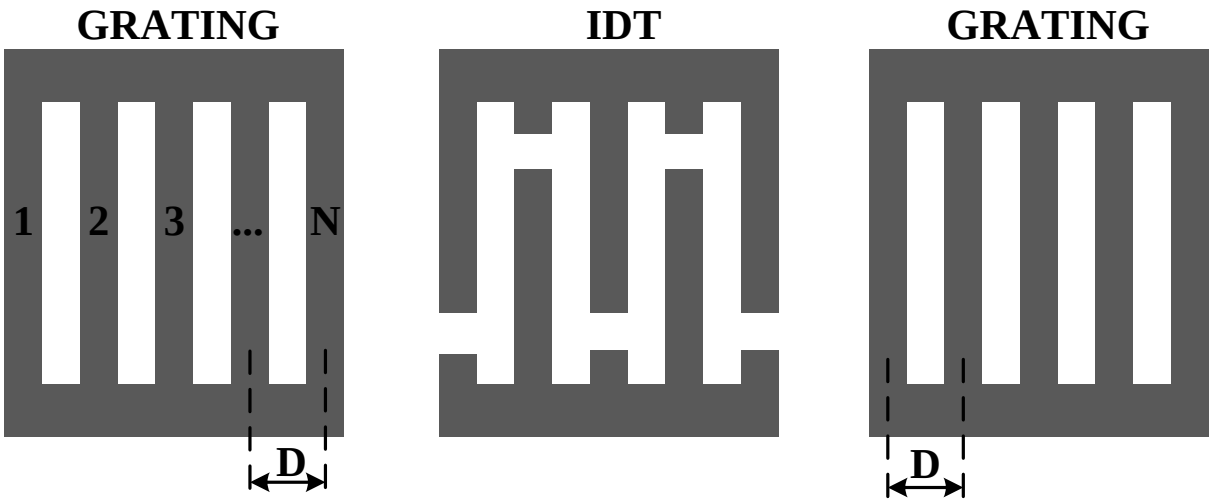


Figure 31: SAW reflector structure.

Upon reaching the interconnected electrode-structure called grating, the SAW then reflected equally from each individual electrode. The center frequency of the response can be calculated as

$$f_0 = \frac{v_{saw}}{D} \qquad (25)$$

where L is the distance between reflecting electrodes (typically half of the wavelength). Total response length of the grating, can be derived as

$$\tau_{reflector} = 2 * \frac{(N-1)*L}{v_{saw}} \qquad (26)$$

where N in a number of electrodes and time is multiplied by factor of two since the SAW needs to travel two ways.

The time domain response of an array of M electrodes in a grating to an impulse function can then be defined as

$$(t) = \begin{cases} \sum_{m=0}^{M} a_m * \sin\left(2\pi f_{o_m}(t - \tau_{distance})\right), & 0 \le t \le \tau_{distance} + \tau_{reflector} \\ 0, & |t| > \tau_{distance} + \tau_{reflector} \end{cases} \quad (27)$$

where a is a weighting coefficient and $\tau_{distance}$ is a time delay associated with propagating of SAW to M^{th} reflector in a bank.

Total reflectivity of the array can be approximated as [8]

$$|R| = \tanh(N * |r|) \quad (28)$$

where r is electrode reflectivity and N is the number of the electrodes in the grating.

6.2 OFC SAW device structure and modeling

An orthogonally frequency coded temperature sensor is a device composed of IDT and a reflector structure, designed in a such a way, that several devices can operate on the same frequency without interfering with each other [9]. A definition of orthogonal frequency coding and its application to the SAW sensors design is discussed in this section.

A time limited, nonzero time function [10]

$$h(t) = \begin{cases} \sum_{n=0}^{N} a_n * \varphi_n(t), & |t| \le \frac{\tau}{2} \\ 0, & |t| > \frac{\tau}{2} \end{cases} \quad (29)$$

where $\varphi_n(t) = \cos\left(\frac{n\pi t}{\tau}\right)$ and a_n is a constant, satisfying condition

$$\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} {\varphi_n}^*(t) * \varphi_m(t)\, dt = \begin{cases} K, & n = m \\ 0, & n \neq m \end{cases} \quad (30)$$

where K is a constant, is said to be orthogonal if

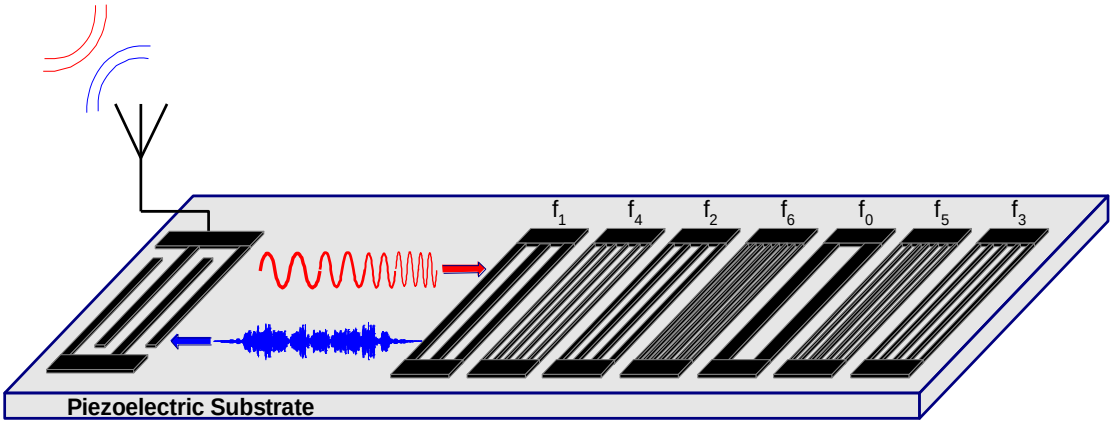
$$h_{even}(t) = \begin{cases} \sum_{n=0}^{N} a_n * \cos(\frac{2n*\pi t}{\tau}), & |t| \leq \frac{\tau}{2} \\ 0, & |t| > \frac{\tau}{2} \end{cases}, n\ is\ an\ integer \quad (31)$$

$$h_{odd}(t) = \begin{cases} \sum_{n=0}^{M} b_m * \cos(\frac{2m*\pi t}{\tau}), & |t| \leq \frac{\tau}{2} \\ 0, & |t| > \frac{\tau}{2} \end{cases}, m\ is\ an\ integer \quad (32)$$

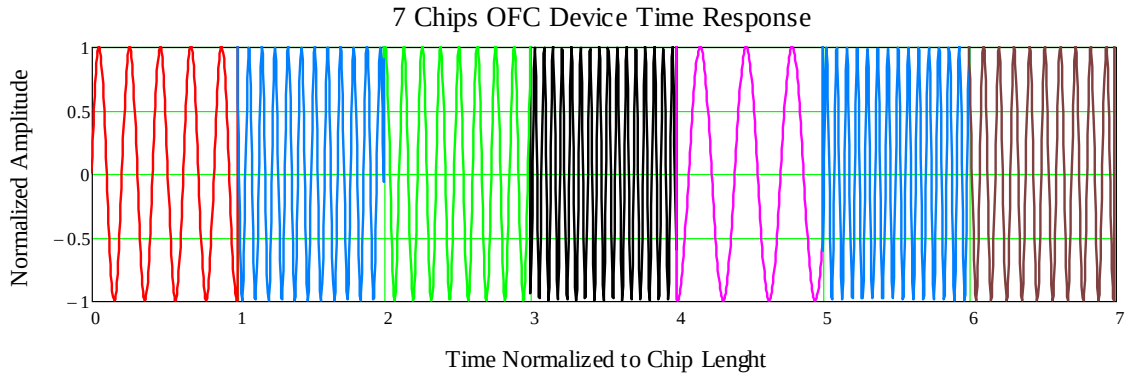
A series of reflectors (chips) can then be built with each chip tuned on frequencies:

$$fn_o = \frac{n}{\tau} \quad (33)$$

The chips do not necessarily have to be placed on the wafer in sequential order according to their frequencies (Figure 32)



a)



b)

Figure 32: Example of an OFC sensor a) with its time domain response b).

As a result of implementing an orthogonal frequency coding, each OFC sensor can be built with its own unique time and frequency response, allowing for reading and post-processing of the data from several sensors at the same time on the same frequency band.

6.3 Sampling and reconstruction theory

To avoid aliasing during the reconstruction of a digital signal, the sampling rate needs to be chosen according to certain rules. Band pass sampling, utilized on receiver subsystem, performs digitation and frequency shift of the reconstructed signal at the same time. For a signal with a center frequency of f_c and a bandwidth of B, the frequency spectrums of the analog and sampled signals is illustrated on Figure 33.

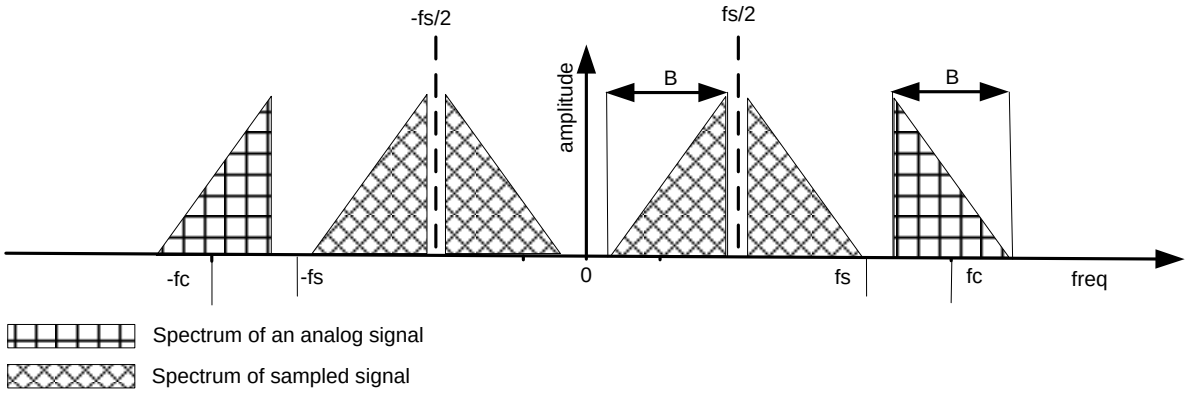


Figure 33: Process of reconstructing of the under-sampled signal.

The sampled signal produces harmonics on every $m * \frac{f_s}{2}$ (m is an integer) [11]. For aliasing-free digitation of the signal, sampling frequency needs to be

$$f_s \leq \frac{2f_c - B}{m} \qquad (34)$$

to avoid intersection of the positive and negative harmonics on the 'inside' (see Figure 34).

To avoid overlapping of the harmonics on the 'outside' f_s needs to satisfy

$$f_s \geq \frac{2f_c+B}{m+1} \qquad (35)$$

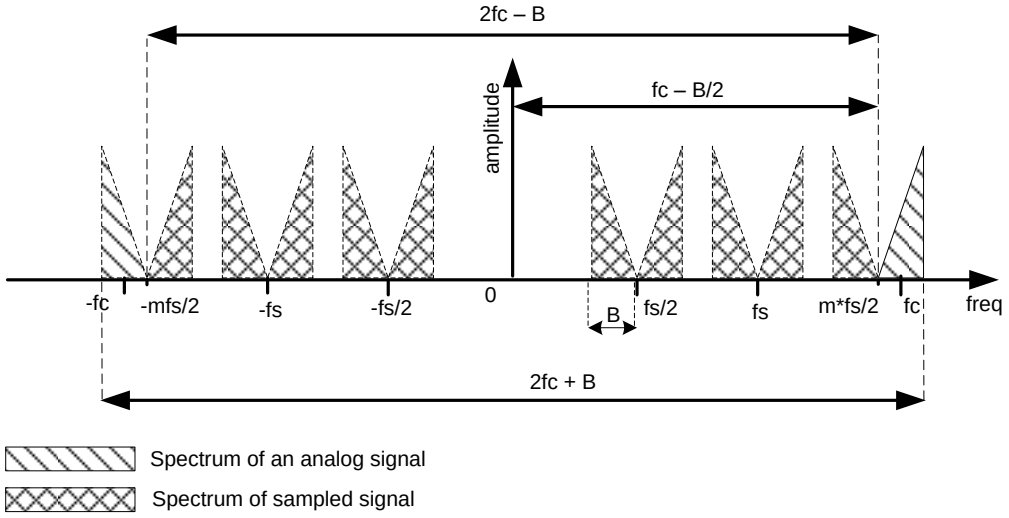


Figure 34: Anti-aliasing conditions for under-sampled signal.

As can be seen on the figure above, a high sampling rate is not always beneficial. Often, the sampling frequency is chosen as the lowest frequency satisfying Equations 34 and 35 and $f_s \geq 2B$ (Nyquist criteria) [12]. For the system built for this thesis, a sampling rate of 80 mega samples per second (MSPS) was chosen (Equation 35).

$$\frac{2*140+20}{3+1} \leq 80 \leq \frac{2*140-20}{3} \rightarrow 75 \leq 80 \leq 86.7 \qquad (36)$$

Table 7 contains the sampling frequency bands that will result in aliasing-free operation

Table 7: Set of clock frequencies resulting in aliasing-free sapling of the signal.

m	fmin	fmax
1	150	260
2	100	130
3	75	86.667
4	60	65
5	50	52
6	42.857	43.333

Grey – not supported by hardware
Yellow – optimum sampling frequencies
Green – guard band is too small
Violet – will result in overlap

6.4 Integration and correlation techniques

Pulse compression radar was one of the first applications envisaged for SAW devices. The energy of the transmitted signal is equal to its power multiplied by signal duration [8]. To maximize SNR, the energy of the signal needs to be increased, which can be achieved either by maximizing the transmitter output power, or by increasing the transmitted pulse width. Increasing the pulse width results in reduction of the bandwidth, which often cannot be acceptable. The pulse compression algorithm enables the pulse length to be increased without reducing the bandwidth. The system generates long frequency coded signal. A matched filter in the receiver compresses the frequency coded signal into a smaller duration without losing any information. The function of the SAW device was to process a frequency-swept, or chirped, signal in such a way as to maximize its signal-to-noise ratio. This process is called correlation and can be symbolically illustrated as on Figure 35

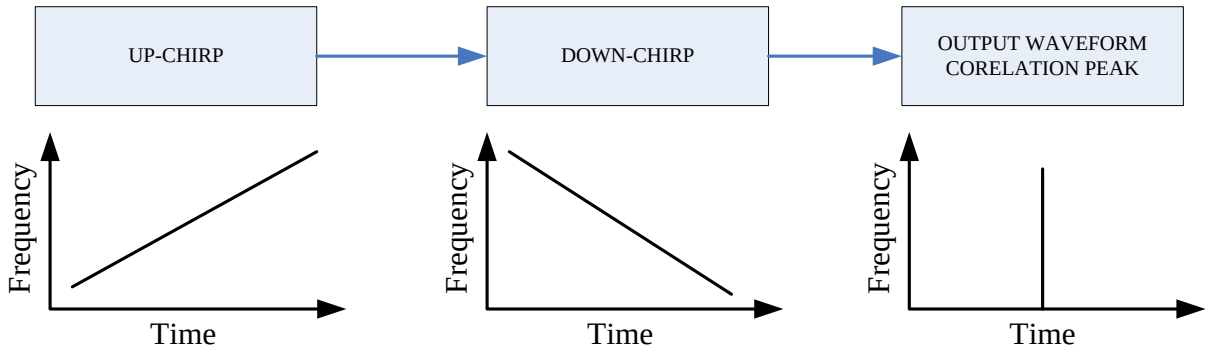


Figure 35: Idealized symbolic block diagram illustrating pulse compression technique.

The output waveform has a narrow peak called correlation peak. The width of the correlation peak is approximately $1/B$, where B is the bandwidth of the input signal. Because the correlation peak width is much smaller than the input pulse length, the described technique is called pulse compression. Utilizing described technique the signal energy can be increased by factor $T * B$ where T is the chirp pulse length. The SNR of the output filter increases (comparable to conventional gated RF burst) by the same factor $T * B$ often referred to as 'processing gain'.

SAW devices performing correlation of the received signal with the down-chirp transfer function were invented in the absence of digital filters. With the use of modern DSP, all signal processing can be done on the computer. A mathematical model to simulate the generation process, coding and decoding of the signal is built and discussed in Chapter 7. A comparison with the experimental results will be provided in Chapter 7 as well.

Integration is the process of combining multiple samples of the signal, each contaminated by noise or other interference, to average down the noise and obtain a single sample that has

higher SNR [13]. Coherent integration assumes that the useful signal has the same phase, pulse-to-pulse. The amplitude of the coherently integrated signal increases by a factor of N, where N is the number of integrated samples. Assuming zero mean, white noise, the noise component's amplitude after integration only increases by the factor of $\sqrt{N}$. SNR of the coherently integrated signal can then be written as

$$SNR_n = \frac{N^2 * A^2}{N * \sigma_w^2} = N * SNR_1 \qquad (37)$$

where A is the amplitude of the signal, σ_w is the noise variance, SNR_n in the resulting SNR and SNR_1 is the SNR of the single sample. The number of integrated samples N is often referred to as an 'integration gain'.

CHAPTER 7: EXPERIMENTAL RESULTS

The purpose of the conducted experiments was to prove the system's functionality and to demonstrate the applicability of the algorithms used for post-processing of pulse-compressed waveforms. The testing of the ISM915 band interrogator had to be conducted in the absence of the ISM915 frequency interval OFC sensors. A proof of the functionality of the system, however, needed to be performed. This chapter will present the measurement results and their analysis.

7.1 DUT characterization

Previously built broad band OFC sensors [14] with one of the chips tuned on 919MHz was chosen as an interrogation target. An OFC device consists of multiple chips, each tuned on a specific frequency. To measure the sensor's frequency response, the device was mounted on the patch antenna. A second antenna was attached to spectrum analyzer. The frequency response of the device is shown on Figure 36.

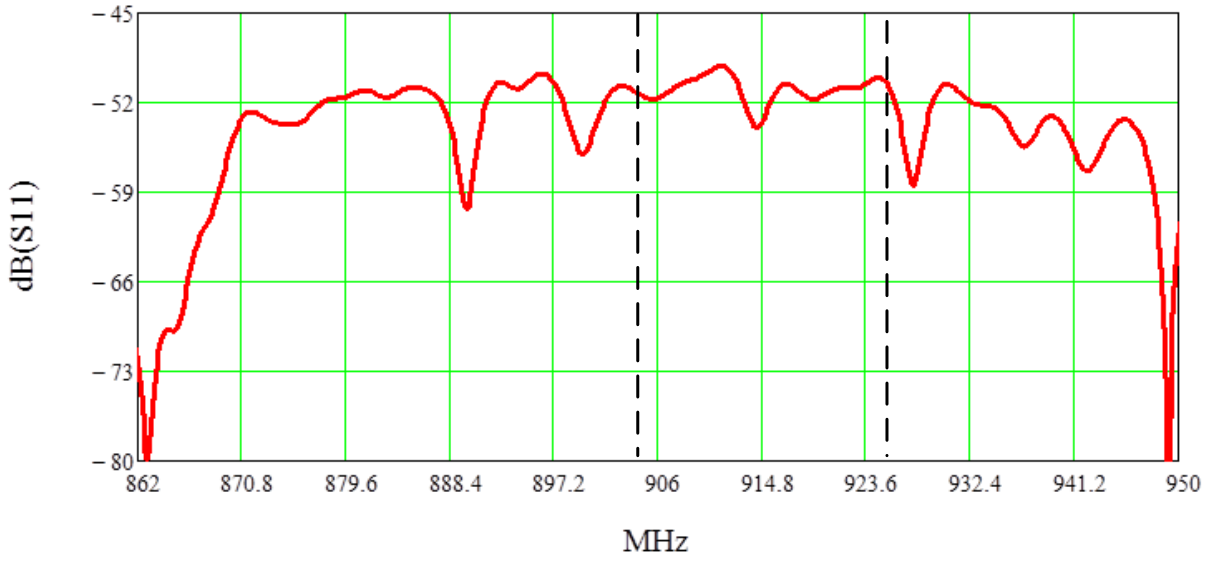


Figure 36: Frequency spectrum of DUT. The frequency band covered by the designed interrogation system is shown inside of the dotted line.

An OFC sensor consisted of five chips coded with different frequencies. Shown in the figure above, all five chips can be individually recognized. The third and the fourth chips of the device will be covered by the transmitted signal.

Receiving and transmitting antennas were located 1m from the sensor. A total of 20 samples were taken, results were compared and proved to be identical. A spectrum of the received signal is plotted on Figure 37.

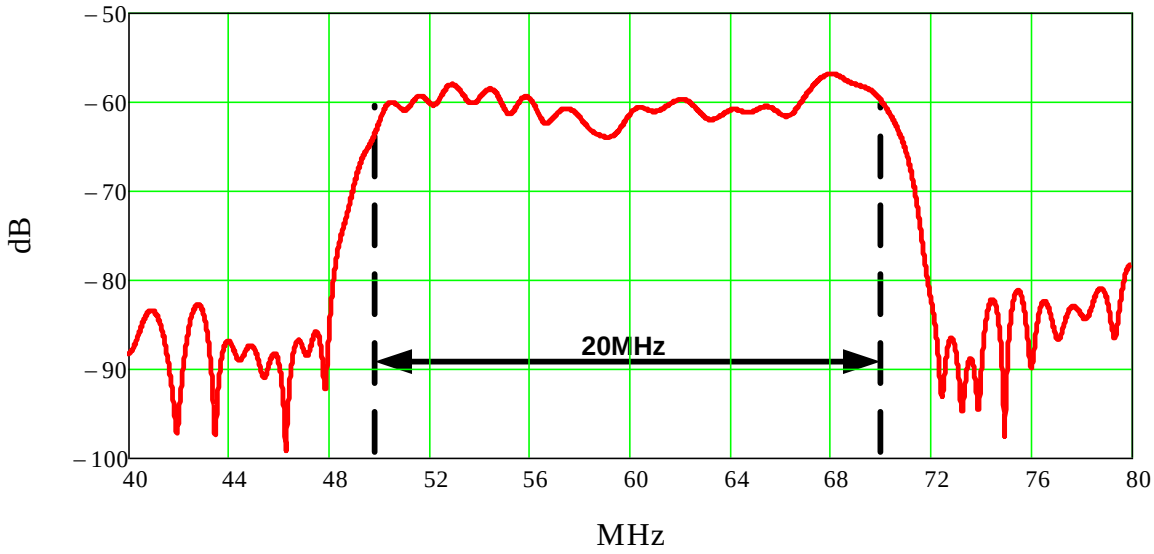


Figure 37: Spectrum of the received signal modulated by the SAW OFC sensor. A fast Fourier Transform was performed to obtain a spectrum from the sampled data. The 20MHz receiver's bandwidth is shown inside of the dotted line.

As was described in Chapter 6, the spectrum of the band-pass sampled signal, is located around $f_{sampling}/2$. The negative, inverted harmonic is situated between DC and $f_{sampling}/2$ and positive harmonic is plotted between $f_{sampling}/2$ and $f_{sampling}$. It can be seen that the amplitude of the spectrum of the received signal repeats the contour of the spectrum of the DUT.

7.2 Matched filter and correlation response

To maximize SNR and for further processing, the received waveform needs to be filtered with the matched filter [15]. For a waveform $x(t)$ defined over the period $0 \leq t \leq \tau$ the matched filter can be described as

$$h(t) = x^*(-t) \quad -\tau \leq t \leq 0 \qquad (38)$$

where τ is the length of the response.

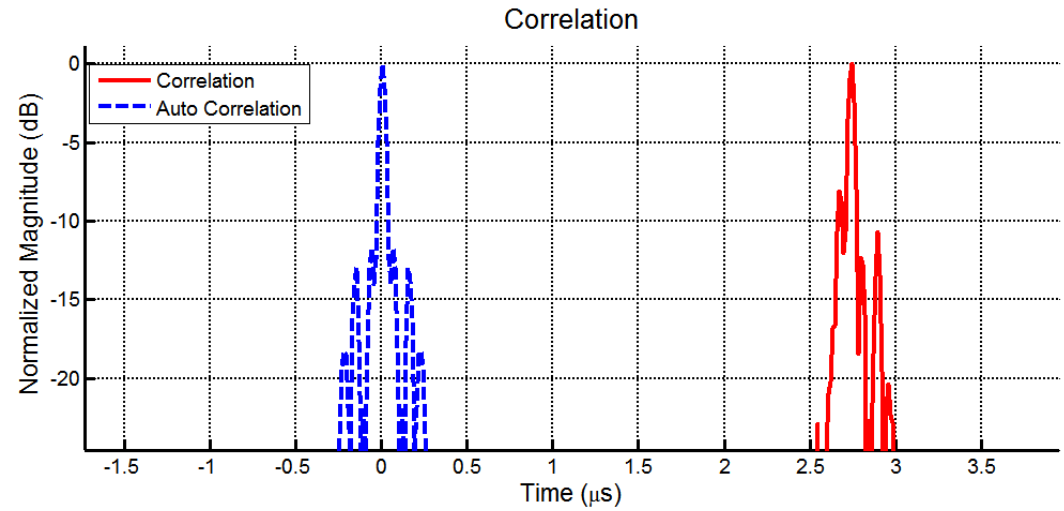
On receive, the matched filter $h(t)$ is convolved with the received waveform $x_r(t)$ to yield the output $y(t)$, or

$$y(t) = \int x_r(\alpha) * h(t-\alpha)d\alpha \qquad (39)$$

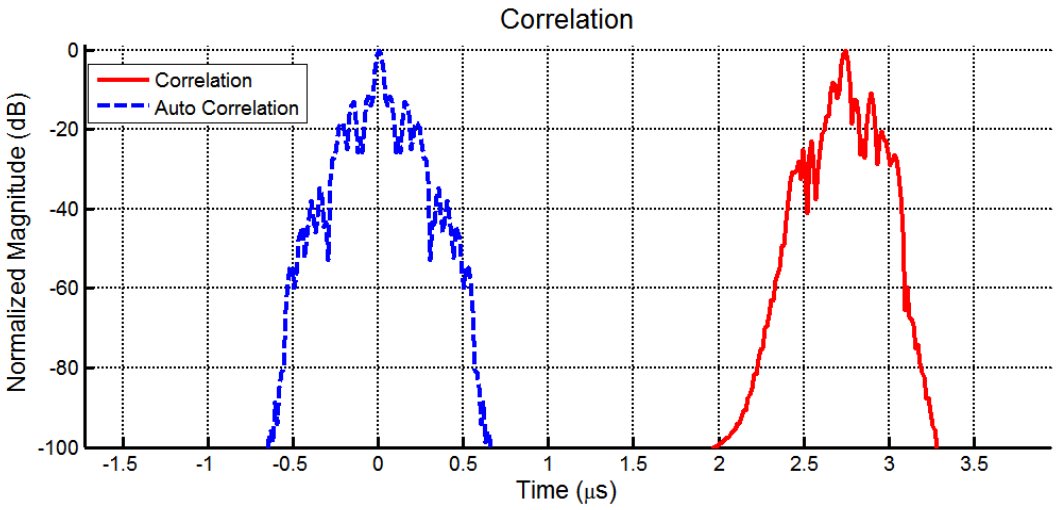
where α is a variable of integration. Substituting Equation 38 into Equation 39 yields

$$y(t) = \int x_r(\alpha) * x^*(\alpha - t)d\alpha \qquad (40)$$

The matched filter was defined in Matlab mathematical software used for post-processing. The resulting waveform was then correlated against a frequency limited model response of the DUT. The device was previously characterized and the existing model was used. The results of the correlation of the receiver signal with the model, versus the auto-correlation of the received signal are plotted on Figure 38.



a)



b)

Figure 38: Plot of the correlation of the received signal against the mathematical model of the device response (red) versus auto-correlation of the received signal (blue). a) magnified view, b) distant view.

The peak of the correlation is seen at the time pertaining to the measured chip unique location specified by the OFC code of the device. The nearest side lobe is observed at -8dB, which

corresponds to a close correlation of the mathematical model of the device with the experimental data. The conclusion can be made, that the received signal is distortions-free and as predicted.

7.3 Multiple device operation measurements

Four temperature sensors with known parameters [3, 9, 10, 16] were chosen for multiple devices reading experiment. The response of each sensor comes at a different time without overlapping the reflections from other devices as shown on Figure 39.

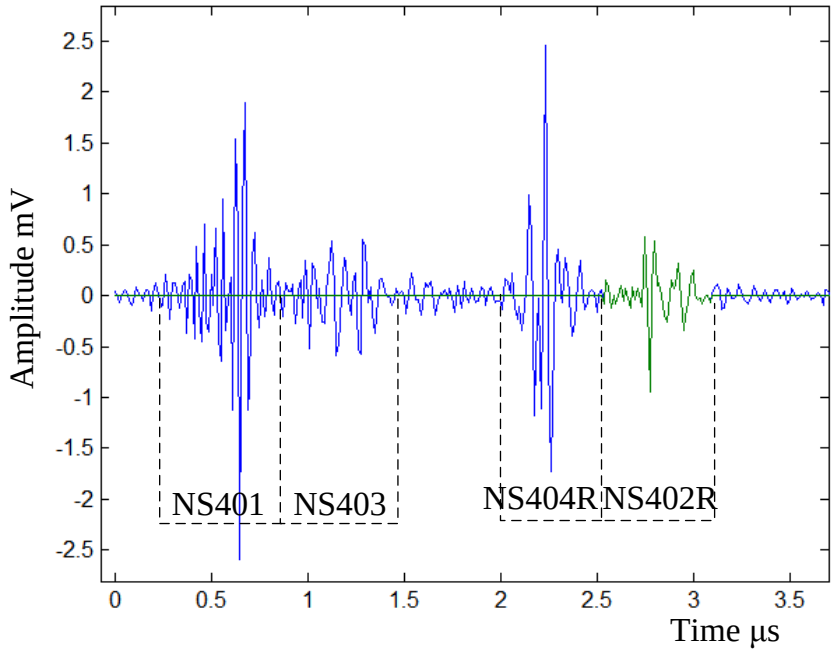
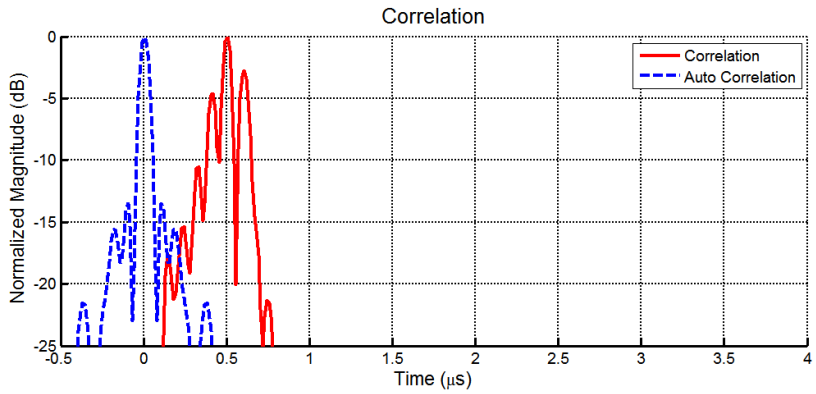


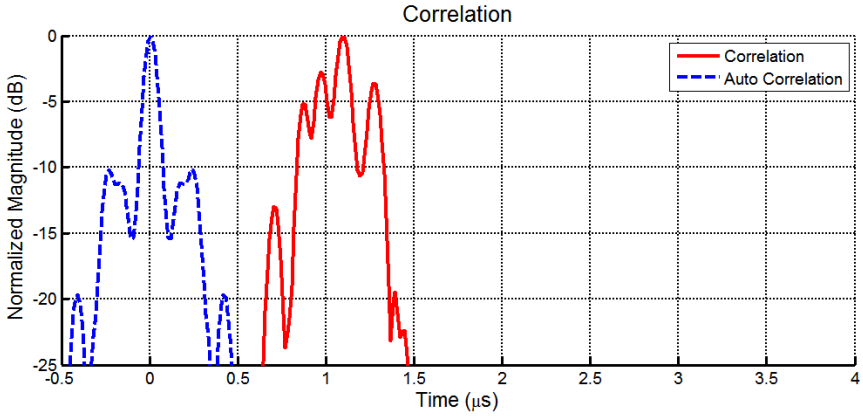
Figure 39: Time domain response of measurement of four OFC temperature sensors. Individual sensor responses, shown between dotted lines are gated with the software

After gating, each particular signal is processed individually as it was shown in section 7.2.

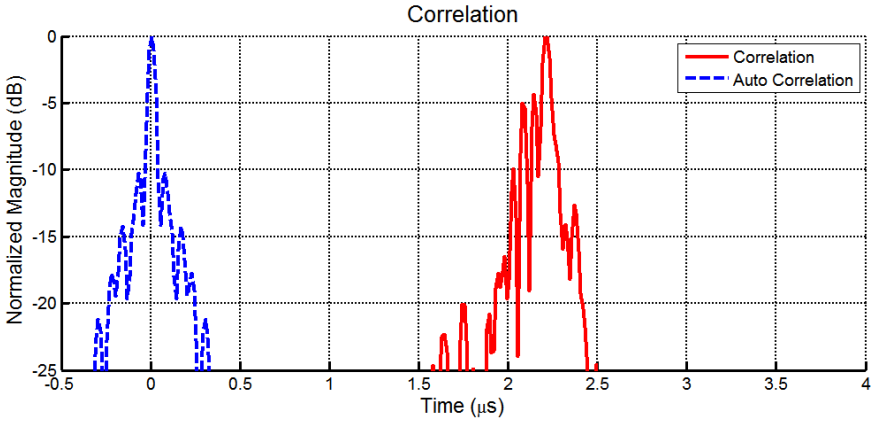
Correlation peaks of four devices are shown on Figure 40.



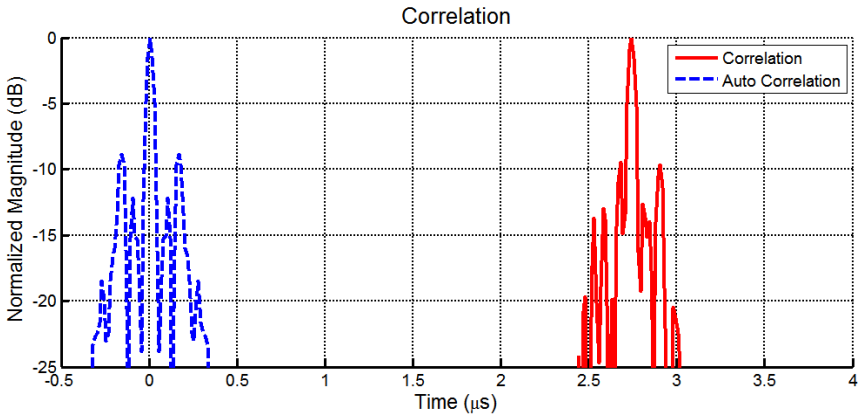
a)



b)



c)



d)

Figure 40: Correlation peaks of measurement of four OFC temperature sensors at the same time. a) correlation peak of device NS401, b) correlation peak of device NS403, c) correlation peak of device NS404R, d) correlation peak of device NS402R.

The time of the occurrence of the correlation peak of every DUT matched the characterized response time of the interrogated chip of the device. The side lobes of the correlation peaks of the devices NS401 and NS403 showed to be relatively high, which is a sign that the matched filter and the obtained measurement did not meet exactly. For temperature extraction purposes, the side lobes of the correlation plots need to be brought down, however this task will not be the part of this thesis. The ability of the system to interrogate four sensors at the same time was demonstrated.

7.4 Pulse-to-pulse integration of the received signal

In order to increase SNR the received signal can be integrated. The integration of the received waveform can serve as a good measure of the stability of operation of the

communication system. Coherent integration would not be possible if there is phase or switching mismatch within the system.

The spectrum of the single measurement versus integration of 12 pulses is plotted on Figure 41. The increase of signal power is approximately 16dB what corresponds to an integration gain of 2.8 and not to 12, as it supposed to be according to Equation 37 in Chapter 6.

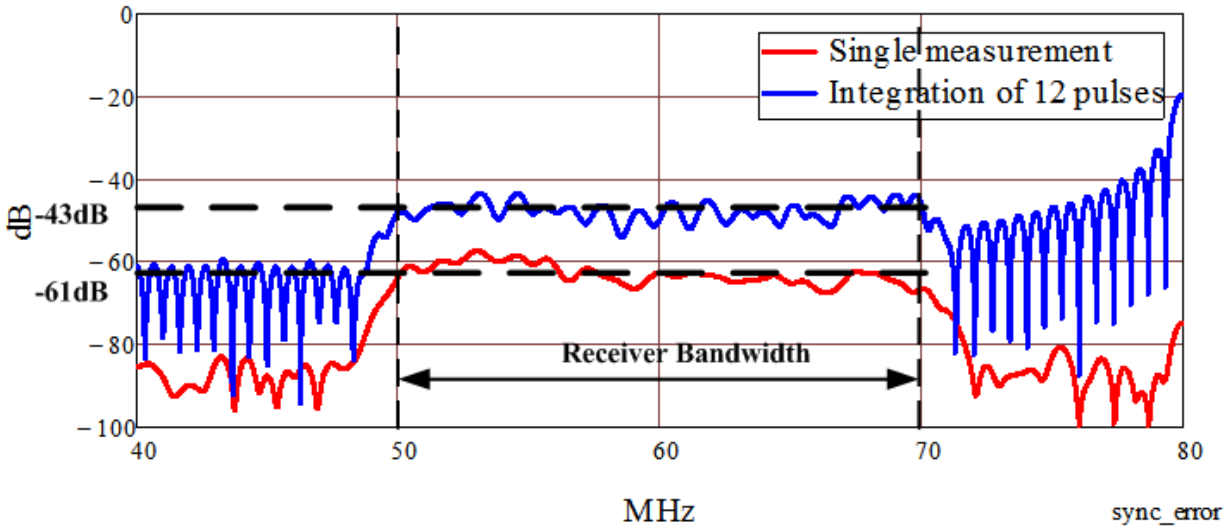


Figure 41: Spectrum of the DUT measured with the interrogation system. Single measurement spectrum versus spectrum of the integration of 12 consecutive pulses.

Time domain data was plotted on Figure 42 to determine the reason of integration gain reduction.

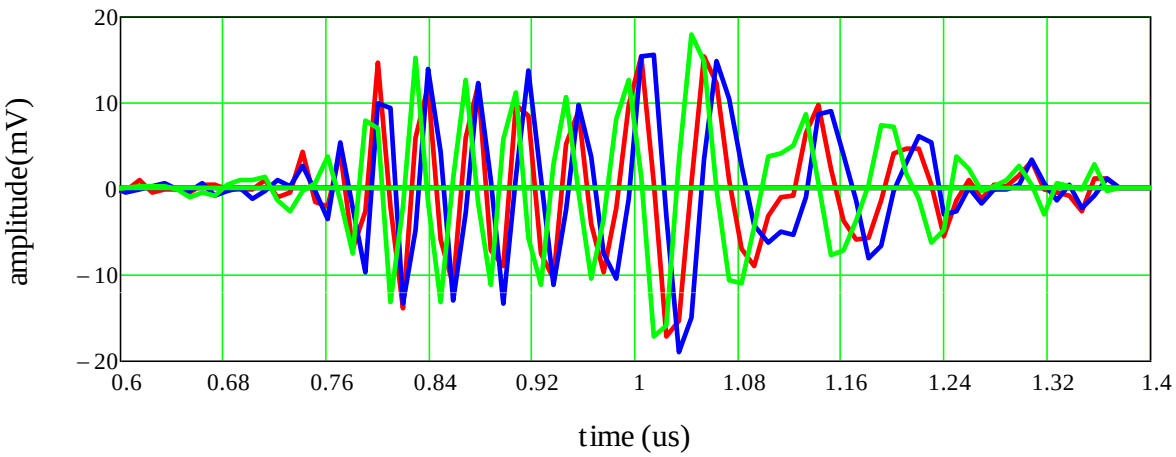


Figure 42:Time domain response of the DUT. Three measurements with worse mis-synchronization are chosen for illustration purposes.

From the processing of over one hundred samples, it was determined that worth mis-synchronization error is ranging close to 19ns. To decrease synchronization error to a feasible limit, a high frequency operating control system is necessary. Synchronization error, discussed in Chapter 4, has a direct effect on the initial, time zero point. A new approach is necessary in order to solve this issue, and, perhaps, this will be a topic for future work.

Correlation of the result of integration of 12 pulses is shown on the Figure 43.

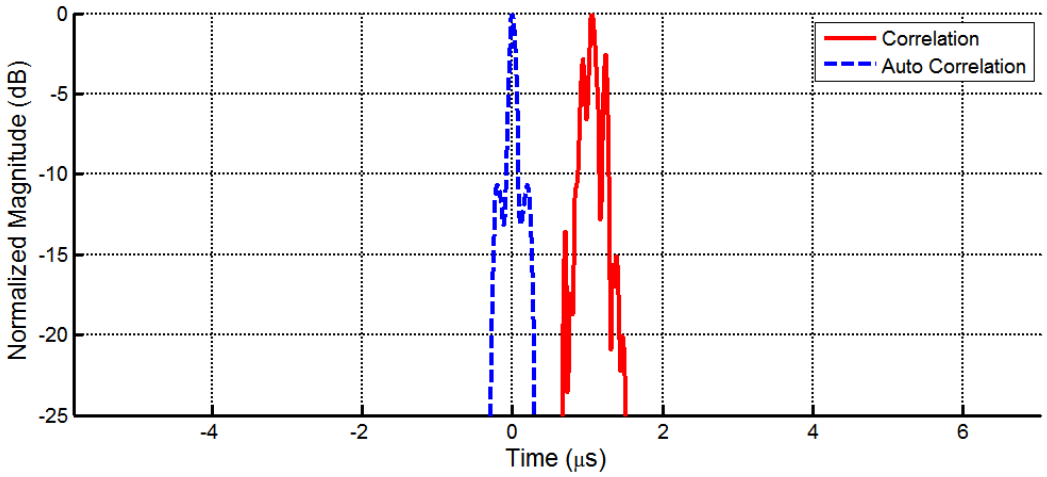


Figure 43: Correlation peaks of auto correlation of result of integration of 12 pulses – blue, and result of an integration of 12 pulses with a matched filter – red.

The peak-to-side lobe ratio decreased after integration was performed. Synchronization error needs to be decreased in order to bring the side lobes down. An experiment proved that integration of the signal received with the interrogation system can be performed, and the data can be processed.

CHAPTER 8: CONCLUSION

The thesis discusses the design of the synchronous communication system for SAW sensors interrogation. Developed to comply with ISM915 regulations, the system has center frequency of 915MHz, bandwidth of 20MHz and peak power of +25dBm. A broad band SAW sensor interrogation system with center frequency of 915MHz was previously reported [5], but the design of the ISM compliant system was not previously explored.

The scope of the thesis includes design, choosing the parts for, and building of the signal generator, amplifier, receiver, common clock circuitry, control system, and the power supply. The system is designed to have a programmable, adjustable transmission frequency ranging from 450MHz to 1.2GHz. The software, developed as a part of this thesis, enables user to generate a desirable frequency modulated signal with simplified GUI. The device was fit into compact presentable body and equipped with an internal power supply. Key system parameters are shown in Table 8.

Table 8: A parameters featured by the designed interrogator.

Transmitter Parameter	Value	Receiver Parameters	Value
Gain	47dB	IF	140MHz
Max. power output	+27.5dBm	BW	20MHz
NF	4.5dB	NF	15.9dB
Center freq.*	915MHz	Gain	34dB
BW*	26MHz	MDS	-83.631dBm
Tx antenna gain	2dB	Dynamic range	-101dBm to -29dB,
Radiation pattern	Isotropic	Sampling frequency	80MHz
Frequency modulation	Programmable	Max. acquisition rate	70 samples per second
LO frequency*	775MHz	System's package size	17"-14"
IF center frequency*	140MHz	System requirements	Windows XP/7 USB port
Target (sensor) loss	22dB	Rx antenna gain	2dB
Target antenna gain	2dB		

*Note: parameters marked with an asterisk (*) sign are programmable. Within this thesis the system only characterized on the listed frequencies.

The functionality of the system was proven by comparison of the mathematical model of the target response with an experimental data.

Existing software [11] was adapted for processing of the sampled signal. With the explored technique, it has been shown that band-pass sampling can be used for analog-to-digital conversion of the received signal without the loss of coded information. The market's most inexpensive components were used, which allowed for very low final price of the system.

Increase of the SNR in the receiver can be achieved by exchanging the currently equipped amplifier for a low noise prototype. An increase of the range of the measurement can be achieved by the increasing the power of the transmit amplifier to the maximum allowable by ISM915. Even further increase of the range of operation can be realized if another amplification cascade is added on the receiver side. An adaptive feed-back loop needs to be utilized for protection of the receiver from excessive amplitude in that case. The integration gain of the

system can be increased if the operational clock of the control FPGA is increased. For an ideal synchronous operation of the system pulse-to-pulse, replacement of currently used control system with a high speed FPGA is necessary.

REFERENCES

[1] "FCC Online Table of Frequency Allocations," ed: FEDERAL GOVERMENT, 2011.

[2] B. M. Cabalfin Santos, *SAW reflective transducers and antennas for orthogonal frequency coded SAW sensors [electronic resource] / by Bianca Maria Cabalfin Santos*. Orlando, Fla: University of Central Florida, 2009.

[3] N. Kozlovski, *Passive wireless SAW sensors with new and novel reflector structures [electronic resource] : design and applications / by Nikolai Yurevich Kozlovski*. Orlando, Fla: University of Central Florida, 2011.

[4] J. G. Proakis, *Digital communications / John G. Proakis*, 4th ed. ed. Boston: McGraw-Hill, 2000.

[5] N. Y. Kozlovski, M. W. Gallagher, and D. C. Malocha, "SAW sensor correlator system performance parameters," in *Frequency Control and the European Frequency and Time Forum (FCS), 2011 Joint Conference of the IEEE International*, 2011, pp. 1-6.

[6] G. Gonzalez, *Microwave transistor amplifiers : analysis and design / Guillermo Gonzalez*, 2nd ed. ed. Upper Saddle River, N.J: Prentice Hall, 1997.

[7] D. M. Pozar, *Microwave engineering / David M. Pozar*, 2nd ed. ed. New York: Wiley, 1998.

[8] D. P. Morgan and C. Ebooks, *Surface acoustic wave filters [electronic resource] : with applications to electronic communications and signal processing / David Morgan*, 2nd ed. ed. Amsterdam ; London: Academic Press, 2007.

[9] D. C. Malocha, J. Pavlina, D. Gallagher, N. Kozlovski, B. Fisher, N. Saldanha, *et al.*, "Orthogonal frequency coded SAW sensors and RFID design principles," in *Frequency Control Symposium, 2008 IEEE International*, 2008, pp. 278-283.

[10] D. C. Malocha, D. Puccio, and D. Gallagher, "Orthogonal frequency coding for SAW device applications," in *Ultrasonics Symposium, 2004 IEEE*, 2004, pp. 1082-1085 Vol.2.

[11] N. Y. Kozlovski, D. C. Malocha, and A. R. Weeks, "A 915 MHz SAW Sensor Correlator System," *Sensors Journal, IEEE*, vol. 11, pp. 3426-3432, 2011.

[12] R. G. Lyons, *Understanding Digital Signal Processing*, 2nd Edition ed.: Prentice Hall, Mar 15, 2004

[13] M. I. Skolnik, *Radar handbook / editor in chief, Merrill I. Skolnik*, 2nd ed. ed. New York: McGraw-Hill, 1989.

[14] N. Saldanha, *Modeling, design and fabrication of orthogonal and psuedo-orthogonal frequency coded SAW wireless spread spectrum RFID sensor tags [electronic resource] / by Nancy Saldanha*. Orlando, Fla: University of Central Florida, 2011.

[15] M. A. Richards, *Fundamentals of radar signal processing / Mark A. Richards*. New York: McGraw-Hill, 2005.

[16] D. C. Malocha, N. Kozlovski, M. Gallagher, N. Saldanha, and D. Gallagher, "SAW wireless RFID correlator system design," in *Ultrasonics Symposium (IUS), 2010 IEEE*, 2010, pp. 269-272.