

TRIGGERED SWEEP GENERATORS USING
MODERN INTEGRATED CIRCUITS

BY

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LIST OF FIGURES

Figure	Page
1. Block Diagram of 555 Integrated Circuit Timer, with External Component Connected for Monostable Operation	4
2. Linear Ramp Generator, using 555 IC and FET Constant-Current Source	8
3. Field-Effect Transistor Constant Current Source, Output Current Versus Source Resistance, 2N5486	11
4. MHTL NAND Gates in a Schmitt Trigger Configuration	20
5. Using the 555 as a Trigger	20
6. The 555 Timer as a High Speed Trigger with DC Trigger Level Control	20
7. Bistable Multivibrator used for Gating of Trigger Pulse ..	25
8. Conventional Logic Gating of Trigger Pulse	25
9. Simple Diode Clamping of Trigger Pulse	25
10. Triggered Sweep System using TTL 7400 Quad 2-Input NAND Gate Trigger	27
11. Simple, Low Cost Sweep using High-level MHTL MC672 Quad 2-Input NAND Gate Trigger	29
12. Complete Triggered Sweep System using only 555 Integrated Circuits and FETs	31

TABLE OF CONTENTS

	Page
LIST OF FIGURES	iv
ABSTRACT	1
THE 555 IC TIMER	3
Basic description and device specifications	
OBTAINING A LINEAR SWEEP FROM THE 555.....	7
Circuit configuration, requirement of FET constant-current source, use of FET as current sources, output sweep frequency and linearity, output buffering	
THE TRIGGER	17
Schmitt trigger using 15 volt MHTL gates, the 555 as a Schmitt, tunnel diode and TTL trigger	
TRIGGER PULSE-FORMING AND GATING	22
Basic requirements, pulse-forming, multivibrator gate, NAND gate, diode gate	
COMPLETE TRIGGERED SWEEP SYSTEM	26
Many versions possible, hi performance TTL circuit, simple hi-level MHTL circuit, unique hi-level 555 circuit, a Comparison of Triggered Sweep Systems	
SUMMARY	33
REFERENCES	35

ABSTRACT

The oscilloscope is undoubtedly one of the most important tools in any electronics shop. Presently there are many relatively inexpensive oscilloscopes available, but triggered sweep capability is still reserved for those oscilloscopes costing more than 200 - 500 dollars. The goal of this project was to develop a respectably performing triggered sweep system at a low enough cost to allow inclusion of this valuable feature in any oscilloscope.

Two of the most important specifications of an oscilloscope are the bandwidth of the vertical amplifier, and the maximum sweep frequency. The broad class of "inexpensive oscilloscope" would include those with a maximum vertical response of 500 KHz to 5 MHz, and a maximum sweep rate of 50 KHz to 500 KHz. Most of these oscilloscopes would not have triggered sweep capability. For about double the cost, the next step upward would be a semi-professional triggered-sweep oscilloscope having a typical vertical response of 15 MHz and a sweep to roughly 2 MHz (500 nsec). Using these classifications as guidelines, a "respectably performing" triggered sweep for inexpensive oscilloscopes may be loosely defined as one having a 500 KHz (2 usec) sweep, triggerable to at least 5 MHz. Depending on actual cost and application, greater or lesser performance could be considered entirely acceptable.

A number of design variations are possible, all of which appear to be a fraction of the cost and complexity of previous designs having comparable specifications. Making this possible are integrated circuits in

general, and a modern linear IC "timer" in particular. This report first describes this timer, then uses it as the main element in the generation of a linear ramp. Several trigger and gating circuits are then described. Finally, several of these subcircuits are combined to form three (out of many possible) complete triggered sweep generator systems. As an example of the results, the most expensive circuit costs about 15 dollars in single quantity, yet offers 10 volt per 200 nsec sweep rates, trigger capability from DC to above 15 MHz, trigger level and phase control, and blanking pulse output.

THE 555 IC TIMER

At the heart of these triggered-sweep designs is a low cost "linear" IC, the 555 Timer.¹ Designed by Interdesign Inc., and made popular through distribution by Signetics Corp., the little eight-pin "half-DIP" plastic version costs less than 75 cents in quantities of 100.

Figure I shows the functional diagram, in the common one-shot (monostable) configuration. This is basically the configuration which will be used later in the sweep generator design. A negative-going pulse on pin 2 sets the flip-flop which drives the output of the power inverter high. At the same time, the transistor across the timing capacitor is turned off and the capacitor is allowed to charge at a rate determined by the RC. When the capacitor reaches two-thirds of the supply voltage, the comparator changes state and resets the flip-flop, driving the output low. The transistor across pin 7 quickly discharges the capacitor and the flip-flop is readied for another input trigger pulse. A key feature is the fact that the bistable flip-flop makes the device insensitive to incoming trigger pulses during the charge time of the capacitor.

In various configurations, the circuit can be used as a precision timer, free-running or one-shot pulse generator, sequential timer, pulse width or pulse position modulator, missing pulse detector, frequency divider, etc. The specifications of this versatile little device include typical temperature coefficients of about 40 ppm/°C, initial RC timing accuracies of 1%, and a comparator input impedance high enough to allow resistors of several megohms to be used for long timing intervals. The

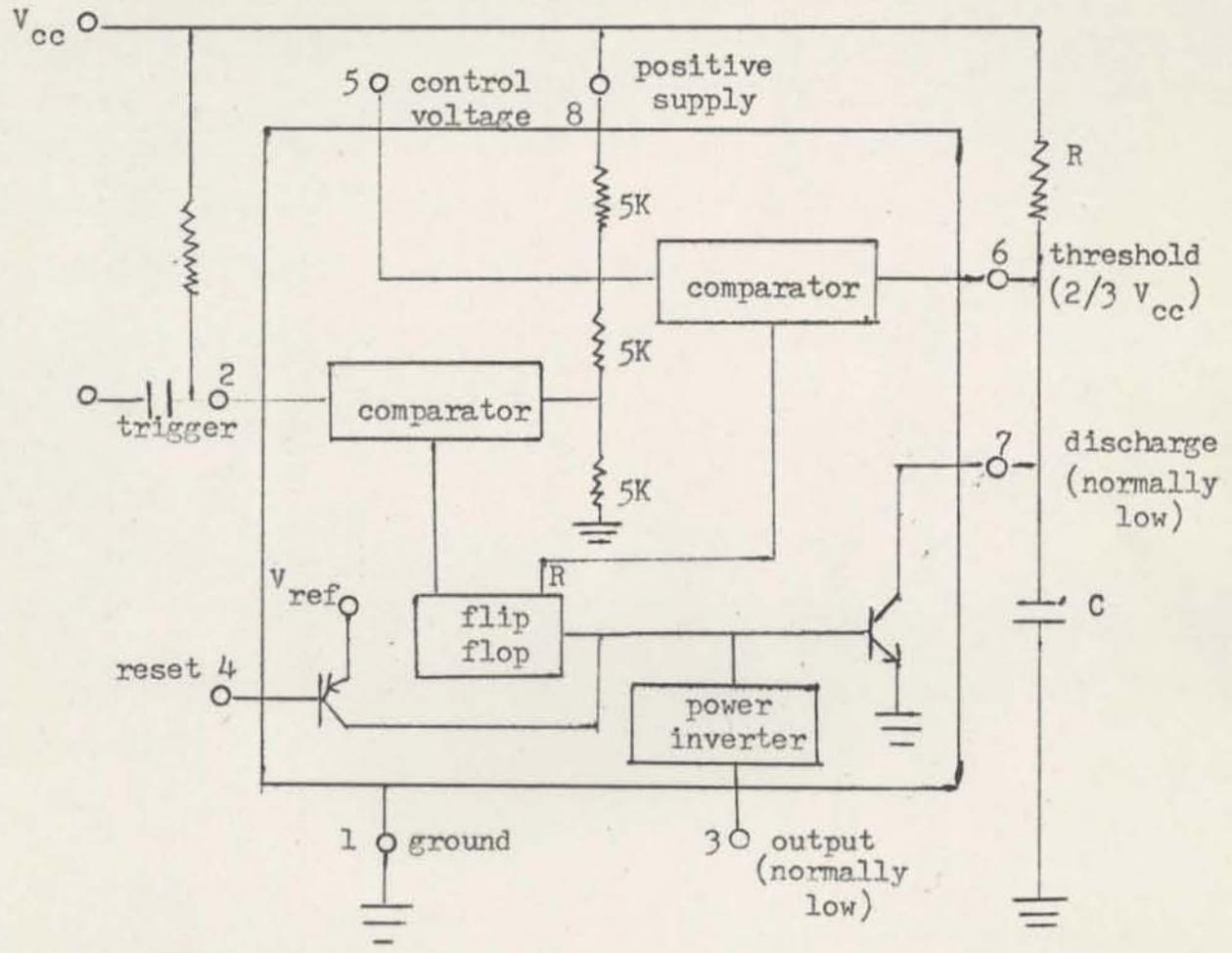


Figure 1. Block Diagram of 555 Integrated Circuit Timer, with External Components Connected for Monostable Operation

two transistors in the inverting output stage can source or sink up to 200 ma, with maximum rise and fall times of 50 nsec at 50 ma. The internal voltage divider consists of three 5K ohm resistors in series, giving nominal trigger levels of $1/3 V_{cc}$ and $2/3 V_{cc}$ for pins 2 and 6 respectively. Since the internal voltage divider makes the comparator trip point and the capacitor charge rate vary in the same manner for supply variations, the sensitivity to supply variations is only 0.01%/volt. These specifications are good for single-ended supplies from 5 volts to 15 volts. Current drain is around 3 ma with 5 volt supply, and 10 ma at 15 volts.

Timing can be adjusted over a wide range. Changing the capacitor allows more than an eight-decade range, while changing R alone allows a four-decade range. An external control voltage to pin 5 will allow a 3:1 variation, and is often used for "modulation" of the device. The time in high state is given by the equation: $T = 1.1RC$, for the circuit shown. In some applications, one may wish to control discharge rate of the capacitor as well as charge rate, by tying the capacitor to pin 6 and adding another resistor between 6 and 7.

It is important to note however, that the device is ready to respond to trigger pulses the moment that the pin 6 trip point ($2/3 V_{cc}$) is reached, and therefore can be triggered back into the high state long before the timing capacitor is fully discharged. In fact, the author has found that the device can be triggered several times during discharge even with pin 6 fall-times of less than 100 nsec.

There are several characteristics that will be of particular interest during the development of the triggered-sweep circuits to follow. The input trigger threshold is within 30% of $1/3 V_{cc}$ (because of tolerance of the internal voltage divider resistors). With a pulse reaching to

0.1 V_{cc} or lower, the device will trigger on a 25 nsec pulse at 25°C, or 50 nsec at 0°C. Although the data sheet states typical output rise and fall times of 100 nsec, tests show that they are more on the order of 40 nsec for moderate and small output currents (below 20-30 ma). Propagation delay is generally 100 nsec. At normal loads and temperatures, the output will switch from .2 volts above ground, to 1.4 volts below the supply voltage, V_{cc} . Conversation with company engineers confirm that the transistor switch across the timing capacitor can safely discharge the largest capacitors without series resistance or other protection. The device was found to be somewhat noisy on sine wave triggering in the audio and sub-audio range, as might be expected. The effect is in the general order of magnitude as that observed with normal TTL logic, which tends to oscillate when the input voltage remains in the threshold region (approximately 200 mv wide) for more than about 15 nsec. However, on the high end, experimentation with the device indicated that it could be made to trigger reliably to at least 20 MHz.

This detailed introduction to the 555 Timer is necessary so that the design considerations and overall simplicity of resulting circuits could be appreciated. The next section covers design of the ramp generator stage by itself. Since this ramp stage leaves very little room for improvement, the remaining sections then deal with several different trigger designs, trigger pulse gating and differentiation, and the completed designs.

OBTAINING A LINEAR SWEEP FROM THE 555

Literature on the device dwells on the viewpoint that the pulse output from pin 3 is "the" output, and pins 6 and 7 exist with R and C mainly to set the timing interval. Since the charge-up of the capacitor is itself a non-linear ramp, and is capable of more than a 10^8 range of sweep times, it naturally becomes the new point of interest for this particular application. All that needs to be done is to provide a constant charging current to the capacitor, then pick off the resultant linear waveform with a high-impedance buffer (see Figure 2).

The sweep rate becomes a simple function of the output of the FET current source, the timing capacitor, and the trip point of pin 6. In terms of slew-rate, this can be expressed as:

$$\frac{dv}{dt} = \frac{I_o}{C} \quad dt = \frac{Cdv}{I_o} \quad (1)$$

For a 15 volt supply, the capacitor charges from 0 to 10 volts. For minimum and maximum sweep times of 200 nsec and 10 seconds respectively, and using realistic values of timing capacitance, the maximum and minimum current requirements are:

$$I_o \text{ max} = \frac{10C}{T} = \frac{10(60 \times 10^{-12})}{200 \times 10^{-9}} = 3 \text{ MA} \quad (2)$$

$$I_o \text{ min} = \frac{10C}{T} = \frac{10(1 \times 10^{-6})}{10} = 1 \text{ uA} \quad (3)$$

These values are easily within range of modern FETs selling for less than a dollar in single unit quantities.

A FET can be a very effective current source if operated with a

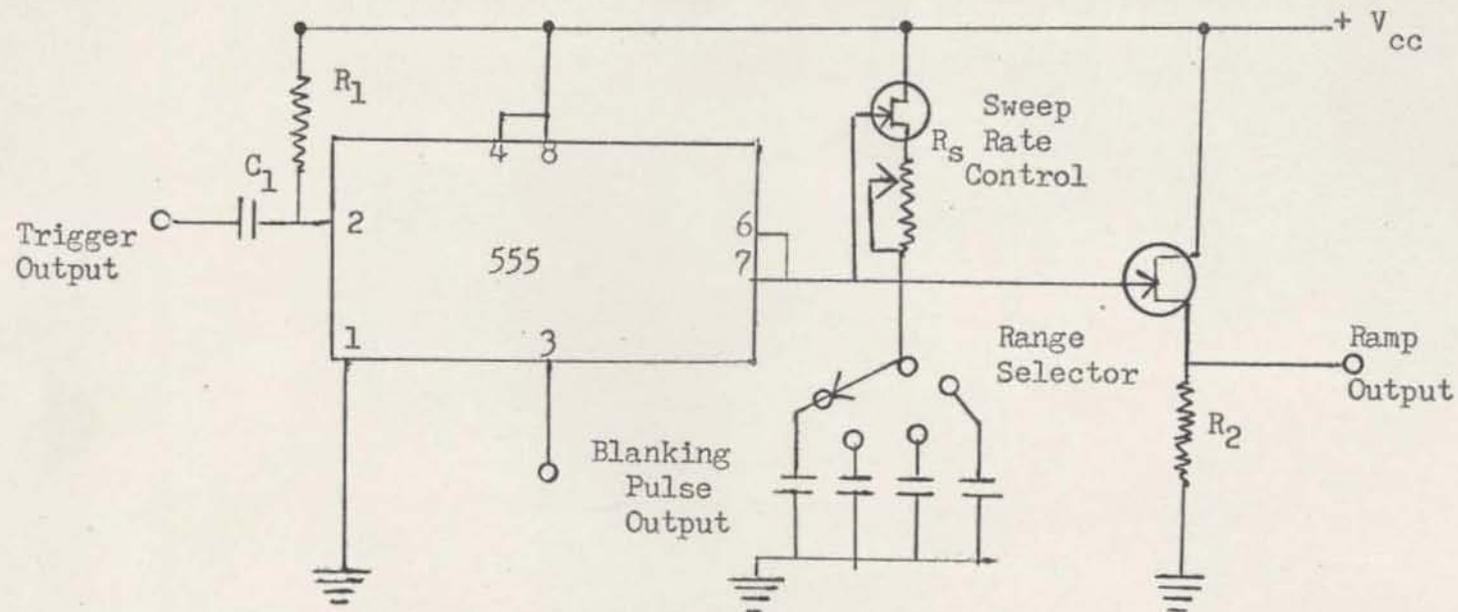


Figure 2. Linear Ramp Generator, using 555 IC and FET Constant-Current Source

drain to source voltage (V_{ds}) greater than pinch-off (V_p), and a drain current below saturation (I_{dss}). A good FET will have an effective impedance of 1/2 megohm or greater. The current versus source resistance relationship, and the resultant effective output resistance, are given by the following equations:^{2,3}

$$V_{gs} = R_s I_o = V_p (1 - \sqrt{I_o / I_{dss}}) \quad (4)$$

$$I_o = I_{dss} (1 - I_{dss} R_s)^2 / (V_p)^2$$

$$r_o = \frac{1 + R_s (g_{os} + g_{fs})}{g_{os}} \approx \frac{1 + R_s (g_{fs})}{g_{os}} \quad (5)$$

Where: g_{os} = output conductance = y_{os} output admittance

g_{fs} = transconductance = y_{fs} forward transfer admittance

g_{os} and g_{fs} decrease with decreasing I_o

It is important to note that the two FETs in this single-supply circuit will have only 5 volts drain to source as the capacitor is charged to 10 volts. For this reason it is important to choose FETs with pinch-off voltages less than this figure, so operation remains within the constant-current "pentode" region. The further that the drain current is below the device's saturation current (I_{dss}) the better the regulation - - therefore a reasonably high I_{dss} is desirable. A low output conductance and a high transconductance contribute to better performance as well. Unfortunately a high I_{dss} is invariably accompanied by a high V_p , which can make device selection somewhat difficult in this particular case, where to stay within circuit tolerances, we need a V_p of 4.5 volts or less.

Inexpensive JFETs can be found which meet requirements very well. First tests were performed with randomly selected 2N3819s and 2N5485s, and oscilloscope displays of the sweep waveforms appeared excellent.

However, actual calculations show that the somewhat tighter specifications and higher I_{dss} of FETs in the 2N5486 class made for noticeably better linearity and calibration. Although the maximum V_p of 6 volts could necessitate device selection, the vast majority of 2N5486s appear to have less than 5 volts V_p . Although not checked in depth, it appears that narrowly specified, high-current switching FETs may be ideal for this application as well.

There is nothing particularly wrong with allowing the output current to reach I_{dss} . However, as a rule of thumb, most FETs seem to provide the most uniform control of output current with values of R_s which provide output currents less than about one-third I_{dss} . Slew-rate requirements will be met with I_o on the order of 3-4ma, therefore a FET with a minimum I_{dss} of about 8 ma or more is to be desired. Since 3-4ma is the maximum current required, larger values of I_{dss} merely allow the R_s minimum to be greater, which in turn could contribute to a smoother control and possibly to a slightly "tighter" current source.

Figure 3 shows a plot of output current versus source resistance for the two extremes of specifications for the 2N5486, using equation (4). In one case, a pinch-off voltage of 6 volts was used along with an I_{dss} of 20ma. In the other extreme, 2 volts and 8 ma were used. For any given setting of R_s , it is seen that the output current could lie anywhere within a 3:1 range. In fact, it is obvious that the predictability of I_o for a given R_s is directly related to the tolerance of I_{dss} for currents greater than about one-third to one-half I_{dss} , and to the tolerance of V_p for smaller currents. This tolerance may seem unacceptably large, until one recalls that even the most expensive laboratory oscilloscopes are calibrated at only one end of each sweep range setting, and have no calibration

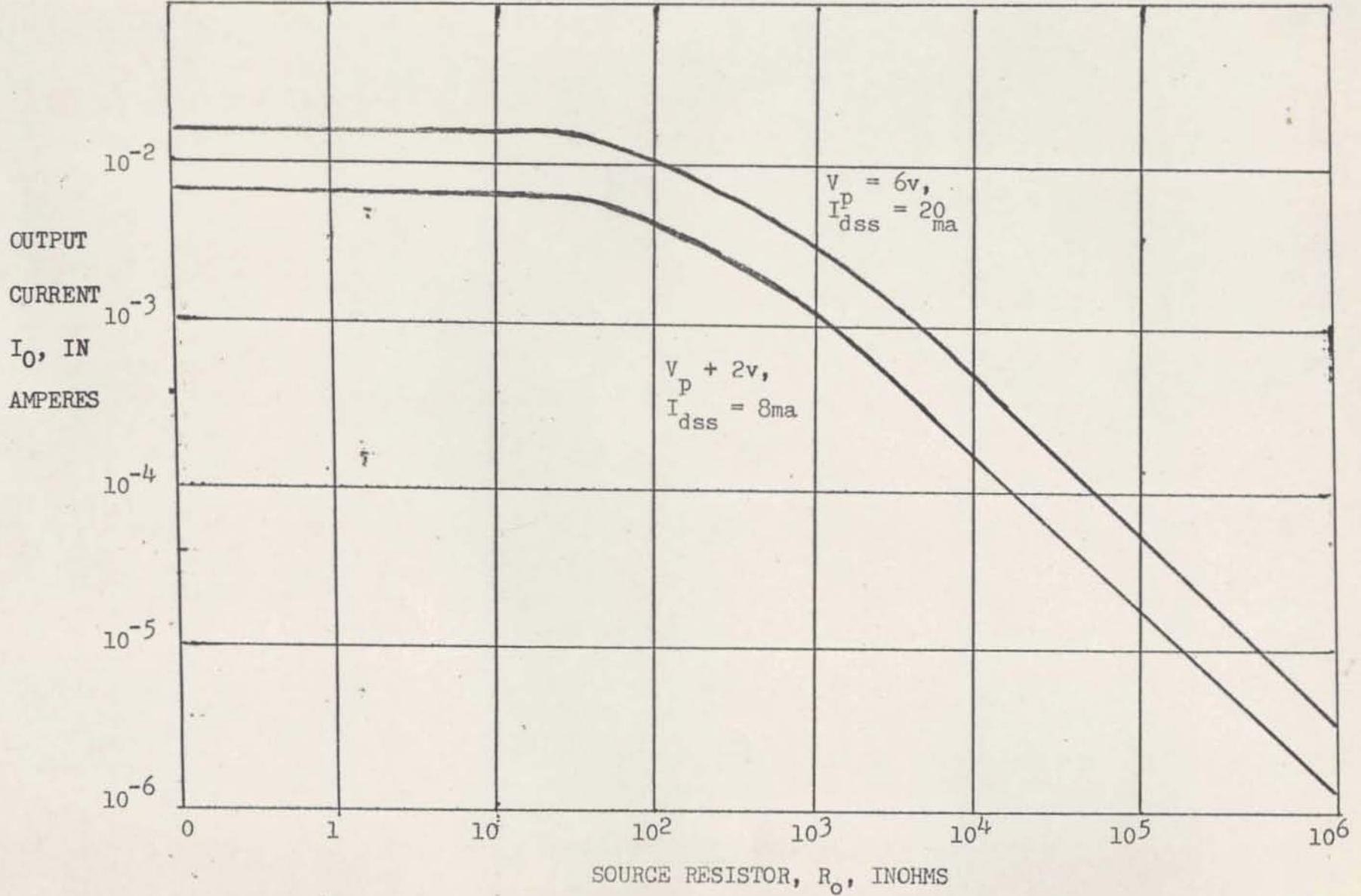


Figure 3, Field-Effect Transistor Constant Current Source, Output Current Versus Source Resistance, 2N5486

elsewhere. A small trimmer can set the maximum current very accurately, so that the sweep rate is predictable within the accuracy desired, at the minimum setting of the main R_s potentiometer. Then the only requirement on the value of the main potentiometer is that it be of high enough resistance to cover the desired range.

If good calibration is desired throughout the range of R_s , the tolerances could be narrowed greatly by grading the FET within narrower specifications. The test for V_p and I_{dss} is extremely simple, so grading could be done economically even for relatively large lots. The normal distribution of parameter values are such that the vast majority of devices fall within desirable limits. Out of tolerance devices could then be used in other parts of the circuit.

Most manufacturer's FET data sheets do not provide enough data for a complete plot of output impedance versus source resistor setting. However, minimum and maximum values of y_{fs} and y_{os} are usually specified for $V_{gs} = 0$ ($R_s = 0$). Using equation (5) these parameters lead to a worst-case r_o of 13.5K for the 2N5486 at zero R_s . At the same resistance, the best-case conditions yield an impedance of 33K.

The ramp's linearity is a direct function of the stiffness of the current source. If we defined non-linearity as the change in current during the 10 volt ramp versus the nominal current for that ramp, this worst-case condition would give:

$$I_n = 8 \text{ ma} \tag{6}$$

$$\Delta I = \Delta V / r_o = 10 / 13,500 = 0.74 \text{ ma}$$

$$NL = \Delta I / I_n = 0.74 / 8 = .093 = 9.3\% \tag{7}$$

The non-linearity for the best case comes to about 3.8%. One might expect that the non-linearity would decrease as R_s is increased,

because of the feedback action across R_s . However, some rough estimates for the 2N5486 indicate that the non-linearity actually may increase gradually to double the above values at 10 microamps output current.

For the better oscilloscopes, non-linearity below 5% would probably be desirable. The calculations for the 2N5486 are still interesting however, as they show what is obtainable with a typical, modern and popular device.

Still better devices are available. Typical switching FETs have 2 to 5 times the transconductance, very low output conductance, and higher I_{dss} - - all of which are very desirable for constant-current applications. On the negative side is the fact that specifications for a particular switching FET generally cover a wide range, and would probably necessitate grading. Since the current source is never turned off, there is no Miller-effect multiplication of drain capacitance, and since the drain is also shunted by external timing capacitance, frequency and capacitance effects are not significant concerns. For example, probably very little would be lost by selecting a FET which has very high transconductance, even at the expense of input and output capacitances. A brief look at National Semiconductor switching FETS indicates that the KE4-392 and 2N5486 may be contenders for this application.

FETs in the class of the Siliconix E232 give excellent performance. The pinch-off voltage for the E232 lies in the narrow range of 4 and 6 volts, and the saturation current is within 5 to 10 ma, improving calibration tolerances proportionately. The minimum and maximum transconductance is 2500 and 4000 umho respectively. The characteristic which contributes most to the ramp linearity is the device's low output conductance, g_{os} , of only 6 umhos maximum. The device sells for less than a dollar

in single quantities, or about 70 cents in lots of 100. Undoubtedly a more exhaustive search would yield many other such devices.

Applying equation (5), the E232's worst output impedance at zero bias is 167 kilohms. This corresponds to a worst-case nonlinearity of only 1.5%, a quite acceptable figure.

The source-follower stage is quite straight-forward. The gain, as expected, is very close to one. The input resistance should be on the order of 10^{12} ohms, and therefore is not felt by the timing network. Input capacitance has negligible effect on the timing network, as given by the following equation:⁷

$$\begin{aligned} C_i &= C_{gd} + C_{gs}/(1 + g_{fs}R_L) & (8) \\ &= 2\text{pf} + 2\text{pf}/1+(3000\text{umhos})(10\text{K}) \approx 2\text{pf} \quad (\text{typically}) \end{aligned}$$

And the output resistance is given by:

$$\begin{aligned} R_o &= R_L/(1 + g_{fs}R_L) & (9) \\ &= 10\text{K}/1 + (3000\text{umhos})(10\text{K}) = 320 \text{ ohms} \quad (\text{typically}) \end{aligned}$$

Although the lowest possible output resistance is desirable for driving following amplifiers, it was found that a source resistance of at least 10K was necessary for best linearity of the output. Even though the calculated output resistance is quite low, a capacitively coupled load of less than 10K again effected linearity. Therefore if low impedance loads are anticipated, another stage, such as a bipolar emitter-follower, might be desired.

There are several reasons for the insistence on a single, 15 volt supply in this initial design, when actually the 555 is capable of operation from 5V to 15V. The lower cost of a single supply is obviously one advantage. Another factor is that the large, 10 volt ramp may simplify the design of following high slew-rate deflection amplifiers. Still

another advantage becomes evident when taking a look at the action of pin 3. The high-current output pulse from pin 3 goes positive and negative in essentially exact coincidence with the start and the end (10 volt break-point) of the sweep. It does so with rapid, 50 nsec rise and fall times, and an excursion of about 13 volts p-p. As such, it makes an ideal unblanking pulse for the oscilloscope. With a 15 volt supply, this will often be of enough voltage so that no further amplification is necessary.

It is just as important to recognize that there are some advantages to a split supply. With 10 volts supplied to the 555, the requirements for a low FET pinch off voltage is greatly reduced. With 5 volts supplied to the 555, we can cease worrying about V_p , and the inputs and outputs of the timer are directly TTL compatible as well.

Initial tests were conducted with 2N3819s, having somewhat poorer specifications than either of the other two types. No visible non-linearity was observed with R_s values from less than 800 ohms to over a megohm, with sweeps from several seconds to 200 nsecs. Using a pulse generator with a 50 ohm output, the 555 triggered nicely with negative-going pulses as narrow as 25 nsec, at rates as high as 20 mc. This basic ramp generator exceeded the best expectations.

Three facts keep this circuit from assuming the entire triggered sweep function. First, the trigger must be a short pulse. If pin 2 stayed low longer than the duration of the sweep, it would over-ride pin 6, allowing the capacitor to charge all the way to V_{cc} and stay there. Second, since pin 2 will not respond to slow waveforms without noise and extraneous triggering, we need to shape the waveform with a Schmitt trigger. Third, and probably the most demanding, is the fact that any input

trigger which occurs during the fall time of the discharging capacitor will cause premature release of the switch, and thereby raise pins 6 and 3 again, before they have time to fully reach the low state. The solution to these problems is the purpose of the trigger circuits described next.

THE TRIGGER

First efforts were directed towards trigger circuits operating at 15 volts, to retain the advantages of the high output and single supply. It was discovered that a truly low cost, high speed Schmitt trigger was more difficult to obtain than the ramp circuit itself. Discrete circuits having good performance from DC to at least 5mc were generally more complex and costly than desired. On the other hand, 15 volt integrated circuits generally had difficulty meeting frequency requirements. Four of the most promising 15 volt circuits are presented here. Conventional TTL triggers are available commercially and are well known, so in-depth analysis of such devices is considered unnecessary.

Figure 4 shows a Schmitt circuit suggested by Motorola⁴ for their 15 volt MHTL IC logic, using active pullup inverters such as the MC680 quad inverter or MC672 quad 2-input NAND gate. As can be seen, regenerative feedback through R_2 allows a relatively slow input waveform to cause a sharp switch from one stable state to the other. Turn-on and turn-off voltages, as well as hysteresis, are functions of R_1 and R_2 . For the values shown, the output goes high at a 7.2 volt input, and goes low at 6.5 volts. MHTL logic is usually capable of 3-4 MHz. On one test, this particular circuit failed quite abruptly around 2 MHz. However, triggering was very clean between .01 Hz and the 2 MHz limit, indicating that it could be an effective trigger for low frequency oscilloscopes.

Considerable effort was expended in an attempt to use the 555 as a Schmitt, since the 8-pin design would allow one 16-pin socket to be used

for both trigger and ramp generator, and there could be a slight cost advantage as well. Figure 5 shows a conventional approach, allowing triggering of the device by either positive or negative going waveforms, depending on the bias level set by the 20K potentiometer. (For this application a negative-going output is desired, necessitating a positive-going input waveform.) The positive feedback to pin 5 helps obtain a sharp switching action. The feedback capacitor must be less than that at which overshoot starts showing up at pin 5. Overshoot causes small "steps" in the exact trigger level, at low (threshold) levels of signal input. Clean output pulses were obtained with very slowly varying waveforms. However, the trigger points tended to shift with trigger amplitude and frequency, and results were inconsistent above 200KC in the case of negative-going input signals, or above 40KC for positive-going inputs.

While experimenting with the device, it was noticed that the device would trigger at $1/3 V_{cc}$, and again whenever pin 2 was driven below zero volts. This caused a doubling of the input frequency, (two output pulses for each input cycle), which of course was not wanted. However, further investigation showed that these trigger points were better behaved than the normal points, as far as the Schmitt trigger application was concerned. At low frequencies, the pin 3 output would switch cleanly from high to low state as a negative-going input waveform passed through approximately -0.3 volts. This trigger point has approximately 100 millivolts of hysteresis. Putting this feature to work resulted in the simple circuit shown in Figure 6. The minus .3 volt trigger level is ideal for a simple AC coupled trigger, but can be used with DC coupling if a level-shifting scheme is applied. The shunt diodes ensure that pin 2 is not over-driven.

Excess reverse bias of the input could cause internal damage, while excess drive in the positive direction will reach the "normal" trigger point, resulting in double-triggering. By biasing pin 5 high, this unwanted high trigger point is raised even higher. Then the desired trigger level can be adjusted over a range of about 15 to 1 by adjusting the DC bias over a range of 0.3 to 5.6 volts, as shown by the figure. It is important that pin 6 be connected to a clean source -- if the supply line is noisy, decoupling with small values of R and C is sufficient. The circuit triggers cleanly on slow waveforms, as long as the input is DC biased to about plus 0.3 volts or more. Tests indicate that a well-designed, low impedance driver could result in reliable triggering to 15-20 mc or more. The device responds to the higher frequencies by frequency dividing the input, but this is not a handicap in this application.

A tunnel-diode level detector⁵ can make a very effective high-speed trigger. However, this method was not investigated in depth, since the cost of a tunnel diode promised to exceed most of the other components put together.

TTL compatible circuits (using a 5 volt supply) allow use of common inexpensive logic elements. In addition, 5 volt TTL is inherently faster, with toggle rates exceeding 15 MHz. Circuits identical to the MHTL trigger can be constructed by merely substituting other active pull-up gates such as the 7404 or 7400, and lowering the values of resistance proportionately. Some of the low-to-high interface gates might be worthy of investigation as well, as they may allow 15 volt operation at higher frequencies than the MHTL.

At TTL levels, a little extra money can buy ready-made Schmitt devices such as the 7413 dual NAND Schmitt trigger or the 74121 mono-

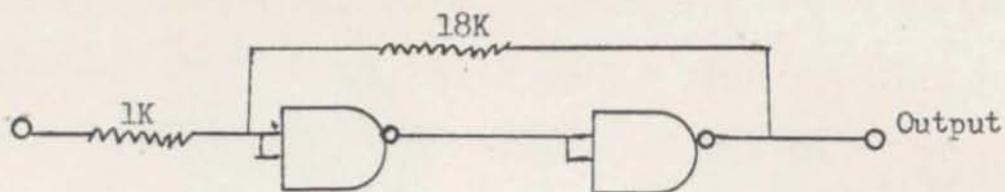


Figure 4. MHTL NAND Gates in a Schmitt Trigger Configuration

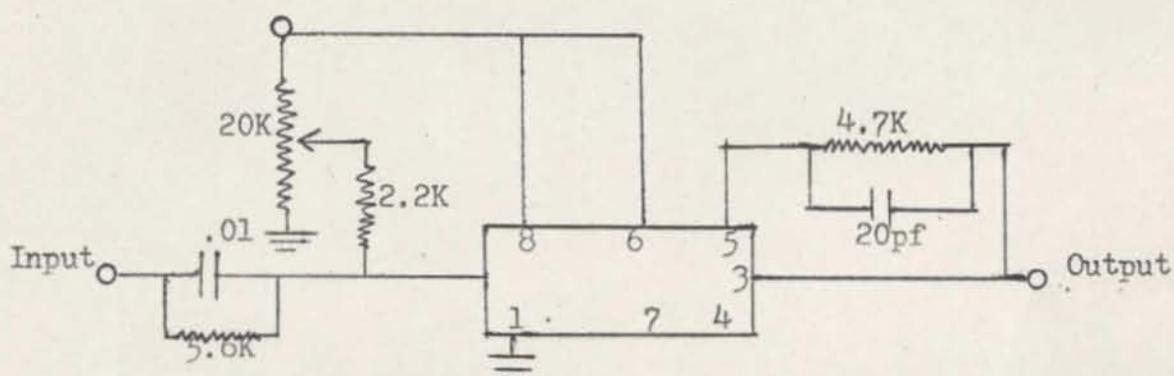


Figure 5. Using the 555 Timer as a Trigger

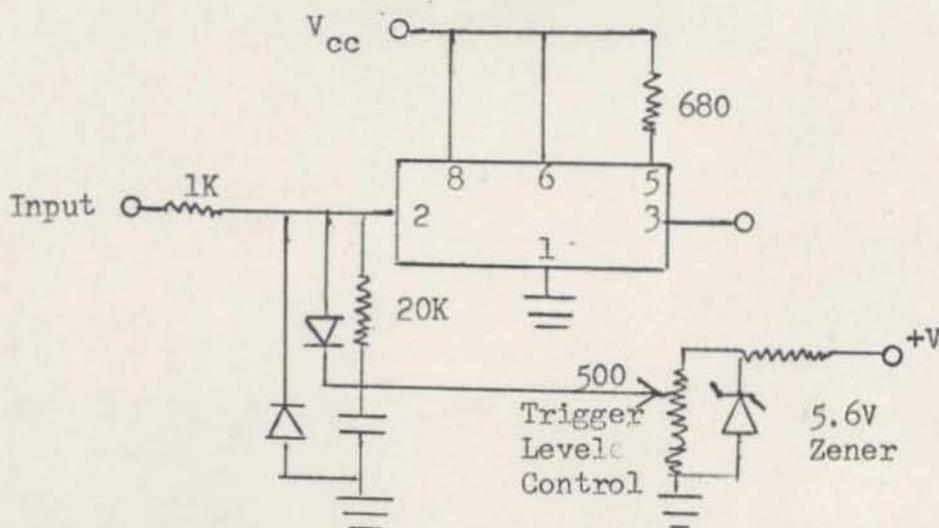


Figure 6. The 555 Timer as a High-Speed Trigger with DC Trigger Level Control

stable multivibrator. The 7413 is specifically designed to give clean, stable output signals from the very slowest of input ramps, yet it retains essentially the same maximum speeds as the rest of the TTL series.

TRIGGER PULSE-FORMING AND GATING

The 555 ramp generator must be driven by a very narrow negative-going pulse, and this pulse must be gated in a way which will prevent any possibility of triggering during discharge of the timing capacitor i.e., the "fly-back" time of the oscilloscope sweep. Except in the case of a monostable trigger, the narrow pulse is most easily obtained by a simple RC differentiator. The gating can be done by using any of three methods -- changing the state of bistable multivibrator, use of logic gates, or diode gating.

The 555 data sheet indicates that it will trigger reliably with a pulse of 75 nsec as long as the pulse reaches well through the one third V_{cc} threshold ($0.2 V_{cc}$ or below). The maximum amplitude of the pulse is reached when an RC differentiator time constant is large with respect to the rise time (T_r) of the input signal. On the other hand, a small RC time constant with respect to rise time is desired for a narrow pulse. Therefore, what is needed is the smallest possible RC to T_r ratio which still provides 80-90% of the input amplitude. This amplitude requirement is safely met when $RC \approx 3T_r$. Anything larger will tend to broaden the pulse so that it does not have time to reach full amplitude for very high input frequencies. At 15 volt levels, typical rise times of 40 nsec imply an RC time constant of 120 nsec. A fairly low value of R is desired, so that frequency effects of the following stage is partially shunted. The trigger input resistance of the 555 is approximately 7000 ohms and effectively parallels the external R. With this in mind, a resistance of 3900

ohms and a capacitance of 47 pf meets requirements very well. The pulse width at the 50% amplitude points will be approximately $2 T_r$, or 80 nsec.

For the faster rise-time of TTL logic, the amplitude requirements could be reached with smaller values of RC. However, the output pulse width would decrease accordingly, possibly to less than the 75 nsec requirement. Therefore, the 3900 ohm, 47 pf combination appears to be a good choice for driving the 555, regardless of the type of logic used for the Schmitt trigger.⁶

A bistable gating circuit can be built easily using two NAND gates. As shown in Figure 7, R_3 helps ensure that output Q is initially high. As the input receives a negative-going signal from the Schmitt trigger, the flip-flop changes state, forcing Q low. The input can then no longer respond to commands until a negative-going waveform at the upper terminal resets the flip-flop. The circuit applies itself to 15 volt as well as 5 volt logic. R_1 and R_2 are probably not absolutely necessary, but they shunt the non-linear input impedance of the gates and thereby make the operation of the differentiator network more predictable. TTL has roughly 2-5 kilohms input impedance and MHTL roughly 7-15 kilohms input impedance. For TTL, the 47 pf and 3900 ohms found earlier, should suffice. Since MHTL requires an input pulse of about 120 nsec for safe triggering, its somewhat higher input impedance again tends to make the combination a satisfactory choice.

The bistable circuit is a conventional, safe approach to ensuring no false triggering. However, if the circuit gets into the wrong initial state, the circuit may never respond to the input. For these reasons, special "arming" circuits are often included.

Routine NAND gating avoids such problems. The one NAND gate shown

in Figure 8 simply blocks incoming trigger pulses until a command allows the pulse to pass. In this case, the input resistor must not only be the proper value for differentiation, but also be low enough to ensure that the gate sees the input as being normally low. MHTL has a threshold of 7.5 volts and an internal bias resistance of 15K, so any R less than 6 kilohms would be suitable. TTL has a threshold of only .8 volt, with a maximum bias current at that level of 1.6 ma. This indicates that a resistance of less than 500 would be necessary to ensure a logic 1 output. This is still well within the load capabilities of TTL. An RC differentiator of 390 ohms and 470 pf appears to be a logical choice in the case of TTL.

The simplest circuit of all uses one diode and one resistor. As long as the gate input signal is high, the diode is forward biased and the driver is unable to pull the output low. When the gate input is low, the diode is cut off and an input pulse is allowed to pass without attenuation. R_2 must be high enough so that the gate and trigger drivers are decoupled and the diode gate can sufficiently clamp the pulse. At the same time, R_1 must be small enough so that it does not contribute a detrimental pole in the frequency response. Assuming a 7.5 pf load, an R_1 of 220 ohms places the pole at approximately 100 MHz.

The trigger and gating sub-circuits so far described, suggest combinations leading to many different versions of the complete sweep system. In the next section some of these circuits will be inter-connected to form complete and tested triggered sweep systems.

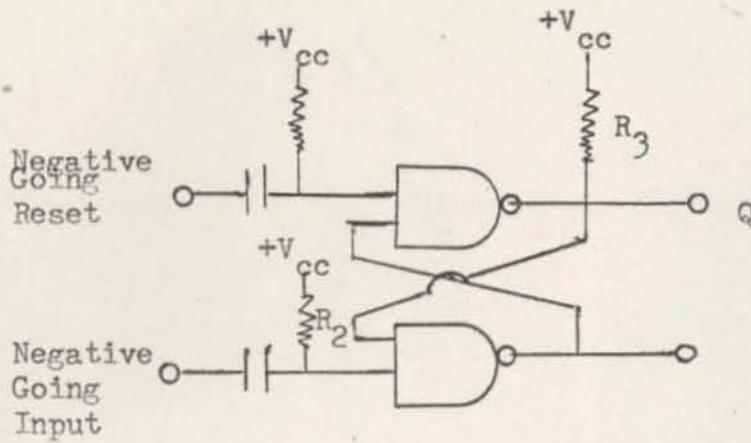


Figure 7. Bistable Multivibrator used for Gating of Trigger Pulse

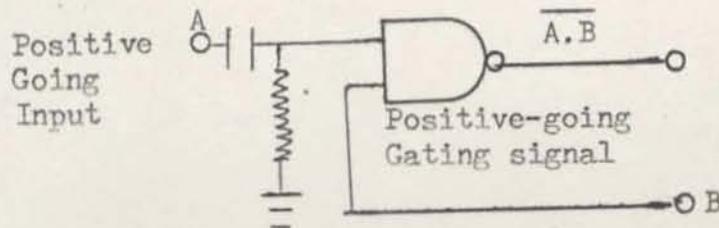


Figure 8. Conventional Logic Gating of Trigger Pulse

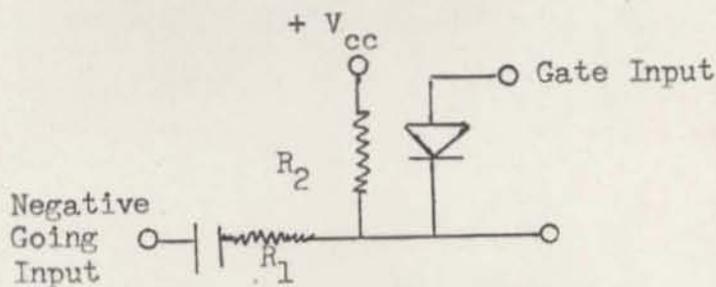


Figure 9. Simple Diode Clamping of Trigger Pulse

COMPLETE TRIGGERED SWEEP SYSTEMS

The main body of this report lays the foundation for many versions of inexpensive but respectably performing triggered sweep generators. This section describes three of the most interesting variations.

The first circuit uses a conventional Schmitt trigger, bistable multivibrator approach to process the input waveform (Figure 10). The diode-protected input FET provides a high input impedance for internal or external oscilloscope triggering signals. Because of the extremely high input impedance of this FET source-follower, the 10K series resistor has almost no effect on the signal. The differential amplifier provides a gain of 15-20, and allows trigger slope selection and level settings. The next two stages, a Schmitt trigger and a flip-flop, are constructed from 2-input NAND gates, as described earlier. A 7413 Schmitt trigger could be substituted for the NAND gates Schmitt, but the arrangement shown works extremely well and requires only one very inexpensive IC package. With proper pulse differentiation and level shifting to pin 2 of the 555 timer, the 555 generates a linear ramp and blanking pulse, then resets the flip-flop when the sweep is completed. A dual supply is needed, but allows the use of high speed logic while retaining high level sweep and blanking pulse outputs.

The voltage divider level shifting scheme at pin 2 of the 555 deserves a little attention. The trigger point is nominally $1/3 V_{cc}$, but can vary by as much as 30%. This means that the lowest bias that can be applied is slightly over $1/3 V_{cc}$, $-(.30) 1/3 V_{cc}$ or about $.5 V_{cc}$. On the

other hand, the input pulse must be great enough to ensure reliable triggering for the opposite extreme of trigger point, which occurs at $1/3 V_{cc} - (.3) 1/3 V_{cc}$, or just over $.2 V_{cc}$. This means that the pulse magnitude must be at least $(.5 - .2) V_{cc}$, or in this case, 4.5 volts. Most TTL guarantees only 2 volts. Therefore, it is wisest to include a bias adjustment potentiometer as shown. This circuit has not been tested in its entirety, but tests of individual subsections promise performance from DC to about 20 MHz.

By powering the 555 from the 5 volt supply, the 555 becomes TTL compatible and the bias adjustment potentiometer is not needed. At the same time, the requirement for low FET pinch-off voltage is eliminated. The only disadvantage is that the sweep and blanking outputs may require additional amplification.

The second circuit uses only a single-level supply. In this less expensive variation, trigger level control is omitted, and trigger slope is switch selected from the phase splitter. The zener diode provides level shifting. Since the zener is forward biased at all times, it does not limit the speed of response. A single MHTL package comprises the trigger and gating circuitry. The first two gates form the Schmitt trigger. The third gate inverts the pulse output of the 555 ramp generator and directs this to the fourth gate, which in turn controls the passage of the differentiated trigger pulse. Some oscilloscopes require a positive rather than a negative blanking pulse. Besides allowing use of a single high-level supply, this circuit has the advantage of providing blanking signals of both polarities (from pin 3 and the output of the inverter). These advantages are gained at the cost of frequency capability, since the MHTL will respond only to input waveforms up to about 2-4 MHz. Substituting 5 volt TTL gates gives response to 20 MHz.

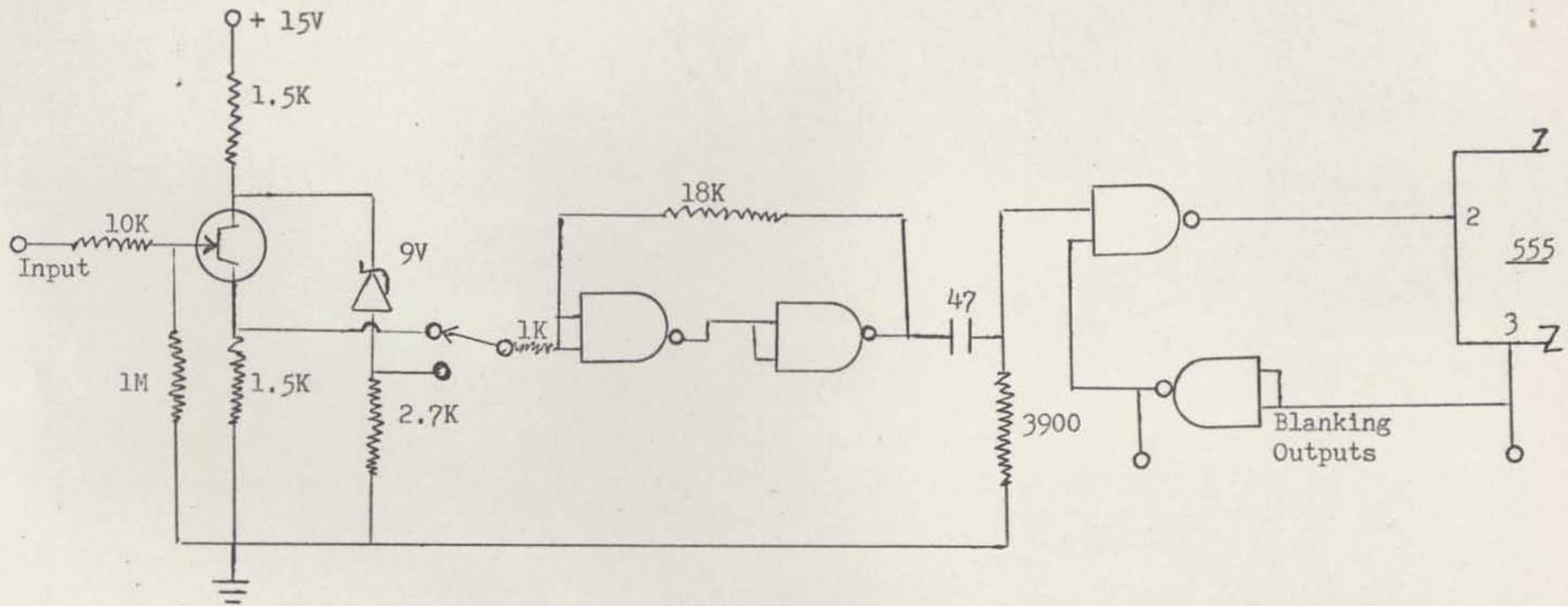


Figure 11. Simple, Low Cost Sweep System using High-Level MHTL MC672 Quad 2-Input NAND Gate Trigger

The third circuit uses the 555 for both the trigger and the ramp generator. The diode-protected MOS-FET input forms a novel phase splitter arrangement which provides both trigger level and trigger phase selection with one control. When the control is centered, the two oppositely phased signals cancel. Sensitivity then increases as the potentiometer is adjusted toward either the positively or negatively phased ends. The potentiometer can create as much as 2500 ohms of series resistance, which contributes to a response pole located above 70 MHz. This pole has relatively small effect of the 10 to 20 MHz range of the trigger, even for short pulses. The two silicon diodes on pin 2 set the bias level as well as limit the positive and negative waveform excursions.

Diode clamping protects the ramp generator from false triggering during the fall-time of the capacitor. While the capacitor is charging, the blanking pulse from pin 3 is high. With the 220 ohm series resistance, the low output impedance of the blanking pulse has no trouble in forward biasing the diode and limiting any negative-going pulse on pin 2. However, the driver also has low impedance, and is still able to force through a small pulse which will appear on the blanking pulse as well as pin 2. As long as this pulse does not exceed the trigger threshold or exceed the blanking requirements of the particular oscilloscope, it creates no problem. This single circuit allows use of a simple high-level supply, uses only one 16 pin IC socket, and triggers well from approximately 10 HZ to over 15 MHz.

A comparison of results is provided in Table 1. Also included are the characteristics of two typical triggered sweep systems described in past magazine articles^{8,9} It can be seen that these circuits compete extraordinarily well.

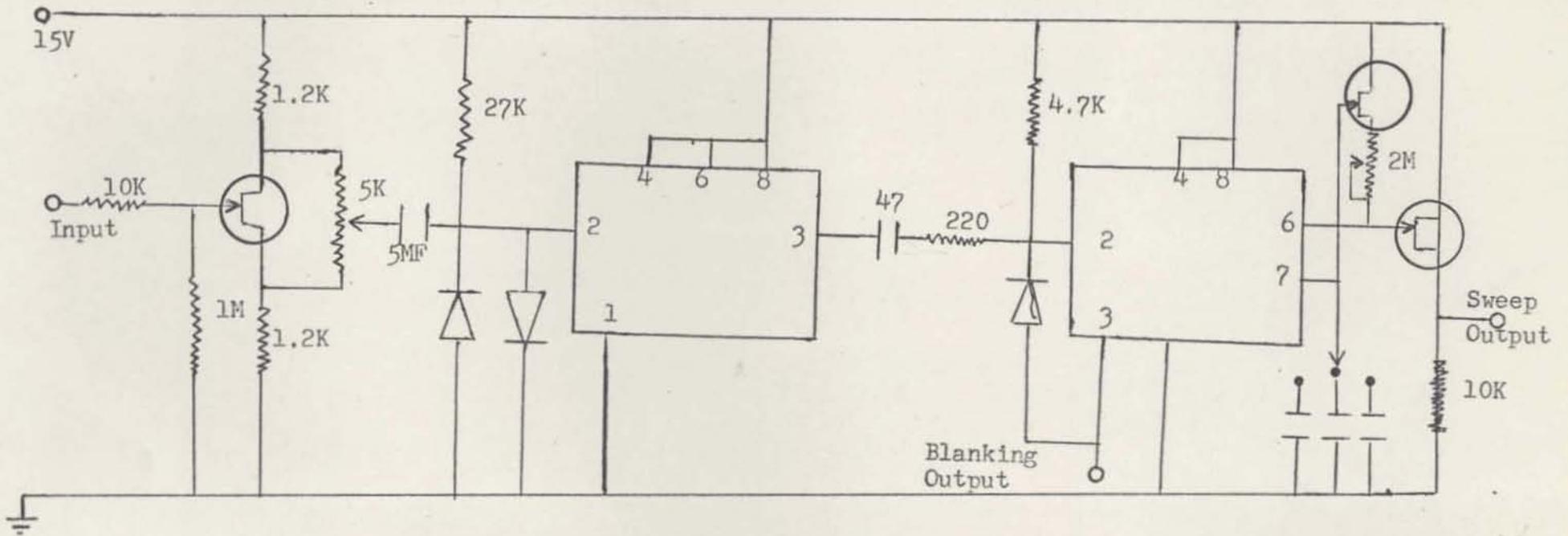


Figure 12. Complete Triggered Sweep System using only 555 Integrated Circuits and FETs

CIRCUIT	SWEEP RANGE	SWEEP AMPLITUDE	TRIGGER RANGE	POWER COUNT	POWER REQUIRED	UNIT COST w/o BOARD	BOARD COST
TTL	100SEC to 200 NSEC	10V	DC - 15 MHz	28	5V-15MA 15-15MA	10.50	4.50
MHTL	SAME	SAME*	DC - 3MHz*	17	15-30MA	6.00	4.00
555	SAME	SAME	DC-15 MHz	20	15V-25MA	8.00	4.25
MAGAZINE ARTICLE ₁	10Hz - 100KHz	8V	10Hz - 1MHz	57	3.6V-20MA	35.00	5.00
MAGAZINE ARTICLE ₂	10Hz - 100KHz	7V	1HZ - 1MHz	33	+ 9V-20MA - 9V-20MA	15.00	4.00

* or 3 volts and 20MHz using TTL

** Approximate cost of single commercially etched and drilled board

A Comparison of Triggered Sweep Systems

SUMMARY

In the past, triggered sweep systems have traditionally been constructed from discrete components, leading to relatively complex and costly circuits. More recent designs have attempted to use logic for trigger circuits and integrating operational amplifiers for ramp generation. However, many of the triggers have been noisy at very low frequencies or unresponsive at high frequencies. Operational amplifiers are capable of very linear ramps, but slew-rate limitations severely limit high frequency performance, and it is sometimes difficult to trigger the amplifier without introducing noise. The result has been that low priced oscilloscopes invariably omit this valuable feature - even though triggered sweep capability is, for all practical purposes, an outright necessity.

By using the latest integrated circuits, it is possible to construct triggered sweep systems that compete extraordinarily well with systems found in professional oscilloscopes. At the same time, the greatly reduced parts count leads to very low hardware and construction costs.

The author uses a modern IC, the 555 Timer, in a simple but original ramp generator scheme which allows highly linear ramps ranging in period from more than 100 seconds down to less than 200 nsec. At the same time, the circuit provides a perfect blanking pulse output, and fast, noise-free return traces. Not counting range-changing capacitors and PC board, the 6 individual components in the basic ramp generator cost less than 4 dollars in single quantities.

Several good triggering and gating circuits are described. By using various combinations, many different complete systems can be constructed. Inexpensive and reliable trigger and gating circuits can be constructed by using readily available MHTL (high level 15 volt logic) or TTL (5 volt logic). Depending upon the exact choice of components, system trigger capabilities of DC through 2 or 15 MHz can be obtained.

Three complete systems are described in the last section, each chosen to illustrate some of the unique features of the circuits described earlier. Cost/performance trade-offs are relatively small, allowing a circuit with all of the most desired features to be built at a cost of less than 15 dollars. The somewhat optimistic goal of this paper was to develop a circuit costing less than about 15 dollars, yet providing a 1 usec sweep period and capable of triggering to about 5 MHz. As it turned out, one of the circuits described can generate 200 nsec ramps, at trigger frequencies of 2-3 MHz (for high level MHTL design) or over 15 MHz (for low-level TTL design), and do so at a cost of about 10 dollars. This is about half the cost and several times the performance of other popular circuits described in the past.

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