SOLAR-BASED SINGLE-STAGE HIGH-EFFICIENCY GRID-CONNECTED INVERTER

by

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ABSTRACT

Renewable energy source plays an important role in the energy cogeneration and distribution. Traditional solar-based inverter system is two stages in cascaded, which has a simpler controller but low efficiency. A new solar-based single-stage grid-connected inverter system can achieve higher efficiency by reducing the power semiconductor switching loss and output stable and synchronized sinusoid current into the utility grid. Controlled by the digital signal processor, the inverter can also draw maximum power from the solar array, thereby maximizing the utilization of the solar array.

In Chapter 1, a comparison between the traditional two-stage inverter and the single-stage inverter is made. To increase the ability of power processing and enhance the efficiency further, a full-bridge topology is chosen, which applies the phase-shift technique to achieve zero-voltage transition. In Chapter 2, average-mode and switch-mode Pspice simulations are applied. All the features of the inverter system are verified, such as stability, zero voltage transition and feed-forward compensation, etc. All these simulation results provide useful design tips for prototyping. In Chapter 3, a phase-shift controller is designed based on UCC3895. Also, a detailed design procedure is given, including key components selection, transformer and inductor design and driver circuits design. In Chapter 4, experimental results of a prototype DC/DC converter are presented and analyzed. By optimization of the circuit, the problems of the prototype are solved and the prototype is working stably. The thesis' conclusion is given in Chapter 5.

Dedicated to my parents and my wife.

ACKNOWLEDGMENTS

I would like to thank my advisor, Dr. Issa Batarseh, for his constant encouragement and thought provoking ideas that have helped me in this thesis work. I would also like to thank Dr. Kasemsan Siri for his creative ideas on the topology of the inverter.

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CHAPTER ONE:INTRODUCTION

The production and distribution of energy affects all sectors of the global economy. The increasing industrialization of the world requires sustainable, highly efficient energy production. Without a major technological advance, projected energy production will dramatically affect the quality and sustainability of life on Earth. With advancements in the field of renewable energy sources and the expected increase in global power demand over the coming years, the need for developing a highly efficient power electronic interface has never been greater.

Alternate energy systems, which are in high demand to minimize our dependence on foreign oil imports, reduce significant capital investments for newer centralized power generating units and lower environmental pollution. Additionally and yet equally importantly, such distributed generation potentially reduces the risk of complete blackout in the event of cascaded power system failures, as experienced in the United States recently on the Northeast grid.

In all kinds of renewable energy sources, such as wind, sun and fuel cells etc., solar energy is one of the best energy sources to utilize, which mainly converts energy from the sunlight to electrical energy through photovoltaic effect. Solar energy is green and inexhaustible energy, without any pollution to the earth and atmosphere.

The major benefit of designing a reliable, stable, efficient and lower cost photovoltaic power electronics system is the availability of reliable and quality power without relying on the utility grid. It also avoids the major investment in transmission and distribution. For the nation, the major benefit lies in the fact that it reduces greenhouse gas emissions, responding to the increasing energy demands by establishing a new, high-profiled industry.

Grid-connected solar power was developed more than ten years ago as an alternative energy source to the utility grid, especially in remote areas and developing countries where the utility is not stable. Due to these reasons, the grid-connected solar power market has annual growth of 10 percent worldwide, which equaled $276 million in 2003 and will be $445 million in 2008 [1]. Figure 1.1 shows the mega-watts of grid-connected solar power since 1993, which provided the fast growth of solar power in worldwide distributed and cogeneration of electrical power.

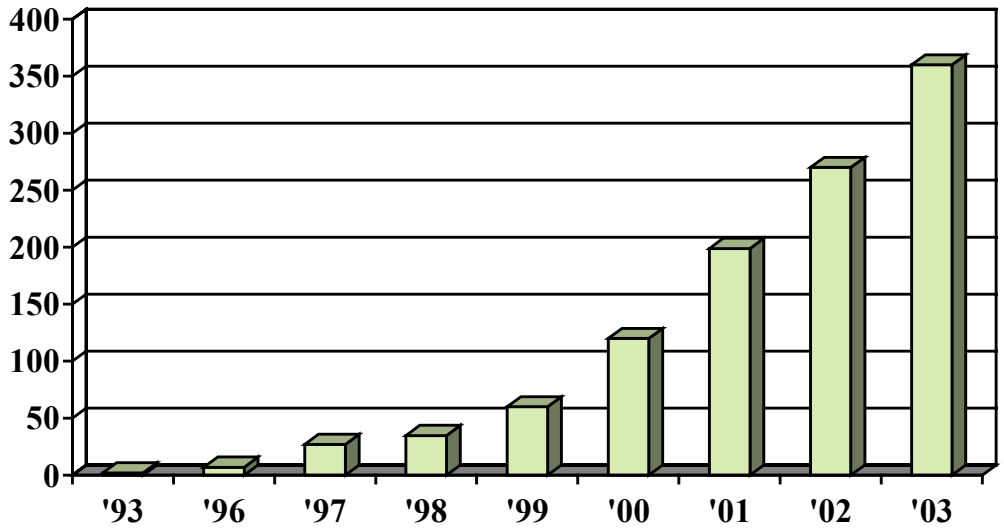


Figure 1.1: Cumulative Installed Capacity in Mega-Watts of Grid-Connected Solar Power [1]

1.1 Solar-Based Inverter System

Figure 1.2 shows the basic I-V curve of PV array, which is a nonlinear source. In general, the current of PV array will drop slowly when the voltage of PV array is smaller than V_{mp}, but

the current will drop quickly when the voltage of solar array is greater than V_{mp}. At the same time, the power of PV array will reach its maximum power point (MPP) when the voltage of solar array reaches V_{mp}.

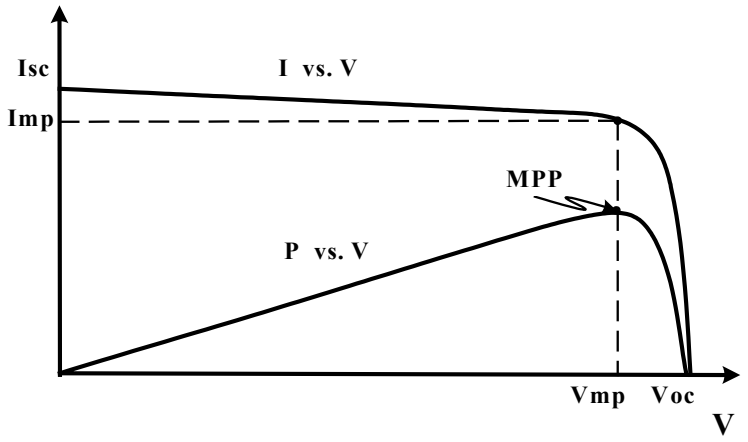
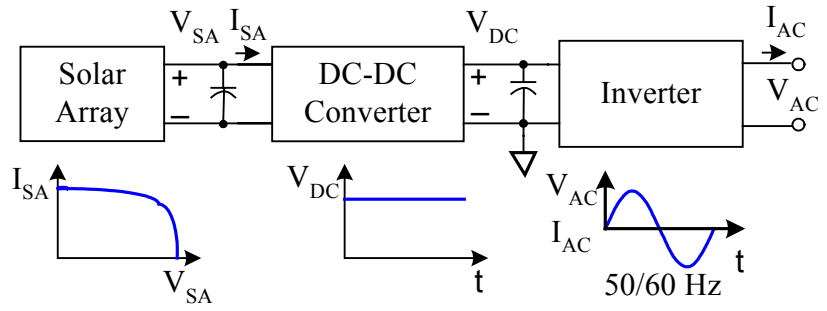


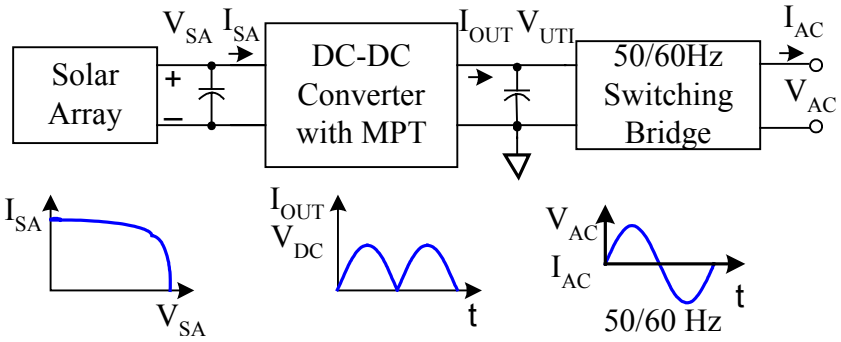
Figure 1.2: I-V and P-V Solar Array Characteristics [2, 3]

The I-V curve of PV array also will change with the ambient temperature and solar radiation. Then the point of V_{mp} is not constant. To regulate the solar array at its MPP, a DC/DC converter with MPP controller is usually applied, which will regulate the solar array at its MPP no matter what temperature or solar radiation. The MPT algorithm and MPT controller are described in [2, 3].

The traditional grid-connected inverter system is a two-stage cascaded system, which uses DC/DC converter as the first stage to regulate the solar power at its MPP. The second stage utilizes a conventional PWM inverter, which will convert the constant DC into sinusoid AC and synchronize with the utility grid, as shown in Figure 1.3(a).



(a) Conventional Inverter



(b) New Inverter Structure

Figure 1.3: Solar-Based Conventional Inverter and New Inverter Structure

A new grid-connected inverter system simplifies the conventional two cascaded stage structure into a single stage structure, as shown in Figure 1.3(b). In this inverter system, the DC/DC converts not only the regulated PV array at its MPP, but also output rectified sinusoid wave shape current. Then, a simple 50/60Hz switching bridge easily can invert this rectified sinusoid current into sinusoid current, which is also synchronized with the utility-grid [3].

The conventional inverter system has a straightforward structure, which is fully developed and studied. Matured commercial products even can be found. Also, it has simpler controller design. The shortcoming of this structure is that the efficiency of the whole system is the product of these two stages. In general, the efficiency of high-frequency switching power

converter and inverter is about 90 percent – 94 percent. Therefore, efficiency of the whole system is only about 81 percent – 88 percent [3].

For the single-stage inverter system, the overall efficiency can be up to 94 percent, due to the single stage design and without high frequency switching at the 50/60Hz switching bridge.

Three key factors will decide the application of grid-connected solar power system, which are price, efficiency and reliability. With less switching transition and higher efficiency, the single-stage inverter system can achieve a lower price and more reliability than a conventional one.

1.2 System Structure of Single Stage Grid-Connected Inverter

A single-stage solar inverter system block diagram is shown in Figure 1.4. It tracks the array maximum power and outputs of an in-phase AC current supplying the utility grid [3]. The inverter system consists of a solar-array source, bulk array filter capacitor C_{BULK}, line-filter, DC/DC converter, 50/60Hz switching bridge, output filter and a system controller. The system controller can be decomposed into six basic control sub-systems: (1) maximum power tracking (MPT), (2) solar-array voltage regulation, (3) converter output average-current regulation, (4) DC/AC switching bridge inverter, (5) compensated current reference generator and (6) utility over-voltage protection.

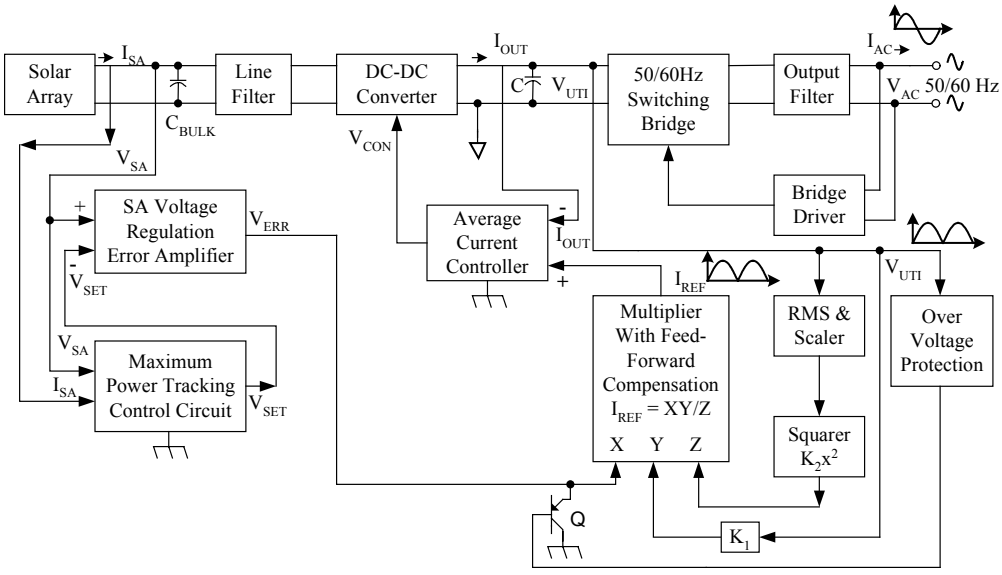


Figure 1.4: Single Stage Maximum Power Tracking Solar Inverter

Employing solar-array voltage V_{SA} and solar-array current I_{SA} as the feedback signals, the MPT control sub-system continuously updates the set-point voltage reference V_{SET}. The set-point voltage reference commands the solar-array voltage regulation sub-system (or SA voltage regulation error amplifier) to produce the error voltage drive signal V_{ERR} for regulation of the solar-array voltage, V_{SA}, at the level corresponding to V_{SET}. Upon reaching a steady state of operation, V_{SA} is controlled to swing back and forth around the peak-power array voltage with acceptable AC ripple voltage of the frequency at twice as much the utility frequency. V_{ERR} signal, which is sufficiently band-limited to have negligible AC ripple voltage, especially at twice the utility frequency despite the presence of an AC array-voltage ripple, commands the converter output average-current regulation sub-system that controls the converter power stage to deliver properly the output current of the rectified sinusoidal wave shape, I_{OUT}. Subsequently, the DC/AC switching bridge inverter sub-system provides switching control at the utility frequency

to the 50/60Hz switching bridge that converts I_{OUT} into an AC current in synchronization with the AC utility voltage and delivers to the utility grid the in-phase AC current I_{AC} with low total-harmonics distortion [4]. When an over-voltage is detected from the rectified utility voltage V_{UTI}, the over-voltage protection sub-system further reduces the error voltage drive signal V_{ERR} through an active pull-down transistor Q. Under this condition, either the absolute average of V_{UTI} is regulated at a predetermined level or the power converter is shut down while the absolute average of V_{UTI} already exceeds the predetermined level [5-7].

The average-current regulation sub-system is part of the innermost control loop that requires the fastest control dynamics (or the highest control unity-gain bandwidth) as compared to those of the array-voltage regulation sub-system since the system requires low harmonics distortion of the rectified sinusoidal current output [8,9]. Serving as the commanding reference-current signal for the average current regulation sub-system, I_{REF} possesses the rectified sinusoidal waveform that is properly scaled from the rectified utility voltage V_{UTI}. To significantly reduce the variation of the error voltage V_{ERR} at an array power level within a utility voltage range, a feed-forward compensation technique is utilized to continuously update I_{REF} through the feed-forward compensated multiplier from which the output reference current signal I_{REF} is the scaled product of three quantities: V_{ERR}, the instantaneous value of V_{UTI}, and the inverse of the RMS squared value of V_{UTI}. Ensuring low total-harmonic distortion in the in-phase AC current $I_{AC,}$ V_{ERR} must have negligibly small AC ripple content superimposed on its DC operating point. Therefore, the control loop gain frequency response of the solar-array regulation needs to have a relatively low unity-gain bandwidth (such as a 10Hz to 15Hz bandwidth). Consequently, the array-voltage regulation control loop is designed to be insensitive to the fundamental frequency of the array-voltage AC ripple (at 100/120Hz) but only to the DC or

much lower frequency components of the solar array voltage [10, 11]. Since the solar array source does not have the stiff characteristics of a voltage source, the system requires a proper value of the input filter capacitance C_{BULK} to limit the array voltage ripple (at 100/120Hz) to an acceptable amplitude (of 5 percent or less) relative to the array operating voltage [3,12,13].

The compensated current reference generator consists of a root-mean-square (RMS) extraction and scaling circuit, signal squarer, and a three-input multiplier. The RMS and scaling circuit extracts a low-pass filtered signal that has its DC component being proportional to the RMS value of the utility line voltage. The scaled RMS signal must have negligible AC components to ensure low harmonic contents of the controlled sinusoidal current supplying to the utility grid. The scaled RMS signal is squared and subsequently inversed after being fed to the Z input of the three-input multiplier circuit. The inversed, squared RMS signal is used as a feed-forward compensation factor, 1/Z, for the three-input multiplier that senses, at the input Y, the rectified utility voltage signal of the rectified sinusoidal wave shape and multiplies V_{ERR} signal as input X by the product of the sensed rectified line-voltage signal (Y) and the feed-forward compensation factor (1/Z). The multiplier outputs the computed result (X*Y/Z) as the reference current signal, I_{REF}, which commands the innermost control loop to regulate the converter output current accordingly [3,14].

The line-filter interfacing to the array source provides sufficient differential-mode attenuation of line voltage and current ripple at medium and high frequencies as well as common-mode attenuation of the conducted-emission at high frequencies [12], as does the output-filter that interfaces to the utility grid. The 50/60Hz switching bridge is driven by a set of switching signals derived from the utility voltage through the bridge driver circuit such that the

resulting AC current I_{AC} that is converted from the converter output current I_{OUT} is always in-phase with the utility voltage.

1.3 Full-Bridge Phase-Shift DC/DC Converter

There are many topologies for a DC/DC converter, such as buck, boost, half-bridge, full-bridge and forward. For a single-stage solar-based inverter system, three requirements need to be fulfilled, which are high-efficiency, high power rating (above 1kW) and isolation. After comparing all these topologies, full-bridge is the best topology for this application.

Full-bridge can handle higher power (1kW or even more) easier than other topologies and supply isolation between the solar array and utility grid, which can protect the customers' safety, as shown in Figure 1.5. The main transformer of full-bridge works under full symmetry of volt-seconds, which will eliminate the saturation of the transformer and reduce the size of the transformer greatly. Another benefit of full-bridge topology is that it can easily achieve zero voltage switching (ZVS) controlled by a phase-shift controller, such as UCC3895, UC3875 and HIP4080, which can increase efficiency and reliability.

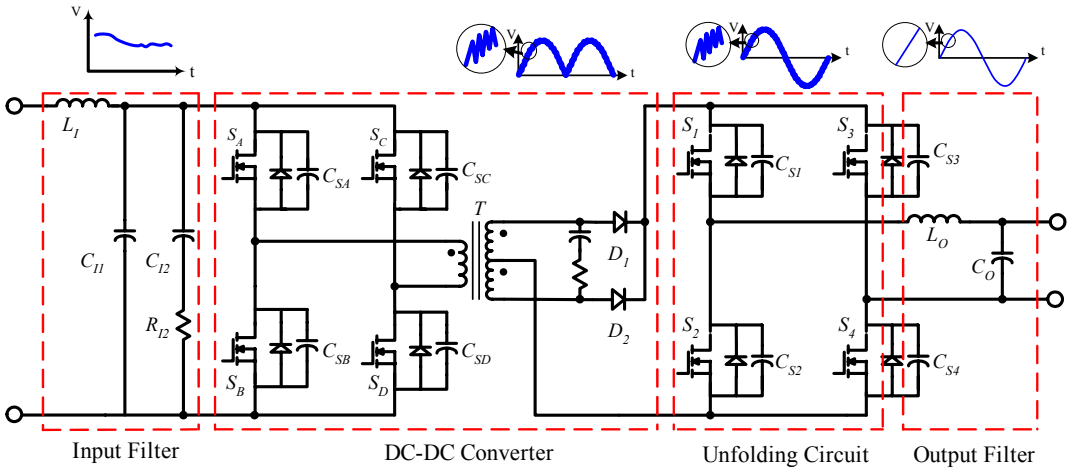


Figure 1.5: Full-Bridge Phase-Shift DC/DC Converter and Full-Bridge Unfolding Circuit

To invert the rectified sinusoid current into sinusoid current, a full-bridge unfolding circuit is applied, which will be switched in 50/60Hz frequency. Without high-frequency switching, the unfolding circuit has much higher efficiency than a high-frequency PWM conventional inverter.

CHAPTER TWO: SYSTEM SIMULATION

To prove the single stage inverter, both average mode and switching mode simulations are applied. Average mode simulation tries to prove the MPT algorithm and find proper bandwidth of an inner-loop and an outer-loop DC/DC converter, by transient and AC analysis. Switching mode simulation is more pragmatic than the average mode, but the simulation speed is much slower. Switching mode simulation can verify the performance of the full-bridge phase-shift DC/DC converter or unfolding circuit and supply useful design tips for the prototyping.

2.1 Average Mode Simulation

2.1.1 MPT of Mode I and II

Figure 2.1 shows the schematics of an average mode of grid connected single-stage solar-based inverter system.

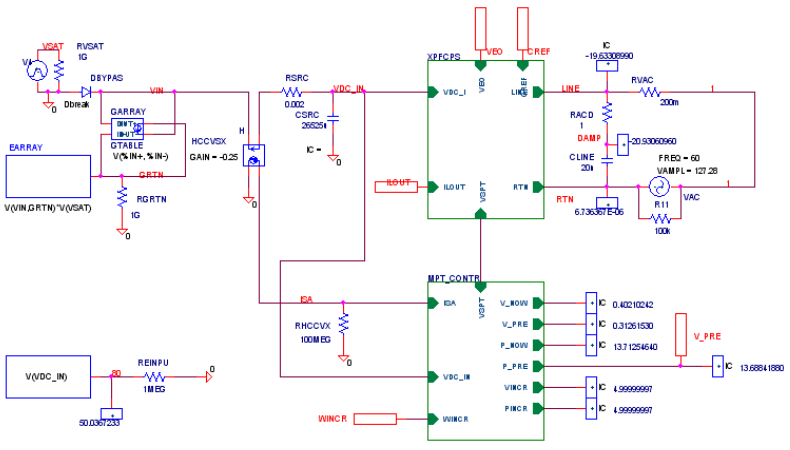


Figure 2.1: Schematics of a DC Analysis Average Mode Single Stage Solar-Based Inverter

Under different weather conditions and solar radiations, the solar array will have different characteristic I-V curves and different maximum power points. To demonstrate the adaptability of the inverter under the control of an MPT controller, two modes of characteristic I-V curves are chosen in simulation, which are shown in Figure 2.2. In simulation, these two modes will be switched linearly, and the transition time of these two modes is set to be 0.1s. As shown in Figure 2.2, the solar array will jump between these two modes as time goes by. The maximum power for mode I and II are set at 600 watts and 480 watts [3].

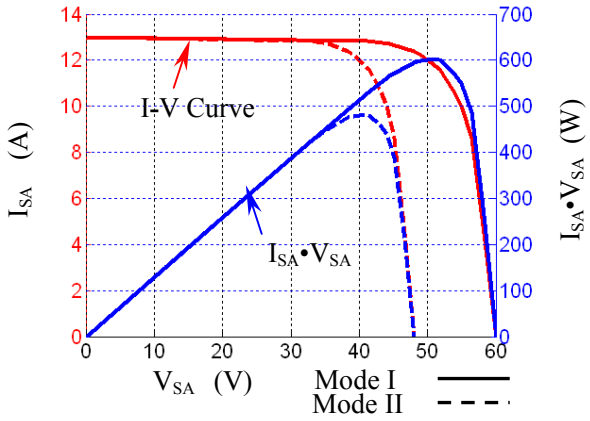


Figure 2.2: I-V Characteristic Curves for Solar Array at Mode I and II

As shown in Figure 2.3, the power of solar array will switch between 600 watts and 480 watts, during solar array mode switching. That means the power of solar array will track the maximum power under the specific mode of the solar array at that time. The simulation results can prove the stability of this system under step change of solar array maximum power point and the dynamic character of MPT controller.

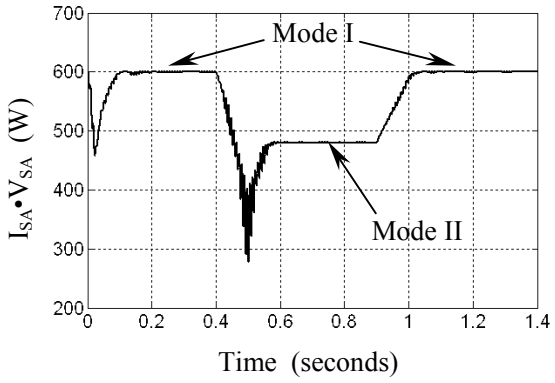


Figure 2.3: Solar Array Output Power of Mode I and II

2.1.2 Utility Grid Interface

Figure 2.4 shows that the voltage and current of utility grid have 180˚ phase shift, which means the energy will be charged into the utility grid from solar array. In addition, the current is nearly pure sinusoid with fewer harmonics. Therefore, the utility grid is not "polluted" by the inverter.

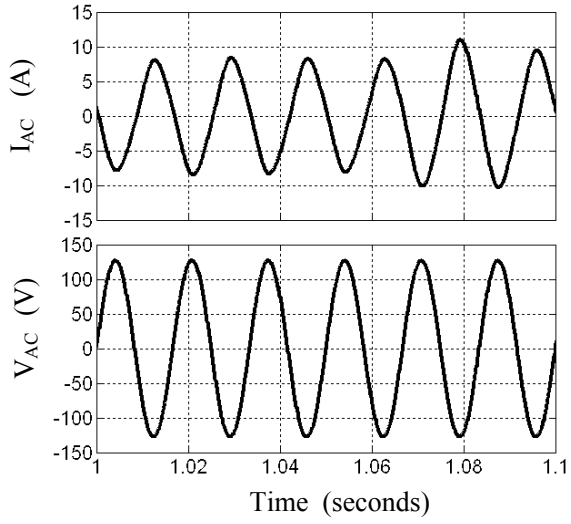


Figure 2.4: Utility Grid Current and Voltage

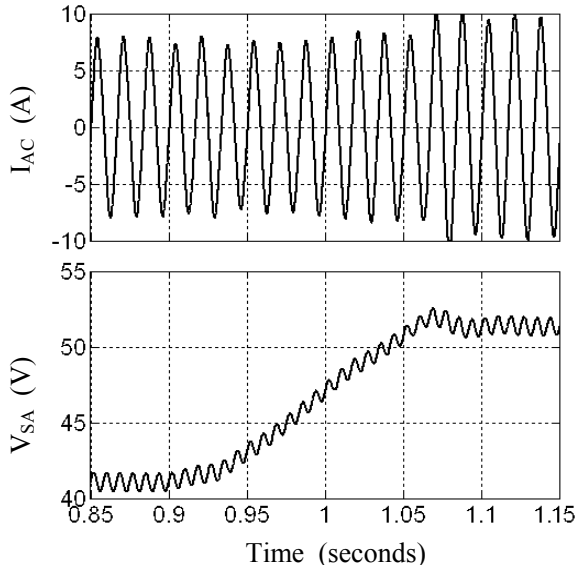


Figure 2.5: Utility Grid Current and Solar Array Voltage

As shown in Figure 2.5, the amplitude of solar array voltage ripple is very small even when the current injected into the utility grid is low-frequency sinusoid. After maximum power point achieved, there is still 120/100Hz ripple on the solar array voltage. The frequency of solar array voltage ripple is double that of the utility AC power frequency. In addition, the amplitude of the ripple is decided by C_{BULK} (Figure 1.4) between the solar array and DC/DC converter. The 100/120-Hz voltage ripple will worsen the performance of the average current controller, and will increase the third harmonics on the utility grid current [15]. To properly stabilize the solar array voltage regulation performance, the line filter interfaced between the array source and the DC/DC converter needs to be properly damped by two R-C damping networks, respectively, terminated across the filter input and output ports. Multiple local maximum peak power points may exist due to solar array shading and inadvertently cause the MPT controller to track at a locally lower maximum power point. This local-maximum power point problem is overcome by

superimposing additional dither signal [16] on the set-point voltage reference V_{set} prior to feeding to the SA voltage regulation error amplifier.

2.1.3 DC/DC Converter

To simplify the inverter design, the output current, I_{OUT}, and voltage, V_{UTI}, of the DC/DC converter should be synchronized rectified sinusoid as shown in Figure 2.6.

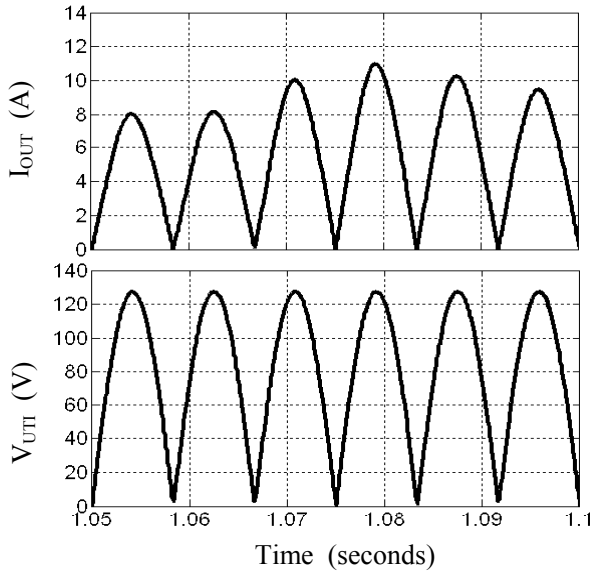


Figure 2.6: I_{OUT} and V_{UTI} for DC/DC Converter

The output voltage of DC/DC converter is just the rectified utility grid voltage. This voltage will be the reference of average current controller to get the synchronized rectified sinusoid current [16].

2.1.4 Feedback Circuits

The feedback portion of the proposed maximum power tracking solar inverter consists of the following blocks:

Average Current Controller provides a smoothly varying control signal V_{CON} to the DC/DC converter to produce rectified and synchronized AC signal to the utility. It compares to a reference current signal, $I_{REF,}$ generated by a multiplier with feed forward compensation to decide the shape and amplitude of I_{OUT} as shown in Figure 2.7.

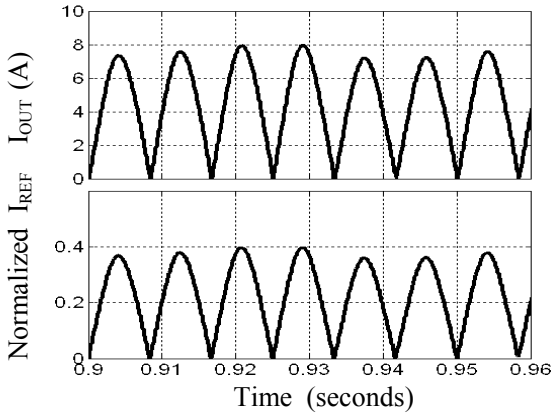


Figure 2.7: Output Current of DC/DC Converter I_{OUT} and Control Signal I_{REF}

Multiplier with feed forward compensation generates the reference rectified sinusoidal signal I_{REF} from V_{UTI} and V_{ERR}. The rectified sinusoidal signal V_{UTI} is properly scaled without being low-pass filtered before being fed to the multiplier's Y input whereas its scaled RMS-squared signal is sufficiently low-pass filtered before being sent to the multiplier's Z input.

Solar array voltage regulation error amplifier regulates the solar array voltage at a level corresponding to the array set-point voltage V_{set} that is controlled to reach its peak-power set-

point voltage. In addition, V_{ERR} will decide the amplitude of I_{OUT}. Solar array output power and the voltage of solar array, with their corresponding control signals, are shown in Figure 2.8 and Figure 2.9.

As shown in Figure 2.8, V_{SET} will decide the output power of solar array. When maximum power point is achieved, V_{SET} will go to steady state to maintain the output power. Different steady states of V_{SET} are corresponding to different array peak-power modes.

Solar array voltage and the output of solar array voltage error amplifier (V_{SA} and V_{ERR}) are shown in Figure 2.9.

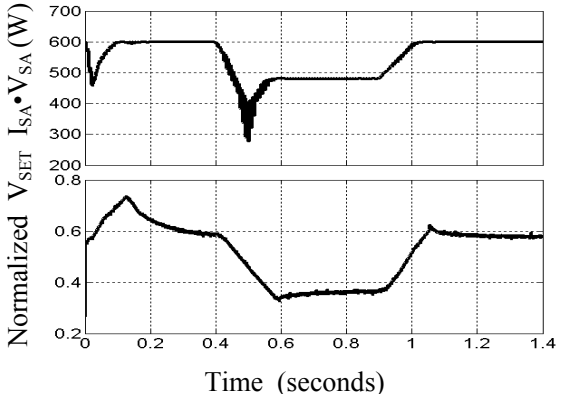


Figure 2.8: Output Power of Solar Array and Output of MPT V_{SET}

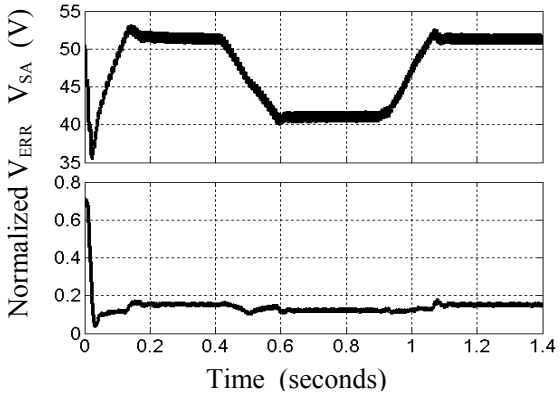


Figure 2.9: Solar Array Voltage V_{SA} and Output of Solar Array Voltage Error Amplifier V_{ERR}

2.1.5 Step Response of MPT

Figure 2.10 demonstrates the robustness of the MPT control when the RMS value of the utility grid voltage steps from 84V to 130V. Solar array power ($I_{SA} \times V_{SA}$) and solar array voltage (V_{SA}) are both restored to their maximum power conditions despite the significant step change.

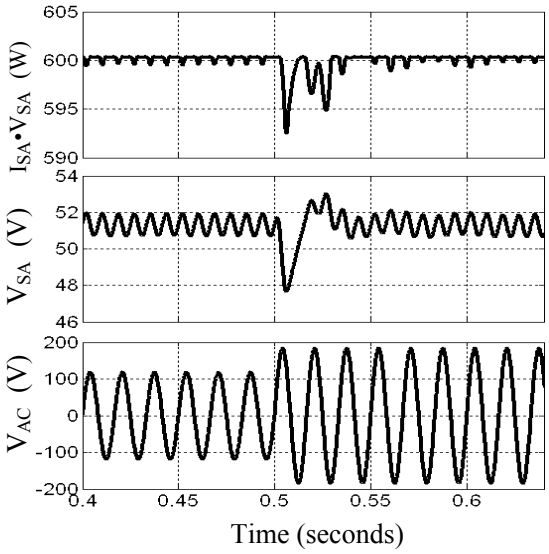


Figure 2.10: Step Response of Solar Array Power $I_{SA} \bullet V_{SA}$, Solar Array Voltage V_{SA} and Utility Grid Voltage V_{AC}

A new control approach for a solar-based inverter that tracks the maximum available power and produces a near unity power factor is presented. It is shown that the proposed approach produce excellent signal-to-noise ratio for the feedback signals, ensuring reliable and robust tracking maximum power while tightly regulating the sinusoidal waveform of AC current supplied to the utility grid with almost unity power factor. Employing a feed-forward compensation technique, coupled with one stage of DC/DC power conversion, the proposed inverter system is simplified when compared to conventional inverter designs. Simulation results

clearly show that the overall system is stable under solar array and utility grid changes. Future work will focus on the control loop design and analysis for robust system stability that specifically deals with the non-linearity of the array source and the resonant behavior of the line-filter. Based on a specific design example, a prototype will be developed after the design to verify the inverter system.

2.1.6 AC Analysis of Average Mode Simulation

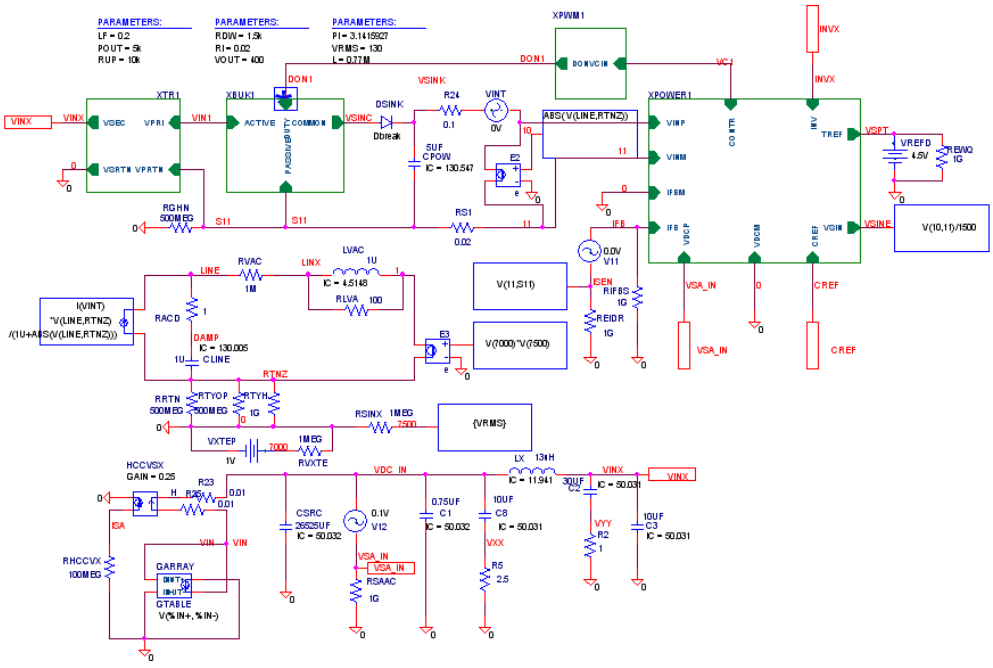
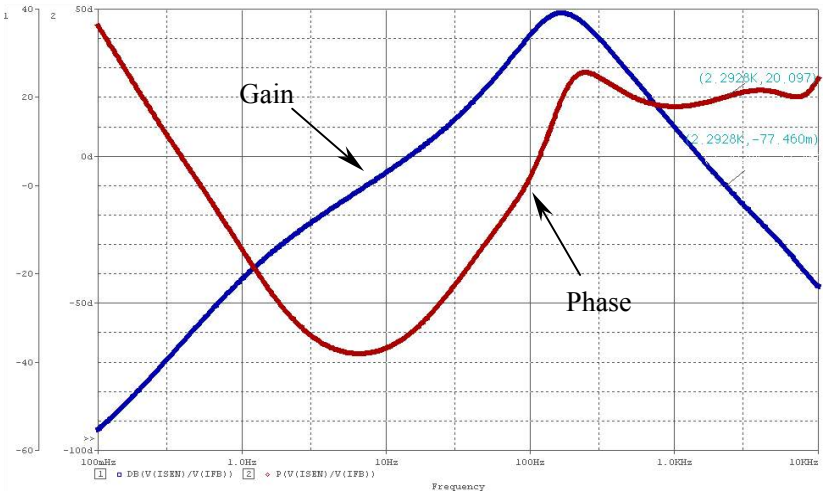


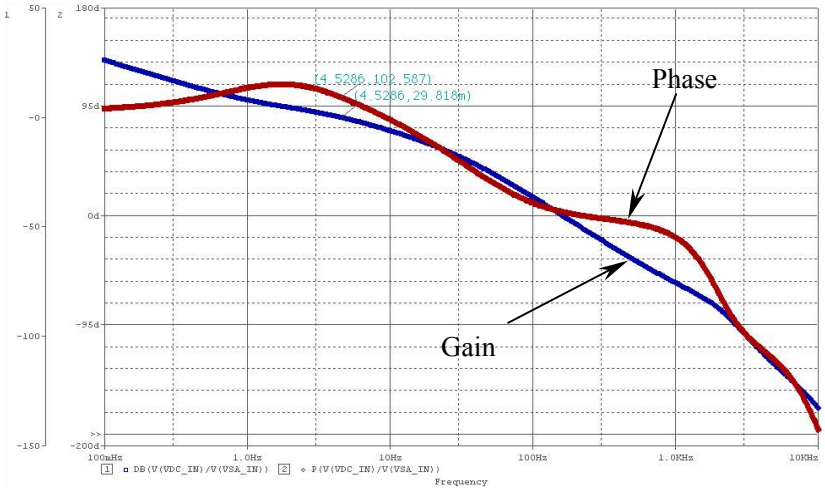
Figure 2.11: Schematics of AC Analysis Average Mode Single-Stage Solar-Based Inverter

AC analysis will verify the bandwidth of solar array voltage regulation and output current regulation of a DC/DC converter, as shown in Figure 2.11. Figure 2.12 shows the bode plots of

these two regulation loops. The two loops' bandwidths are 5kHz and 6Hz, which meet the requirements in Chapter One.



(a) Bode Plot of Solar Array Voltage Regulator



(b) Bode Plot of Output Current Regulator of DC/DC Converter

Figure 2.12: Simulation Results of AC Analysis

2.2 Switching Mode Simulation

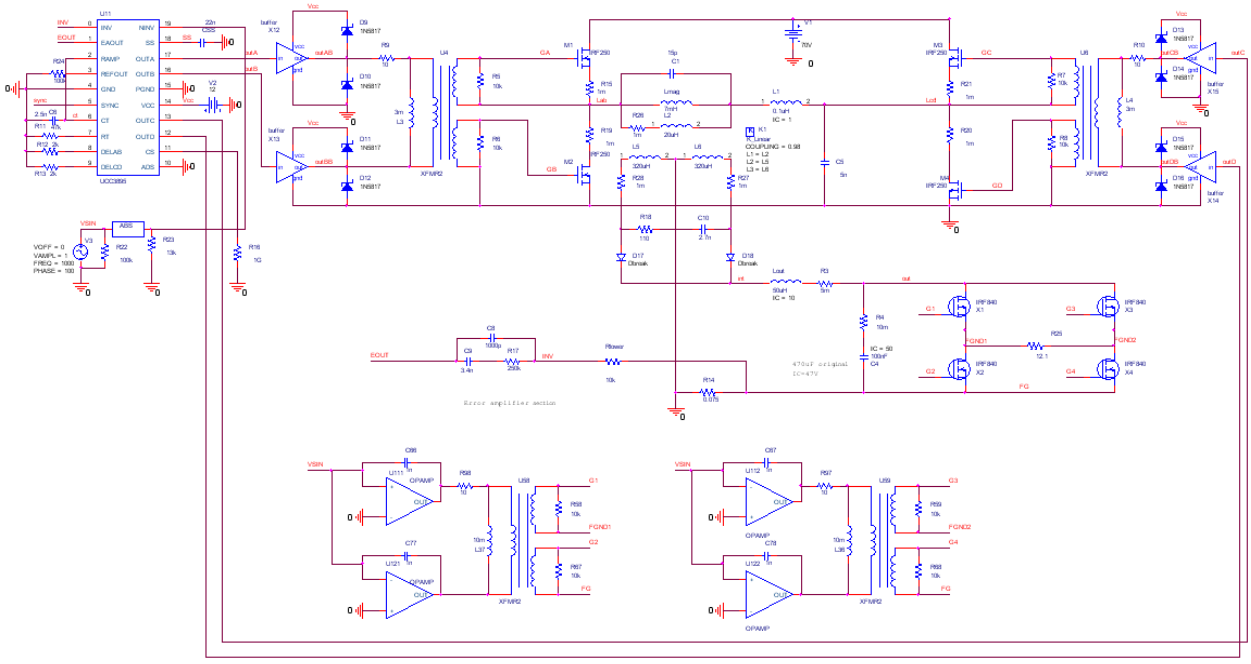


Figure 2.13: Schematics of Switching Mode Simulation

Figure 2.13 shows the schematics of the full-bridge phase-shift DC/DC converter simulation. The controller is UCC3895. The full-bridge switch is IRF250 and the unfolding switch is IRF840. All the gate drivers are isolated by transformers. The solar array was represented by a 70V DC voltage source. The turns ratio of the DC/DC conversion transformer is 1:4. The UCC3895 is working under average current mode control. That means the converter is a current source, which can output rectified sinusoid current strictly followed in the reference. The load is a resistor of 12.1Ω. The full-bridge is operated at 70kHz [18, 19].

Figure 2.15 shows the ZVS of all four switches. Note that the switch current is negative before the switches turn on. That means the body diode is on before the switch turns on. As the

load current decreases to the zero crossing, the ZVS failed. To enlarge the ZVS range, a commutation inductor is used. However, it will reduce the maximum duty ratio of the DC/DC converter.

In addition, a trade-off is needed between the THD and output voltage high frequency ripple. Because the output capacitor will generate a DC offset on output voltage, reducing the output capacitor will increase the high-frequency ripple of the output voltage. To damp this high-frequency ripple, the switching frequency will be increased [20].

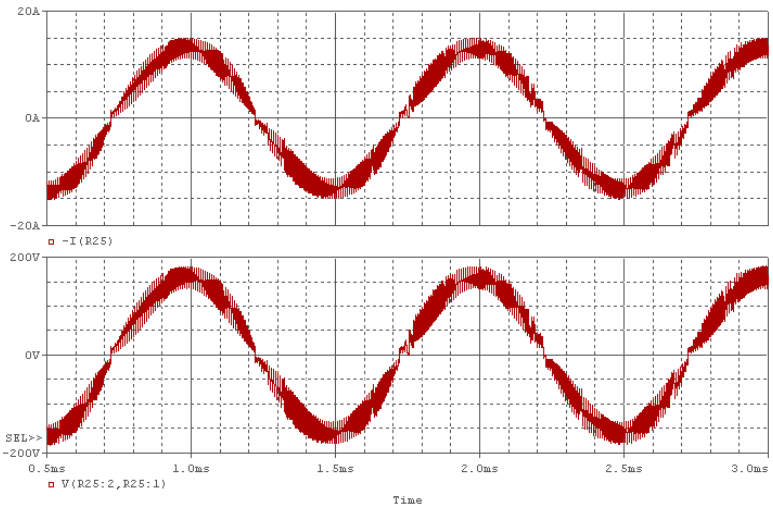


Figure 2.14: Output Current and Voltage

Although the commutation inductor will reduce the output voltage, it will also help to achieve the ZVT and because more inductance energy is stored, and it is much easier to achieve the ZVS. The inductance will affect the system greatly and need to be designed carefully. Because we have voltage drops on the commutation inductor, the more inductance of it, the less

the turns ratio of the main transformer is needed to boost the voltage. Another shortcoming is that the more inductance of it, the less of a maximum duty ratio of the conversion [19].

The filter inductor can help to achieve ZVT, and the filter current will be reflected to the primary side of the transformer, which then helps to freewheel the current during its switch to off. Also, the larger the filter inductor, the lower the output current THD, especially for the switching noise, which can be greatly damped [22].

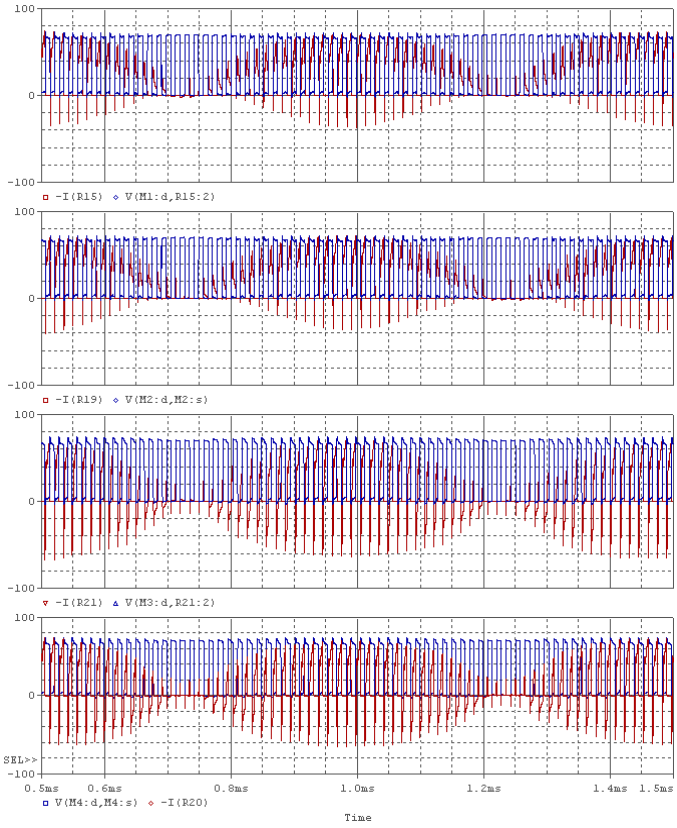


Figure 2.15: Voltage (Blue) and Current (Red) of Full-Bridge Switches

(From Top to Bottom are Switches: A, B, C and D)

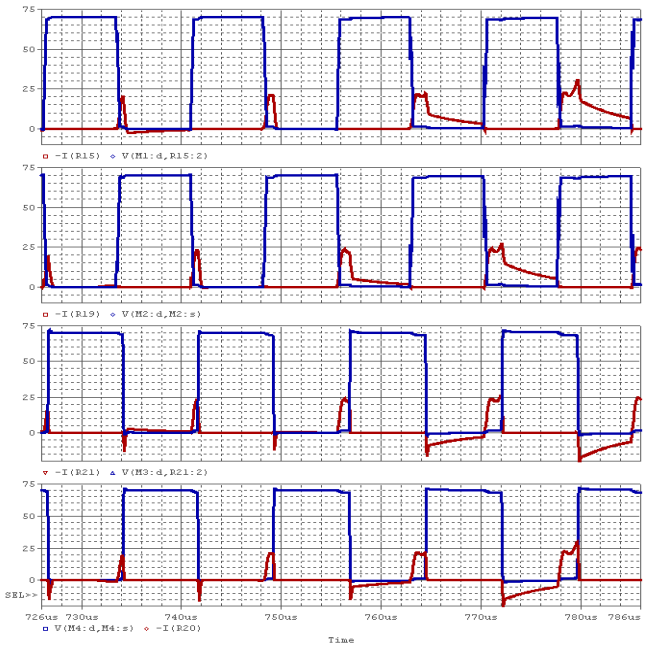


Figure 2.16: Voltage (Blue) and Current (Red) of Full-Bridge Switches

(From Top to Bottom are Switches: A, B, C and D)

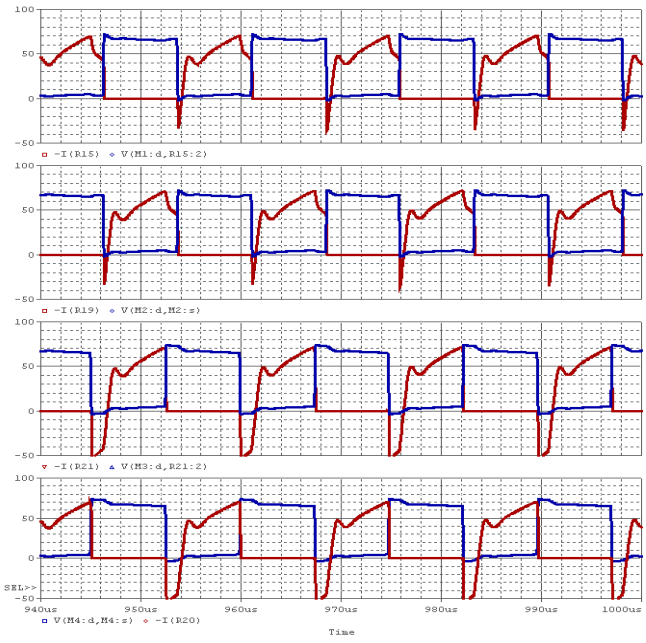
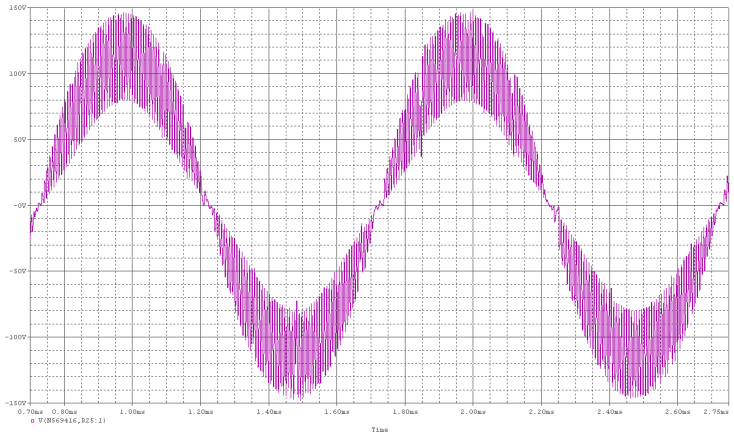


Figure 2.17: Voltage (Blue) and Current (Red) of Full-Bridge Switches

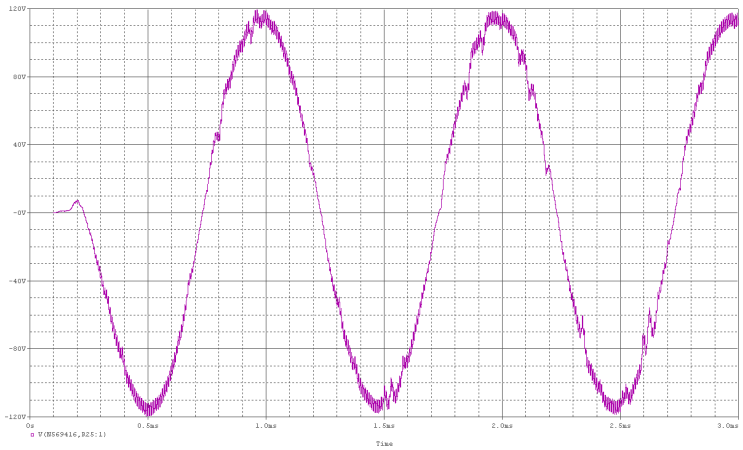
(From Top to Bottom are Switches: A, B, C and D)

The single-staged solar-based grid-connected inverter system also can work on a stand-alone mode, which means that the inverter will supply the load, not the utility grid. At that time, the system should work as the voltage source, not as the current source. To make the system a voltage source, the feedback should be the output voltage, not the output current.

To verify this design, a signal from scaled-down output voltage is taken as a feedback signal in the switching-mode simulation. The simulation results are shown in Figure 2.18.



(a) Output Voltage of (50uH Output Inductor and 100nF Output Capacitor)



(b) Output Voltage (50uH Output Inductor and 1uF Output Capacitor)

Figure 2.18: Simulation Results of Voltage Mode

As Figure 2.18 has shown, the voltage mode still can regulate the output voltage as pure sinusoid and $110V_{rms}$. In addition, as the output filter capacitance increases, the output voltage noise is being reduced.

So far, the switching mode simulation has already verified the inverter controller and ZVS transition. Due to oscillation between the leakage inductance of the secondary side of the transformer and equivalent of parasitic capacitance of rectifier diodes, anode voltage of the rectified diodes has high-frequency ringing. To solve the ringing on the secondary side, the series resistor and capacitor have been applied. However, they decrease the efficiency [22].

To solve the ringing effect on the primary side, two clamping diodes are added as shown in Figure 2.19 [22]. Note, to simplify the simulation, a phase-shift full-bridge DC/DC converter has been built, and all the simulation results are in the steady state.

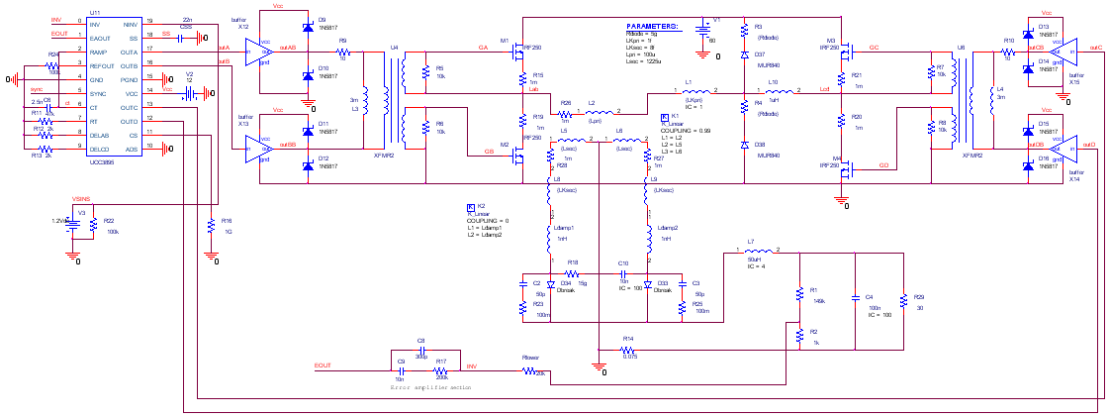


Figure 2.19: Simplified Phase-Shift Full-Bridge DC/DC Converter

To magnify the ringing effect, a real diode, MUR840, is applied as the rectifier on the secondary side. Also, a 50pF capacitor was put in parallel. The leakage inductance on the secondary side is 8uH. All these values are larger than the real situation.

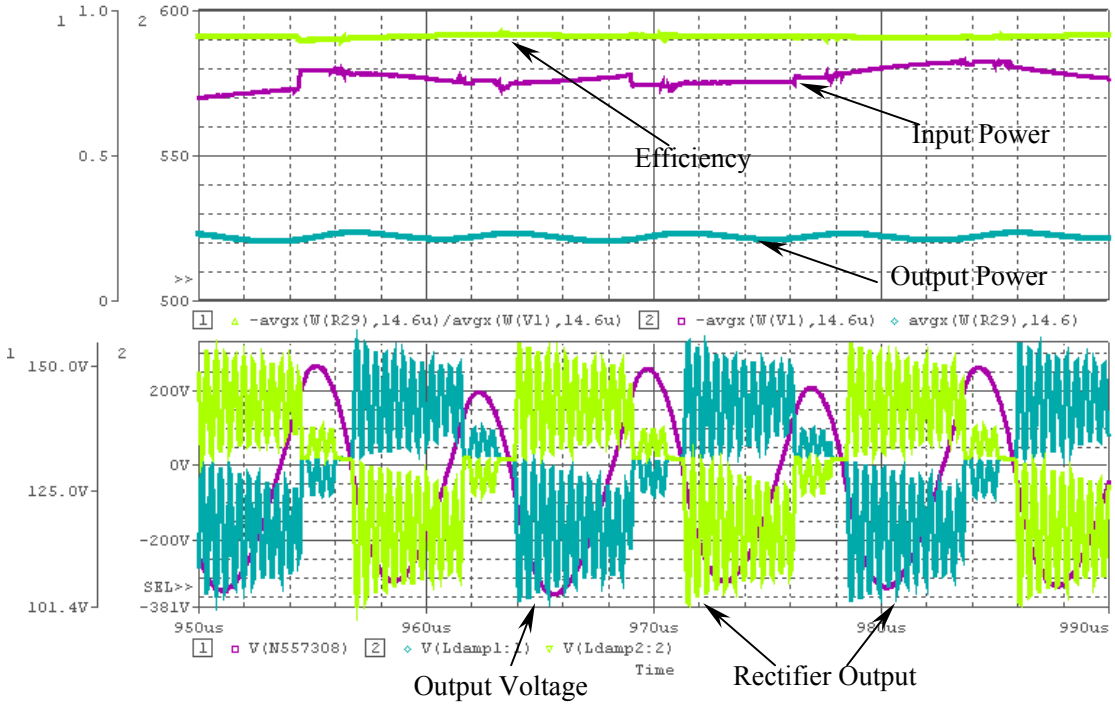


Figure 2.20: Simulation Results without Clamping Diodes

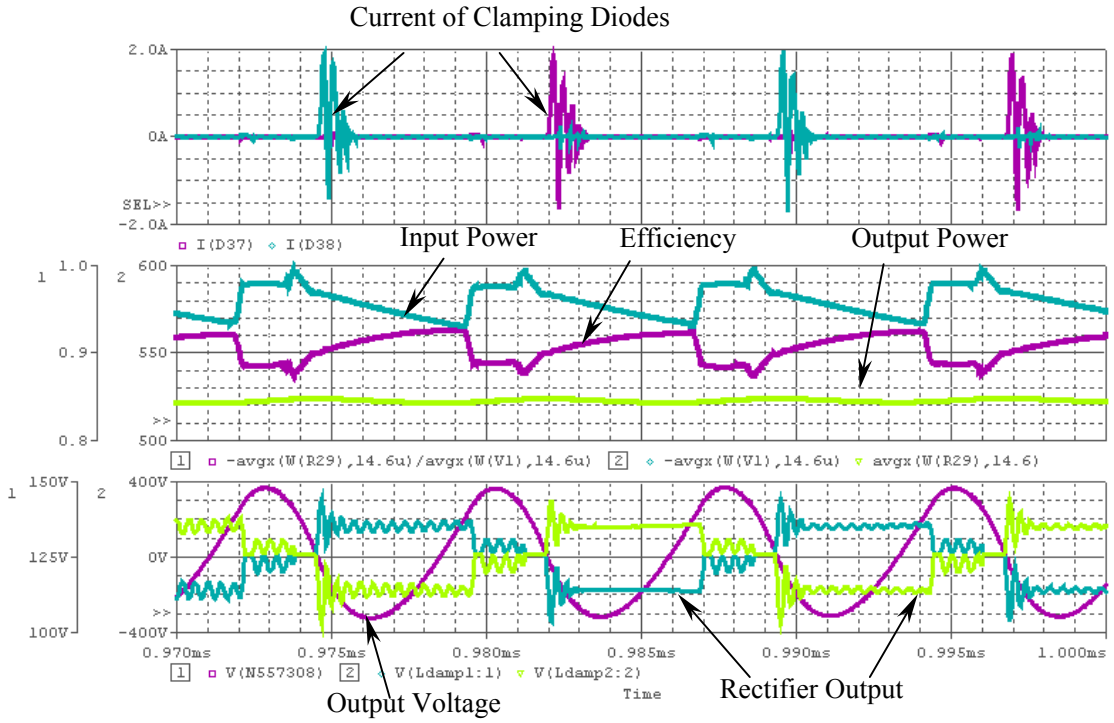


Figure 2.21: Simulation Results with Clamping Diodes

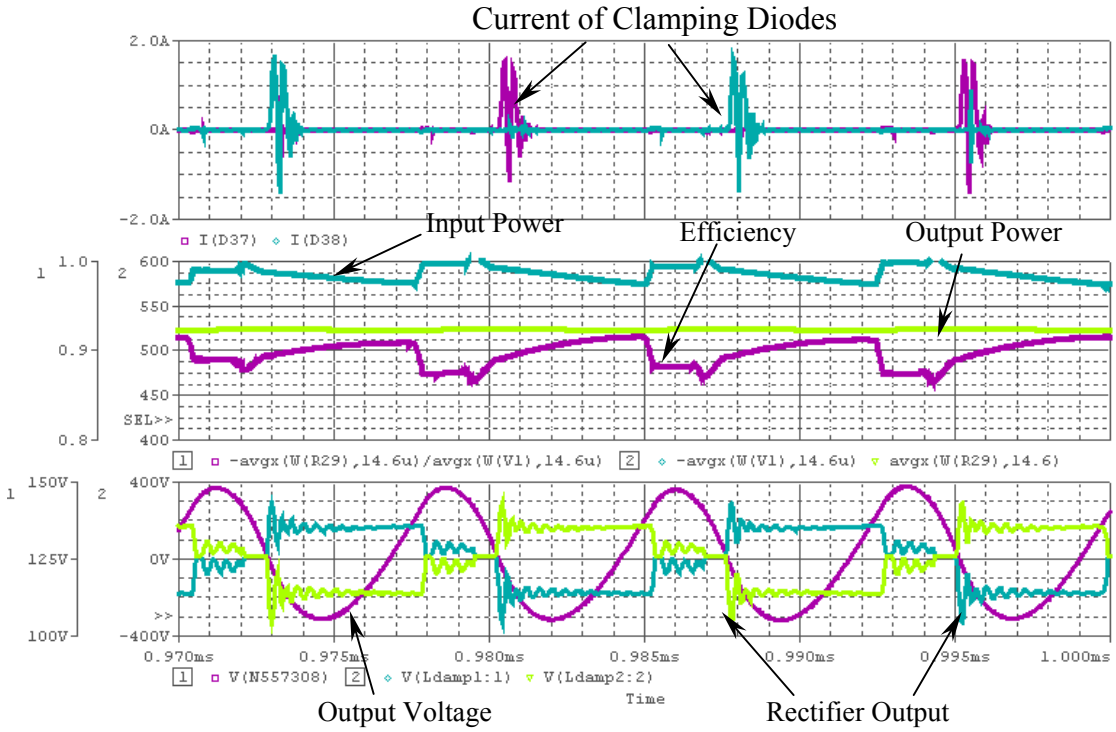


Figure 2.22: Simulation Results with Clamping Diodes, Series Resistor and Capacitor

The figure above shows the simulation results without any clamping diodes, series resistor or capacitor on the secondary side, as shown in Figure 2.19. The ringing effect on the secondary is severe. As Figure 2.21 shows, adding two clamping diodes and commutation inductor 2uH on the primary side can damp the ringing, but efficiency is decreased.

As Figure 2.22 shows, the ringing can be dampened further by adding the clamping diodes on the primary side and a resistor and capacitor in both series. However, the efficiency is continuously decreased [22, 23] in this scenario.

All the simulation results are under the worst conditions, such as leakage inductance and parallel capacitance of the rectifier. The experimental results should be much better than this.

CHAPTER THREE: DESIGN OF DC/DC CONVERTER

3.1 System Block Diagram and Description

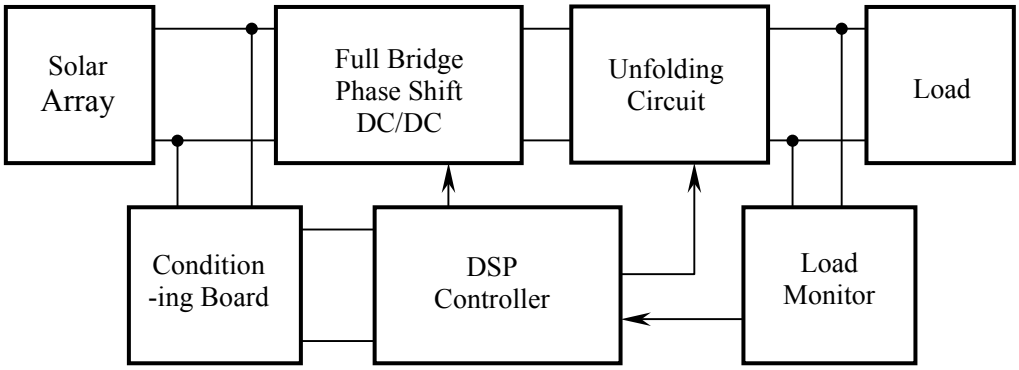


Figure 3.1: Block Diagram of a Solar-Based Inverter System

As Figure 3.1 shows, the solar-based inverter system will include five separate parts: full-bridge phase-shift DC/DC converter, unfolding circuit, conditioning board, DSP controller board and load monitor. The conditioning board senses the voltage and current of the solar array and sends these signals to the DSP controller board. DSP will regulate the solar array working under the maximum power point, and driving the full-bridge phase-shift DC/DC converter and unfolding the circuit to deliver sinusoid current to the load or utility grid. The load monitor will examine the load character and decide the phase lag or phase lead of the output current with the utility grid or load. Integration with a load monitor will let the system conquer the flaw of unidirectional current source, allowing the unidirectional current source to have the ability to

handle the bidirectional load or reactive load. In addition, this function will be achieved by the proper the design of digital controller [24].

Except for the load monitor, other blocks have been designed and even have prototypes ready. The design of the load monitor needs more time and research. The requirements for the load monitor may not be very strict, because the load or utility grid may not change too quickly or very often. Like a refrigerator, it will start to work after half an hour. In addition, without any power factor correction, the power factor of it may as low as 0.8.

The prototype will be built block by block. First, the DC/DC converter will be built. After testing and debugging, the unfolding circuit will be built. Then, conditioning board and DSP controller follow.

Separating the power stage into DC/DC converter and unfolding circuit can increase the time efficiency of the whole system development. The unfolding circuit is simple and fully designed. The DC/DC converter may have major changing. In the next phase, the topology of the DC/DC converter may be another bi-directional topology. Therefore, the unfolding circuit can be used in next phase.

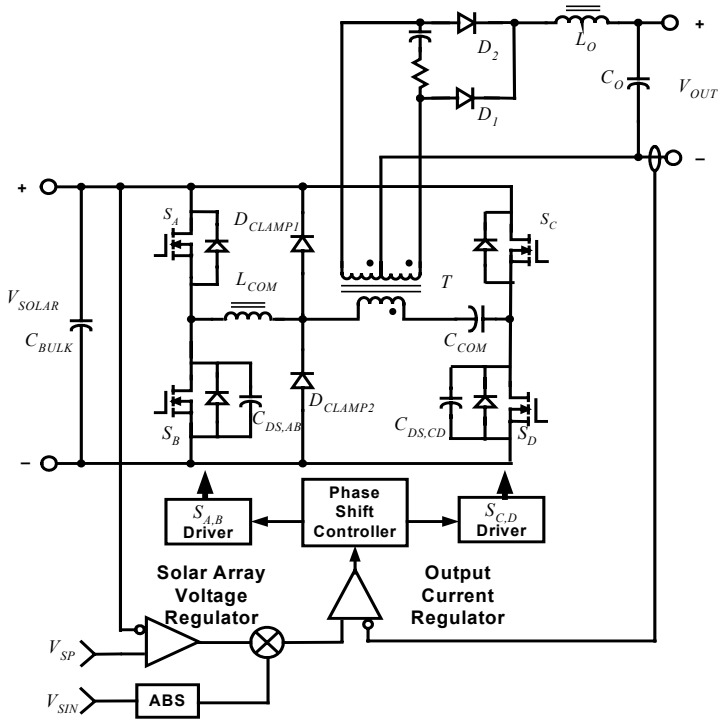


Figure 3.2: Block Diagram of a Full-Bridge Phase-Shift DC/DC Converter

The schematics of the full-bridge phase-shift converter are shown in Figure 3.2, and there are two input signals. V_{SP} controls the voltage of solar array, which is generated by the DSP controller. V_{SIN} is the reference signal for the output current shaping. It is scaled down from the voltage of utility. The phase shift controller is UCC3895, which generates phase-shifted modulation driving signal according to the magnitude of the current through the switches. The more output current, the more overlap of driving signals. MOSFETs drivers are IR2110s. Each IR2110 drives one switch leg. The communication inductor L_{COM} facilitates the Zero Voltage Switching (ZVS) of full bridge. The communication capacitor C_{COM} only can let AC components of the input current pass through and will not let the transformer T be saturated by DC components of the input current. D_{CLAMP1} and D_{CLAMP2} will clamp the oscillation caused by the

leakage inductance of the transformer and parasitic capacitance of rectifier diodes D_1 and D_2. On the secondary side of the transformer, another damper is used. $C_{DS,\ AB}$ and $C_{DS,\ CD}$ are the equivalent capacitance of switches A, B, C and D, which should be considered on the ZVS analysis.

The unfolding circuit will be a separated board, which has its own MOSFET or IGBT driver circuit on the board. The reason for the separated design is that this unfolding circuit board can be used by different topologies of DC/DC converters [24].

As previous experimental results have shown, this DC/DC converter can output rectified sinusoid shape current to an unfolding circuit and regulate the solar array voltage to its maximum power point. Except for the unfolding circuit board, the whole inverter system still needs another two PCB boards of DSP MPPT controller board and conditioning board.

Output current feed-forward compensation is not included on this prototype. In the next stage, feed-forward compensation will be applied in analog or digital method.

3.2 Full-Bridge Phase-Shift Controller Design

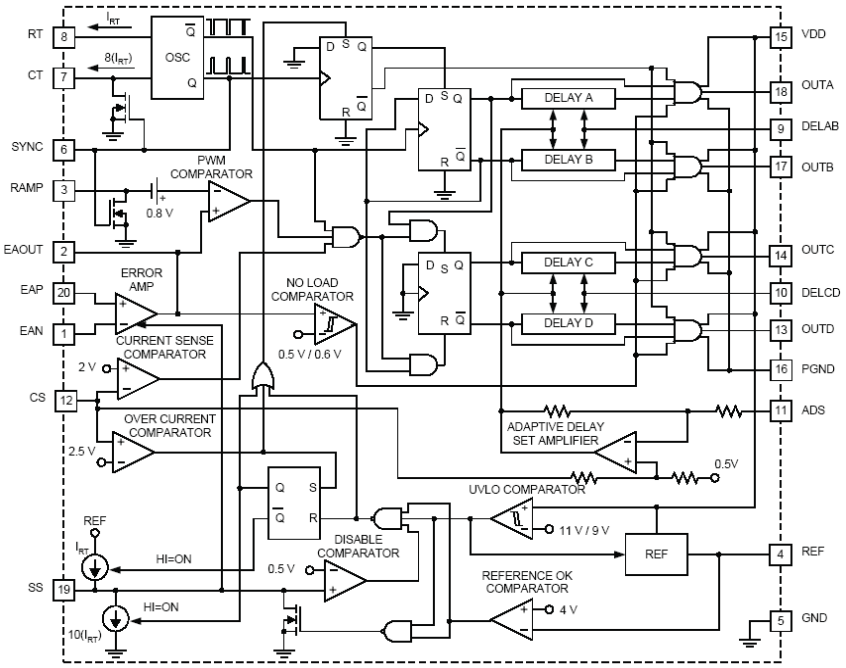


Figure 3.3: Block Diagram of UCC3895 [20]

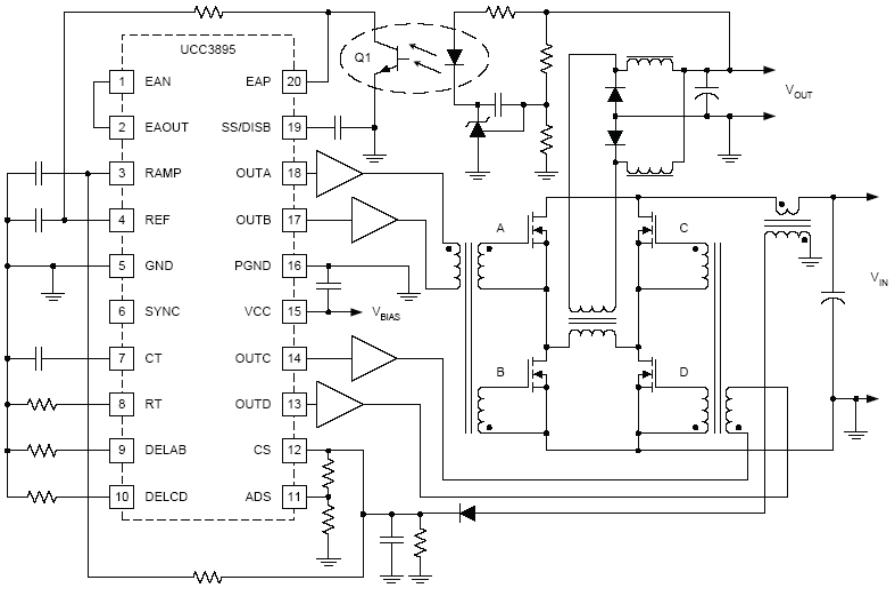


Figure 3.4: Typical Application of UCC3895 (Voltage Mode) [20]

The UCC3895 is a phase-shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used as either an average voltage/current mode or a peak current mode controller.

EAOUT: Error Amplifier Output. It is connected to the non-inverting input of the PWM comparator and the no-load comparator as shown in Figure 3.3. It is also clamped to the soft-start voltage of the SS pin. The no-load comparator is a hysteretic comparator. When EAOUT is less than 500mV, no-load comparator shuts down the output of UCC3895, and when EAOUT is greater than 600mV, it turns on the output again [20]. This feature of UCC3895 can shut down the system when the faults happen, such as over voltage, under voltage, over current and over temperature. There are several pins of UCC3895 that can shut down the power stage, such as EAOUT, CS, SS/DISA and REF. Properly choosing a design can make the protection modules' design much easier. Note that the RAMP has 0.8V DC offset in Figure 3.3, which can achieve the zero output current at the zero crossing of sinusoid current. To clamp the EAOUT under 0.8, a series diode will be added, just like UC3842/3.

CT: Oscillator Timing Capacitor. A smaller C_T and a larger R_T combination decrease the fall times of the C_T waveform. Therefore, the value of the external capacitor connecting CT to the ground should range from 100pF to 880pF. On the contrary, the increasing fall time of CT will increase the SYNC pulse width, then the maximum phase shift between OUTA, OUTB, OUTC and OUTD outputs will be decreased, which limits the maximum duty cycle of the converter. Due to programmed current charges CT by the oscillator, the waveform on CT is a

saw tooth, with a peak voltage of 2.35V. The period of the oscillation is calculated by the following formula from the datasheet:

$$t_{OSC} = \frac{5 \cdot R_T \cdot C_T}{48} + 120ns$$

To minimize the fall time of C_T, the value of R_T is chosen to be the maximum value: 120kΩ. The switching frequency is 200kHz, which means the frequency of oscillation is 400kHz. Therefore, C_T=190pF.

CS: Current Sense. It is the inverting input of the Current Sense comparator and the non-inverting input of the over-current comparator and the ADS amplifier. The current sense signal can be used for cycle-by-cycle current limiting and for over current protection in all cases with a secondary threshold for output shutdown [20].

In this application, the UCC3895 will work in the average current mode instead of peak current mode. Therefore, the current sense comparator is not necessary. To set the adaptive delay time accordingly, it is still necessary to have the current sensing signal on the CS pin. The current sensing signal will trigger the Current Sense comparator at 2.0V and Over Current comparator at 2.5V. In the normal condition, the signal on CS should be less than 2.0V.

Only the switch current needs to be sensed directly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation [20].

Note that the maximum input current is 3kW/48V=62.5A, or 1kW/48V=20.8A, and the resistor at the secondary side of the current sensing transformer is 5Ω. Therefore, the turn's ratio

of the current sensing transformer is 2V/5Ω:62.5A=1:150 or 1:50 as shown below. It also shows that filtering is added to the transformer secondary in order to reduce noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.

In addition to position and reset considerations, actual current transformer construction must be considered. Using current transformers that have been designed and manufactured for operation at 20 kHz will not give good performance at switching frequencies of 200 kHz and greater. Low frequency designs generally have too much leakage inductance to be used for high-frequency operation and can cause inaccurate sensing and/or noise problems.

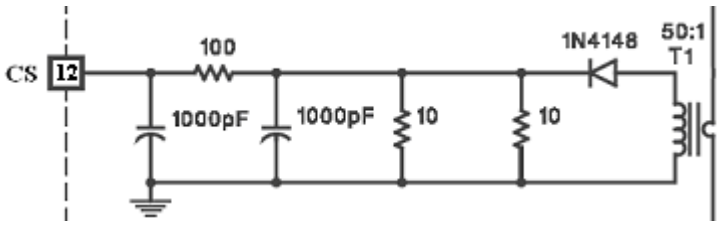


Figure 3.5: Current Sensing Circuit [21]

DELAB, DELCD: Delay Programming Between Complementary Outputs. DELAB programs the dead time between switching of OUTA and OUTB, and DELCD programs the dead time between OUTC and OUTD. This delay is introduced between complementary outputs in the same leg of the external bridge. In addition, during this delay time, the resonant switching takes place. The UCC3895 allows the user to select the delay, in which the resonant switching of the external power stages takes place [20]. Separate delays are provided for the two half-bridges to

accommodate differences in resonant capacitor charging currents. The delay in each stage is set according to the following formula:

$$t_{DELAY} = \frac{25 \times 10^{-12} \cdot R_{DEL}}{V_{DEL}} + 25ns$$

Because DELAB and DELCD only can output 1mA maximum, the proper delay resistors need to be selected to make sure the output current is less than 1mA. Figure 3.6 illustrates the resistors needed to program the delay periods and the adaptive delay set function.

In the preliminary experiment, the delay function will be simplified by short ADS with CS directly. That means V_{DEL}=0.5V and selecting R_{DEL}=1.5kΩ, t_{DELAY}=100ns. The final design of the delay function will be done with more simulation and experiments.

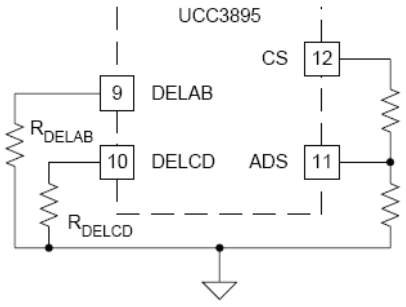


Figure 3.6: Delay Circuit [20]

ADS: Adaptive Delay Set. This function sets the ratio between the maximum and minimum-programmed output delay dead time. When the ADS pin is directly connected to the CS pin, there is no delay modulation. When ADS is grounded, there is maximum delay

modulation. In this case, delay time is four times longer when CS = 0 than when CS = 2.0V (the peak current threshold), and ADS changes the output voltage on the delay pins DELAB and DELCD by the following formula [20]:

$$V_{DEL} = \left[0.75 \cdot \left(V_{CS} - V_{ADS}\right)\right] + 0.5V$$

ADS must be limited to between 0V and 2.5V and must be less than or equal to CS. DELAB and DELCD also will be clamped to a minimum of 0.5V [20].

In the preliminary experiment, the ADS pin will be directly connected to the CS pin, which will make no delay. In addition, the CS pin will be grounded also, which will simplify the whole system and remove the unexpected effect of noise. When all the other circuits work well, a resistor will be used between the ADS pin and CS pin. In addition, CS will receive the feedback signal of the input current to let UCC3895 generate the delay properly according to the value of the input current of DC/DC converter.

The Adaptive Delay Set feature (ADS) allows the user to vary the delay times between switch commands within each of the converter's two legs. The delay time modulation is implemented by connecting ADS (pin 11) to CS, GND or a resistive divider from CS to GND to set V_{ADS}. From the equation for V_{DEL} above, if ADS is tied to GND then V_{DEL} rises in direct proportion to V_{CS}, causing a decrease in t_{DELAY} as the load increases. In this condition, the maximum value of V_{DEL} is 2V. If ADS is connected to a resistive divider between CS and GND, the term (V_{CS}-V_{DS}) becomes smaller, reducing the level of V_{DEL}. This will decrease the amount of delay modulation. In the limit of ADS tied to CS, V_{DEL}=0.5V and no delay modulation occurs. In the case with maximum delay modulation (ADS=GND), when the circuit goes from light load

to heavy load, the variation of V_{DEL} is from 0.5V to 2V. This causes the delay times to vary by a 4:1 ratio as the load is changed. The ability to program an adaptive delay is a desirable feature because the optimum delay time is a function of the current flowing in the primary winding of the transformer and can change by a factor of 10:1 or more as the circuit loading changes. [20, 25]

EAP: The non-inverting input to the error amplifier. The sinusoid reference signal will be connected to this pin to regulate the output current following it.

EAN: The inverting input to the error amplifier.

This 7MHz error amplifier will be used as the output current regulator in this application. A will be constructed to regulate the output current following the sinusoid reference signal as shown in Figure 3.7. In addition, the transfer function is:

$$H(j\omega) = \frac{1 + j\omega R_2 C_1}{-\omega^2 R_2 C_1 C_2 + j\omega(C_1 + C_2)} \frac{1 + j\omega(R_1 + R_3)C_3}{R_1 + j\omega R_1 R_3 C_3}$$

This reference signal is generated by multiplication of the output of the solar array voltage regulator and the scaled utility grid voltage. As previously reported, this configuration will regulate the output voltage of solar array to its MPPT and the output current to pure sinusoid.

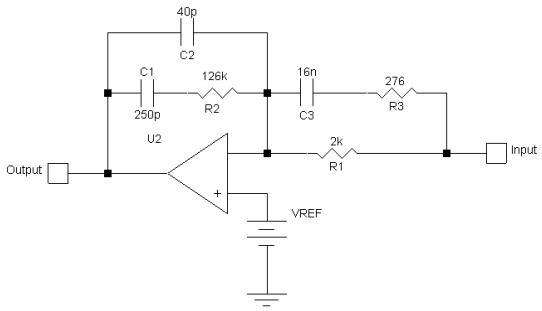


Figure 3.7: Three-Pole Two-Zero Current Error Amplifier

OUTA, OUTB, OUTC and OUTD: The 4 outputs are 100mA complementary MOS drivers, and are optimized to drive FET driver circuits. OUTA and OUTB are fully complementary, assuming no programmed delay. They operate near 50 percent duty cycle and one-half the oscillating frequency. OUTA and OUTB are intended to drive one half-bridge circuit in an external power stage. OUTC and OUTD will drive the other half-bridge and will have the same characteristics as OUTA and OUTB. OUTC is phase shifted with respect to OUTA, and OUTD is phase shifted with respect to OUTB. Note that changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50 percent duty ratio on OUTC and OUTD during those transients [20, 26].

To increase the driving ability and driver for the upper MOSFETs of the full-bridge, two IR2110 MOSFET drivers will be applied.

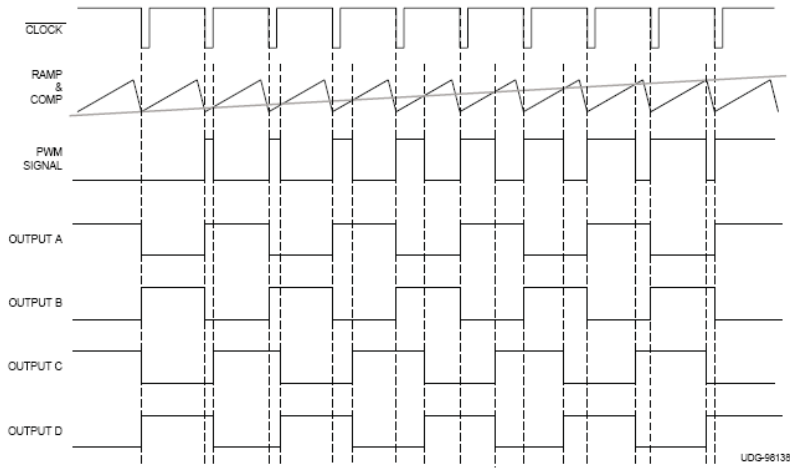


Figure 3.8: UC3895 Timing Diagram (No Output Delay) [20]

RAMP: The inverting input of the PWM comparator. This pin receives either the CT waveform in voltage and average current mode controls.

RT: Oscillator timing resistor. The oscillator in the UCC3895 operates by charging an external timing capacitor, CT, with a fixed current programmed by R_T. R_T current is calculated as follows:

$$I_{RT} = \frac{3.0V}{R_T} = \frac{3}{120k} = 25\mu A$$

3.3 Transformer and Inductor Design

Normally, the starting point of transformer design should be an estimate of an acceptable temperature rise, and a 25˚C total rise is quite typical. Next, the core Area Product can be calculated using the formulas to approximate the core size for a conventional design. However, the first prototype is to verify the control concept and examine the application of full bridge topology. Therefore, the transformer and inductor design will not follow the industrial standards strictly [27, 28].

After all the concepts are verified, the second prototype will apply commercial planar transformer and inductor, which have better performance and out-looking.

The E shape Ferrite Cores we have are listed below:

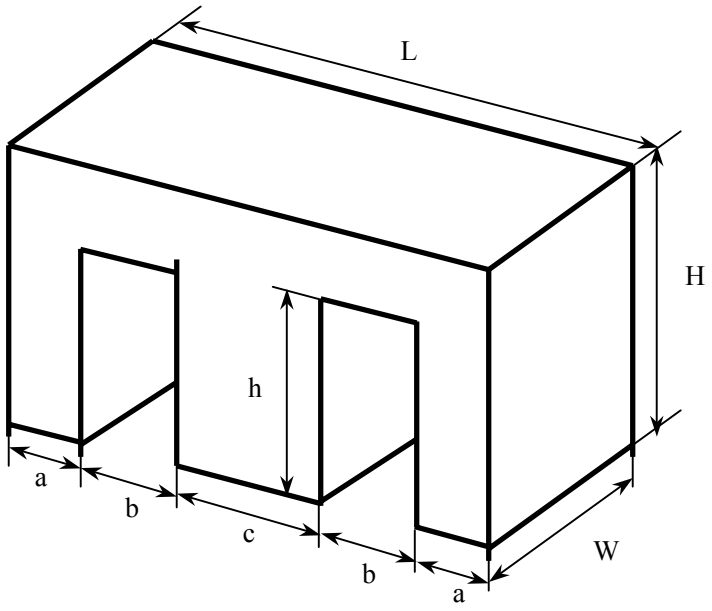


Figure 3.9: Specs of E Ferrite Core

Table 3.1: Specs of Transformer Ferrite Core

	L (mm)	*H* (mm)	*W* (mm)	*a* (mm)	*b* (mm)	*c* (mm)	*h* (mm)
E Core	56	27.6	20.8	8.6	10.6	17.2	19.2

Assume $\Delta B < 3000$ Gauss, then B_{max}=1500 Gauss, -B_{max}= -1500 Gauss.

The required number of primary turns is calculated by solving Faraday's Law using the known parameters [29].

$$N_{PRI} = V_{IN} \cdot t_{ON} \cdot 10^4 / (A_e \cdot \Delta B)$$

In this particular design:

V_{IN}=60·80%=48Vdc(min)

D_{MAX}=0.8

t_{ON}=4μsec

$f_{transformer}$=100kHz

A_e=c·W=3.58cm^2

ΔB=0.3Tesla

Therefore:

$$N_{PRI} = 48 \cdot 4 \times 10^{-6} \cdot 10^4 / (3.58cm^2 \cdot 0.3T)$$

$$N_{PRI} = 18 \text{ turns (estimated)}$$

The number of turns for each secondary winding is calculated knowing the available volt-second product on the primary winding and the desired output voltage. The exact transformer primary to the secondary turns ratio (N) is derived from the following relationships used for any buck-derived converter:

$$V_{OUT} = V_{IN(MIN)} \cdot D_{MAX} / (N_{PRI} / N_{SEC})$$

where D_{MAX} is the maximum obtainable duty cycle of the converter, which occurs at the minimum input voltage, $V_{IN(MIN)}$. In this application, V_{OUT} is the peak value of the output voltage, which is 155.54Vdc.

Substituting the turns ratio N=N_{PRI}/N_{SEC} into the above equation and solving:

$$N = V_{IN(MIN)} \cdot D_{MAX} / V_{OUT}$$

$$N = 48 \cdot 0.8/155.54 = 0.25 \text{ (estimated)}$$

Therefore, the secondary number of turns is:

$$N_{SEC} = N_{PRI} / N = 18 / 0.25 = 72 \text{ turns}$$

When an inductor filters DC current, it tends to be saturated. The inductance needs to be constant even when maximum DC current is passing through it. In this case, air gap may be needed to get rid of saturation and keep the inductance constant.

The maximum current of the output filter inductor is:

$$I_{O,MAX} = 120\% \cdot \sqrt{2} \cdot P_O / V_O = 120\% \cdot 1.414 \cdot 1000/110 = 15.4A$$

In addition, the specs of inductor Ferrite Core are:

Table 3.2: Specs of Inductor Ferrite Core

	L (mm)	*H* (mm)	*W* (mm)	*a* (mm)	*b* (mm)	*d* (mm)	*h* (mm)
E Core	48.9	24.7	16.4	7.1	10.2	16.36	18.1

Without air gap, the inductance is:

$$L = \frac{\mu_o \cdot \mu_r \cdot N^2 \cdot S}{l}$$

where μ_r is the relative material permeability 1500~2000; μ_0 is the permeability of free space $4\pi\times10^{-7}$Wb·A^{-1}·m^{-1}; N is the number of coil turns; S is the cross section area of the iron powder corn 2.1×10^{-4}m^2 and l is length of the magnetic loop1.27×10^{-1}m.

To filter switching noise, we need 100μH inductance at least. Solving N:

$$N = \sqrt{\frac{L \cdot l}{\mu_o \cdot \mu_r \cdot S}} = \sqrt{\frac{100\times10^{-6} \cdot 1.27\times10^{-1}}{4\pi\times10^{-7} \cdot 1500 \cdot 2.1\times10^{-4}}} = 4 \text{ (estimated)}$$

Check B:

$$B = \mu_o \mu_r H = \mu_o \mu_r \frac{IN}{l} = 4\pi\times10^{-7} \cdot 1500 \frac{15.4\times4}{1.27\times10^{-1}} = 9138 > 3000 \text{ Gauss}$$

Therefore, air gap is necessary because μ_r=1500>>1. Then compute the inductance caused by air gap:

$$B = \mu_o H = \mu_o \frac{IN}{l_o} = 1.25 \frac{IN}{l_o} \text{ (Gauss)}$$

where l_0 is the length of air gap.

If $B < 3000$：

$$l_o > \frac{1.25IN}{3000}$$

$$L = \frac{\mu_o \cdot N^2 \cdot S}{l_o} = \frac{\mu_o \cdot N^2 \cdot S}{\frac{1.25IN}{3000}} = \frac{3 \times 10^{-5} NS}{I}$$

Solving N:

$$N = \frac{L \cdot I}{3 \times 10^{-5} \cdot S} = \frac{100 \times 10^{-6} \cdot 15.4}{3 \times 10^{-5} \cdot 2.1} = 25 \text{ turns (estimated)}$$

And solving l_0:

$$l_o = \frac{1.25IN}{3000} = \frac{1.25 \cdot 15.4 \cdot 25}{3000} = 1.6 \text{ mm}$$

The communication inductor will follow the rule of try-and-error. In addition, simulation will be used to find the proper inductance for it. All of the transformer and the inductor will be wound manually in the laboratory, using an LC meter to measure them [43].

3.4 Driver Circuit Design

In this prototype, there are two options to drive the full bridge MOSFETs. One is the gate-driving transformer as shown in the schematics of simulation; the other one is IR2110 or

HIP2500 [30]. The isolation provided by the gate-driving transformer is unnecessary in this application. So using IR2110 can make the design simpler.

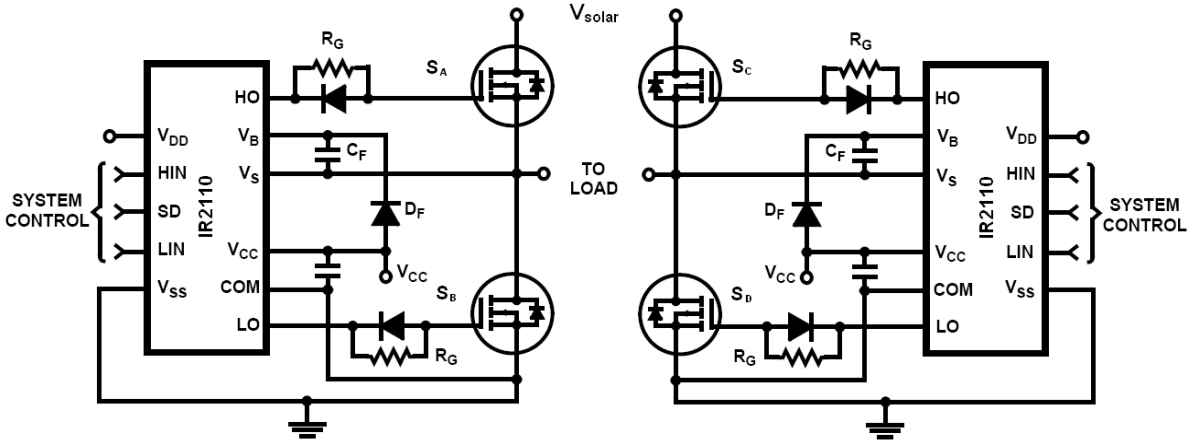


Figure 3.10: Driver Circuit [30]

Figure 3.10 shows the circuit of MOSFETs driver that uses IR2110. Note that the SD pin of IR2110 can be used as a disable function pin as shown in Figure 3.11.

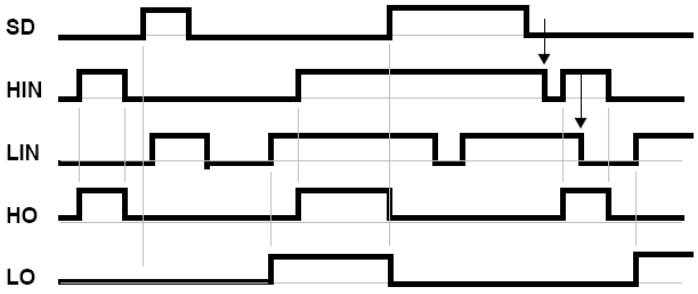


Figure 3.11: Input Timing Diagrams [30]

This function can be used by protection modules to shut down the system in any emergency conditions. Note that the same function also can be done by CS, SS or REF pins of UCC3895.

For most MOSFETs and IGBTs, there is a point at which increasing gate-to-source voltage yields no significant reduction in switch forward drop. Usually, this occurs at about 8 to 9 volts. Avoid overcharging the gate of the power switch because the higher the gate voltage is the longer it takes to turn off the device [37, 38]. In addition, more charge must be transferred, which dissipates more power both in the IR2110 and in the switch device.

The upper bias is maintained by the Bootstrap Capacitor C_F between refresh cycles. A refresh cycle is defined as the time that elapses between conduction periods of the lower power switch and/or its body diode or flyback diode. Sometimes compromises on the size of the bootstrap capacitor must be made. For example, the capacitor should not be so large as to require an excessively long refresh period. Nor should it be so small that the voltage drops below the undervoltage trip point during the upper switch conduction period.

In any event, this capacitor C_F must have sufficient charge to dump into the bootstrap capacitor whenever the VS terminal moves toward COM. This happens when the lower switch is on and usually whenever the upper switch has just been turned off. If R_G is too small it tends to reduce the effective dead time and increase shoot-through tendency. In addition, switching dv/dt increases EMI. $R_G \times C_F$ time constant for too long causes excessive power device switching loss. In addition, if R_G is too big, it may fail to hold the gate low when the opposing power device turns on, either tending to turn on the device prematurely or slow desired turn-off, due to the Miller Effect. One may need to bypass R_G with an anti-parallel signal diode [30, 39].

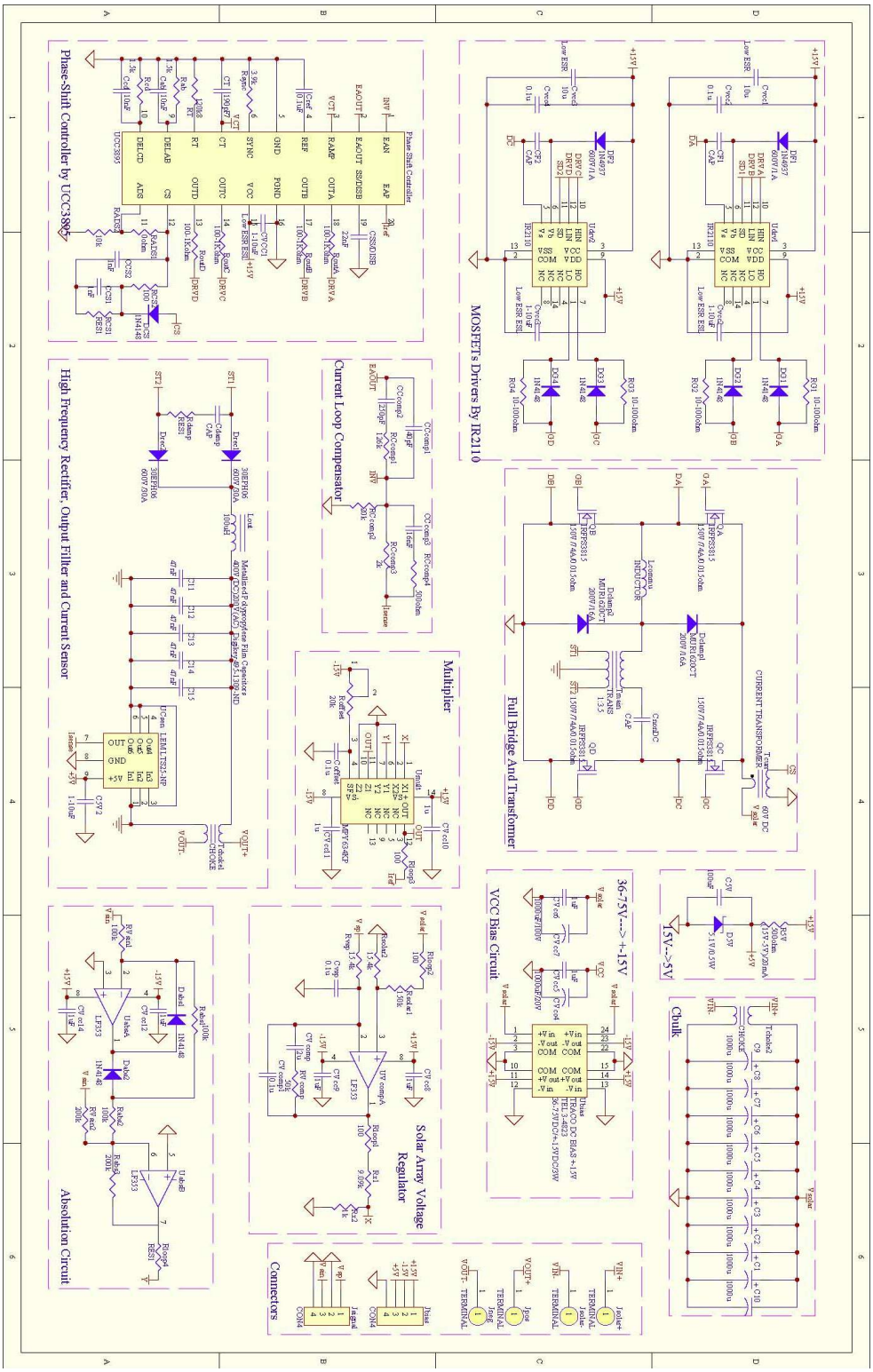


Figure 3.12: Schematics of a Full-Bridge Phase-Shift DC/DC Converter

3.5 Key Component Selection

- **MOSFET**

The input source is solar array or solar array simulator, and the voltage is less than 100V. The output power of the converter is 1kW, but the load can be 3kW for 20 cycles, which is 0.333sec. Assuming power conversion efficiency is 80 percent and the minimum input voltage is 40V for 1kW, the maximum input RMS current is 32A. It will be 96A when 3kW. To meet the short time 3kW output power, thermal issue is very important. To get high efficiency, the ON-resistance of the MOSFETs should be as low as possible [44].

Table 3.3: Specs of Full-Bridge MOSFETs

Model	IRFPS3815 HEXFET	IRFSL52N15D HEXFET
Polarity	N	N
Package	TO-274AA	TO-262
VBRdss (V)	150	150
RDS(on) (mΩ)	15.0	32.0
ID @ 25C (A)	105	60
Id @ 100C (A)	74	43

The MOSFETs of the unfolding circuit will conduct maximum current of 1kW/110V×1.414 = 12.8A, and 38.6A under 3kW. The maximum voltage will be 110×1.414 = 156V.

Table 3.4: Specs of Unfolding Circuit MOSFETs

Model	IRFP264N HEXFET	IRFP264 HEXFET

Polarity	N	N
Package	TO-274AC	TO-274AC
VBRdss (V)	250	250
RDS(on) (mΩ)	60.0	75.0
ID @ 25C (A)	44	38
Id @ 100C (A)	31	24

- **Diode**

High-frequency rectifier diodes at the secondary side of the transformer need fast recovery, so ultra-fast recovery diodes will be applied. Normally, the maximum current through diodes is 12.8A. However, the inverse voltage across is twice that of the maximum output voltage, which is 2×156V=312V. When using an improperly designed damper, the voltage and current of diodes may be worsened by oscillation. When the driving signal of diagonal switches is fully overlapped, the inverse voltage will be even higher, which is 80V×turns-ratio×2=560V.

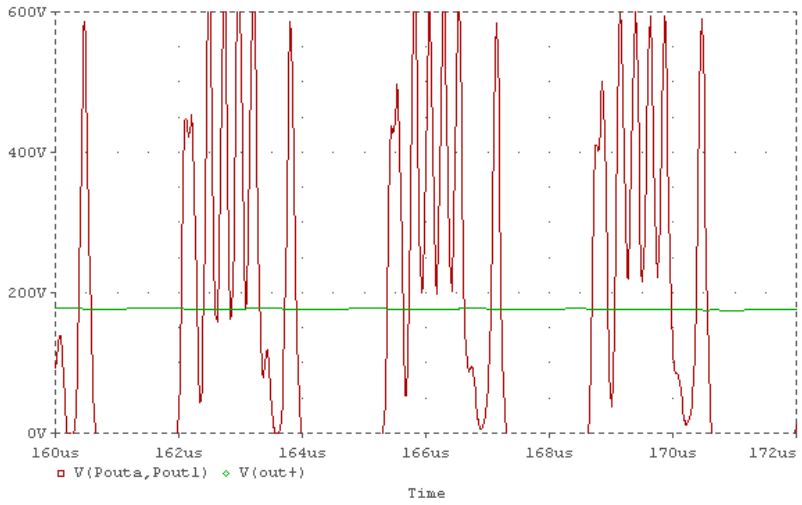


Figure 3.13: Simulation Results of Diode Current

Table 3.5: Specs of Rectifier Diodes

Model	30EPH06
t_{rr} Reverse Recovery Time (ns)	28
Package	TO-274
V_R Breakdown voltage (V)	600
V_F Forward Voltage (V)	2.0
$I_{F(AV)}$ Average Rectifier Forward Current (A)	30
C_T Junction Capacitance (pF)	33
L_S Series Inductance (nH)	3.5
I_{FSM} Non Repetitively Peak Surge Current (A)	300

At the primary side of the transformer, the clamp diodes will clamp the oscillation, but need one more commutation inductor. The breakdown voltage of these two diodes is greater than 80V, and the maximum current is less than 12.8A

Table 3.6: Specs of Clamping Diodes

Model	MUR1620CT
t_{rr} Reverse Recovery Time (ns)	25
Package	TO-220AB
V_R Breakdown voltage (V)	200
V_F Forward Voltage (V)	0.975
$I_{F(AV)}$ Average Rectifier Forward Current (A)	2×8
C_T Junction Capacitance (pF)	25
L_S Series Inductance (nH)	8
I_{FSM} Non Repetitively Peak Surge Current (A)	100

DF1 and DF2 are the bootstrap diodes, which should be a small-signal high-voltage type capable of blocking full DC bus voltage plus the VCC voltage. The recovery charge of the diode should be small so that when it recovers it will not appreciably discharge the bootstrap capacitor. Leakage current is usually not a concern, since the recovered charge of the diode will be much

more significant than the leakage current over the PWM cycle. A 1,000 volts signal diode, such as industry standard 1N5622, is preferable to a lower voltage diode, since its junction capacitance and recovered charge will be smaller. Also, a higher voltage diode will have a low reverse leakage current when operated a half of its related blocking voltage [40].

Table 3.7: Specs of Bootstrap Diodes

Model	1N5622	1N4937
Maximum repetitive peak reverse voltage (V)	1000	600
Maximum RMS voltage (V)	700	420
Maximum DC blocking voltage (V)	1000	600
Maximum average forward rectified current at TA=55ºC (A)	1.0	1.0
Maximum instantaneous forward voltage at 1.0A (V)	1.2	1.0
Maximum DC reverse current at rated DC blocking voltage TA=25ºC (μA)	0.5	1.0
Maximum reverse recovery time (μs)	2.0	0.15
Maximum junction capacitance (pF)	15	
PACKAGE	DO-204AP	Axial Lead

Other diodes will be 1N4148.

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CHAPTER FOUR: PROTOTYPING OF DC/DC CONVERTER

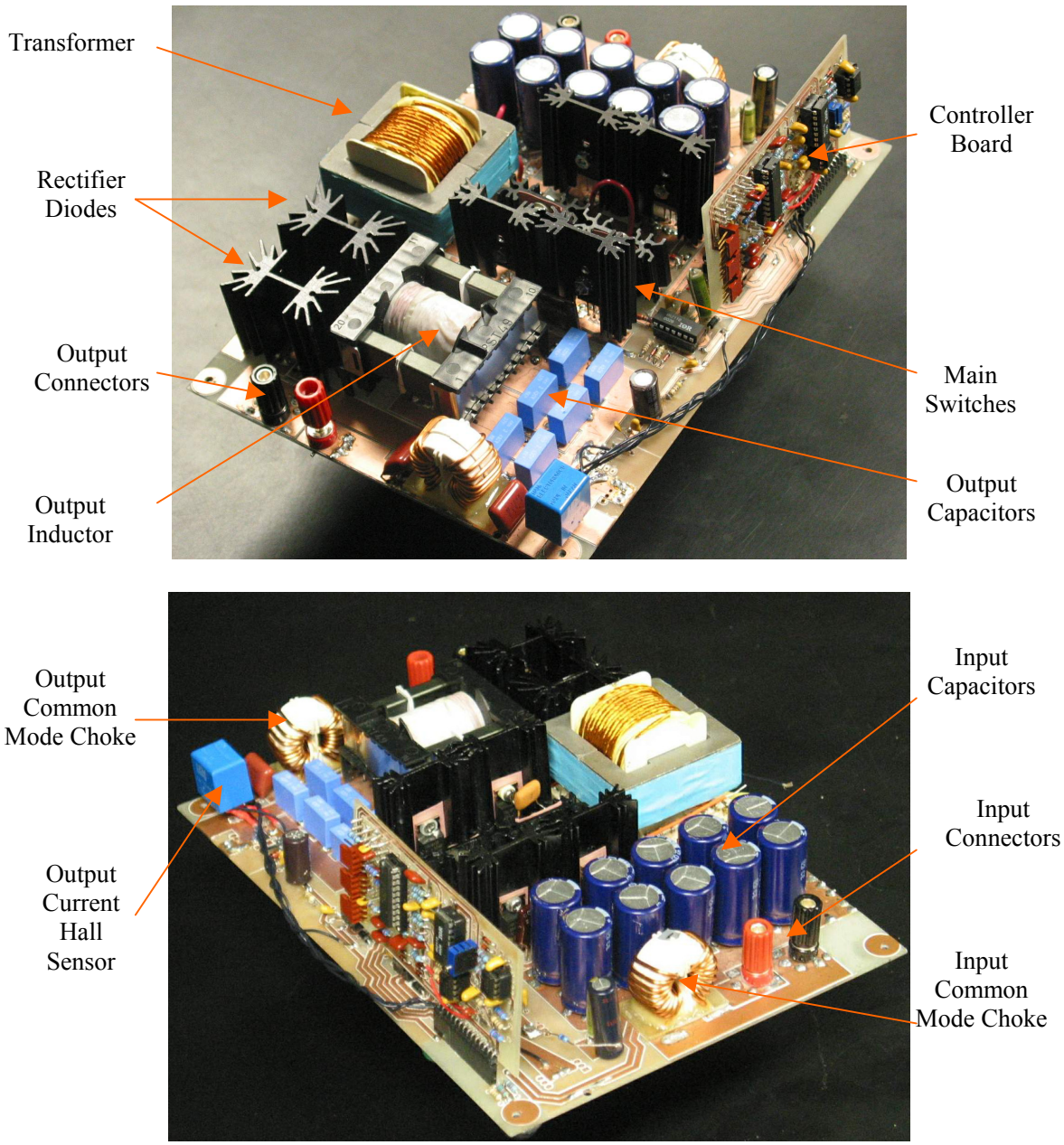
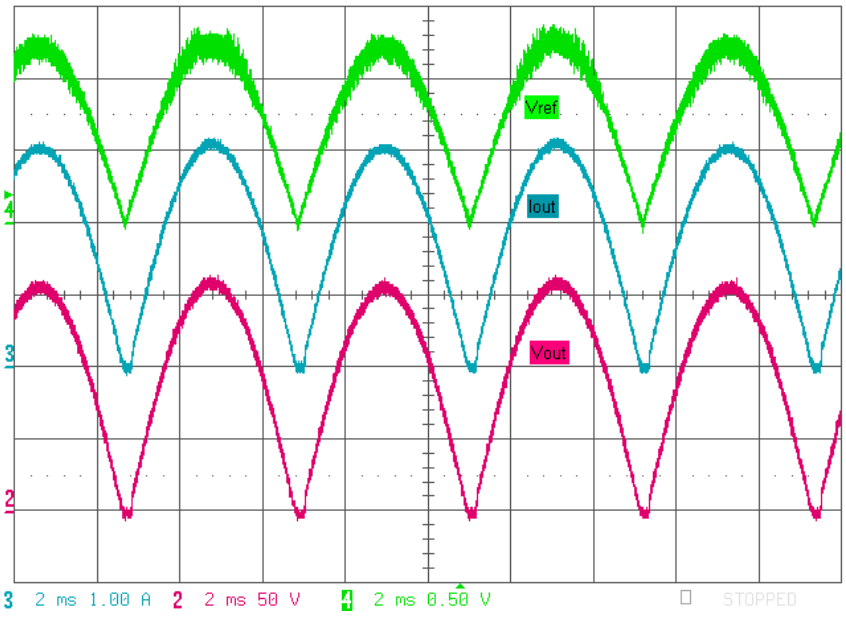


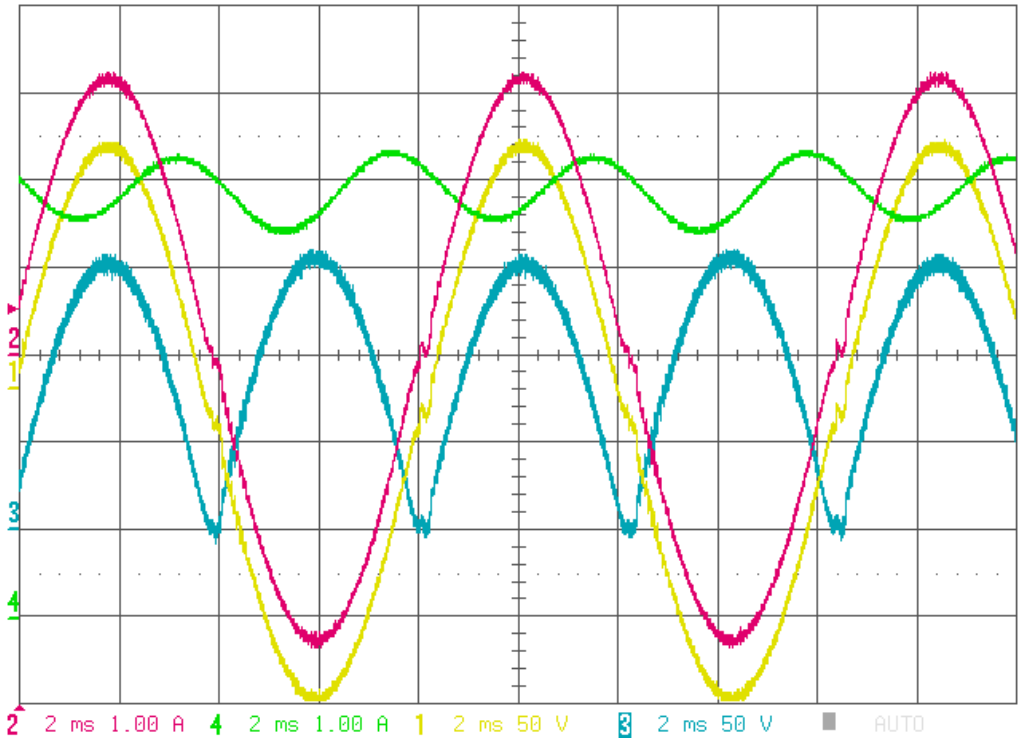
Figure 4.1: Prototype of DC/DC Converter

Figure 4.1 shows the pictures of the DC/DC converter's prototype. The prototype is made of two print circuit boards (PCB): the controller board and the power stage board. In this way, the high-voltage components and trace will be confined on the power stage board and on the low voltage components and trace on the controller board. Another benefit of this structure is that the power stage prototype need not change too much, but the controller board may change a lot. Making them into two different boards can make the optimization much easier. The drivers' circuit is on the power stage board to make sure that they are as near the MOSFETs as possible to eliminate the noise and parasitic inductance affections.

4.1 Analysis of Experimental Results



(a) V_{ref}, Output Current and Voltage



(b) Output Voltage of DC/DC(blue), Input Current(green), Inverter Output Current(red) and Inverter Output Voltage(yellow)

Figure 4.2: Experimental Results

As Figure 4.2 shows, the output current reference signal is generated by the absolution circuit from a sinusoid signal, which is generated by a function generator. The load is a 52Ω resistor. The r.m.s. value of output voltage and current is 110V and 2.2A.

Figure 4.2 also shows, the output current follows the reference strictly. After the properly designed output filter, the output current has very little noise and distortion. The next stage will be an unfolding circuit, which will invert this rectified sinusoid current and voltage into sinusoid.

With this kind of rectified current, the output of the inverter can achieve very high power factor and power quantity [45, 46].

The peak value of output voltage and current is 160V and 3.1A. The peak output power is 450Watts, which is limited by the power rating of the single channel solar array simulator. Zero crossing is still a small problem. A very small DC offset, such as 50mV, can solve it.

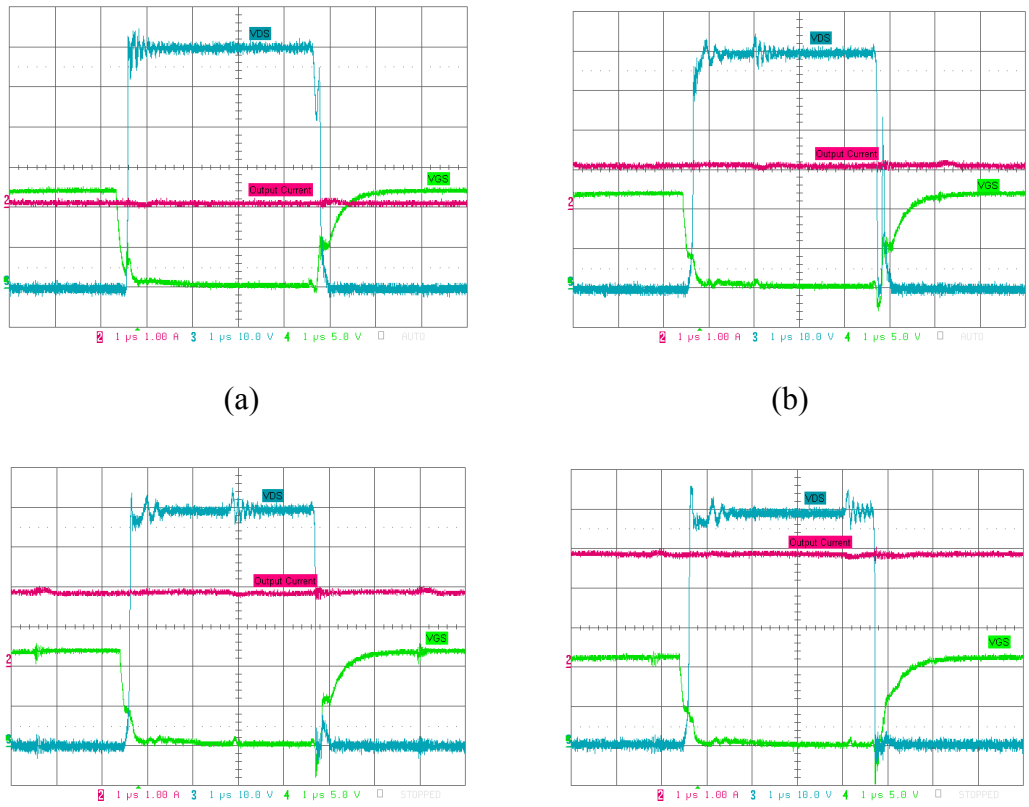
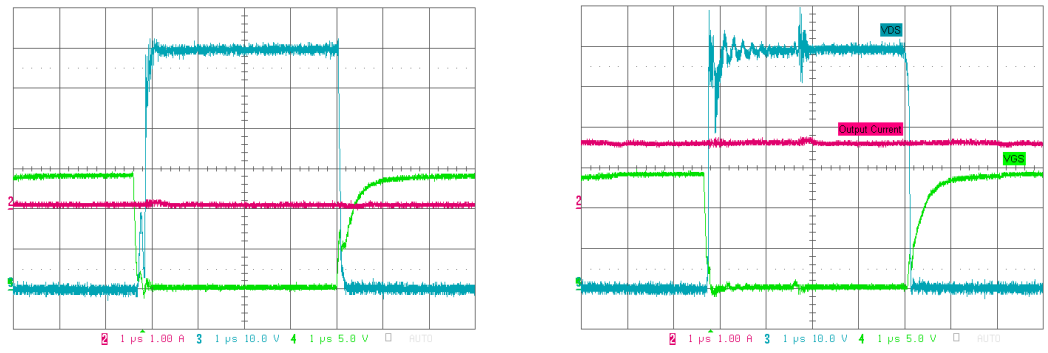


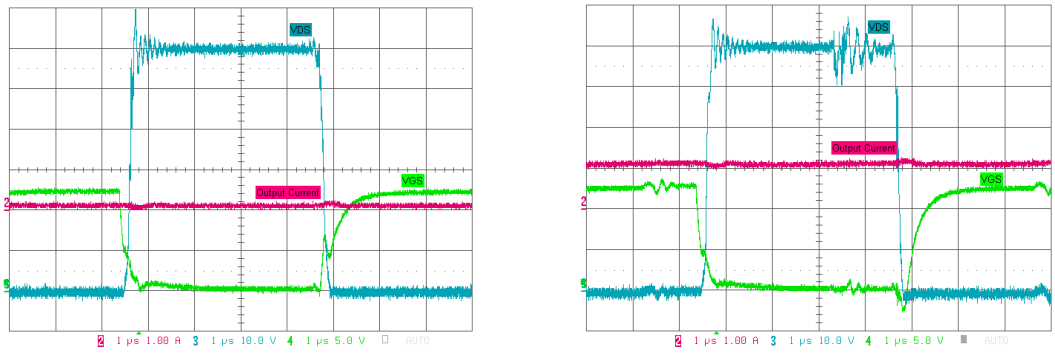
Figure 4.3: Experimental Results of Output Current, V_{DS} and V_{GS} of Switch A



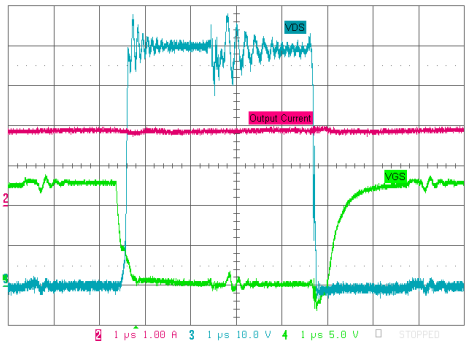
(a) (b)

(c) (d)

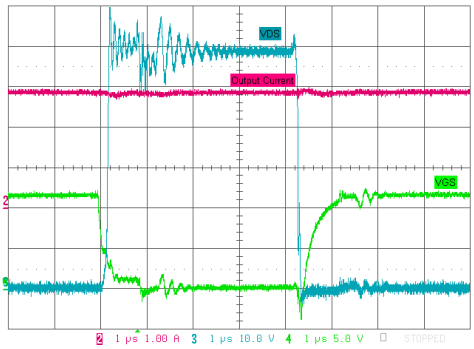
Figure 4.4: Experimental Results of Output Current, V_{DS} and V_{GS} of Switch B



(a) (b)

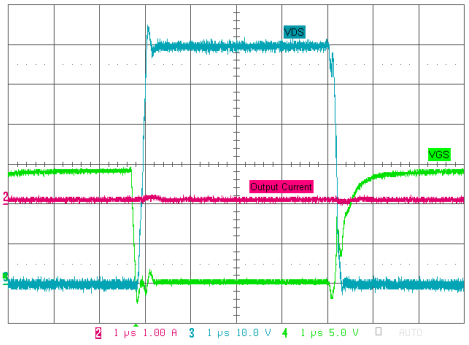


(c)

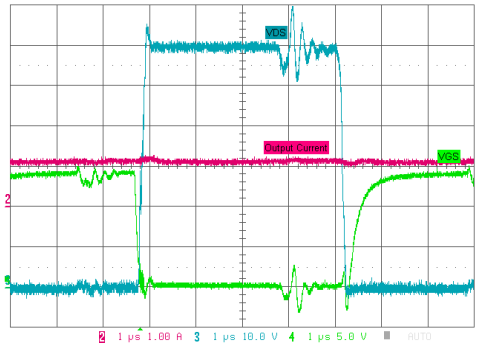


(d)

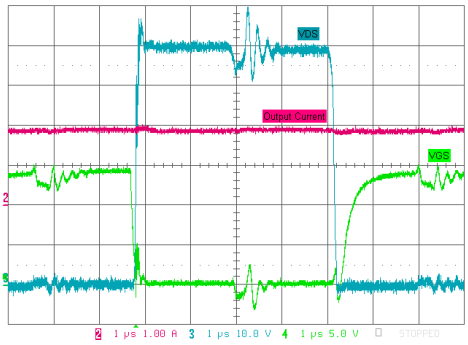
Figure 4.5: Experimental Results of Output Current, V_{DS} and V_{GS} of Switch C



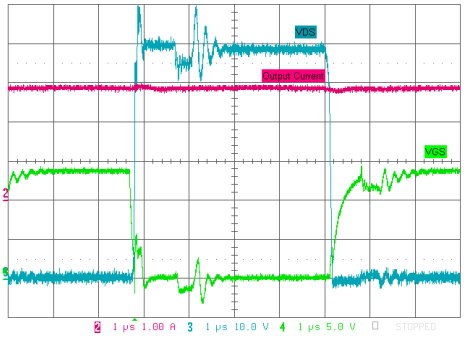
(a)



(b)



(c)

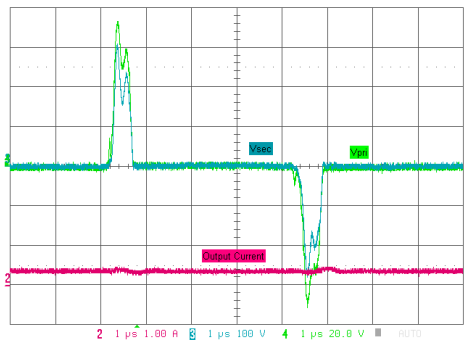


(d)

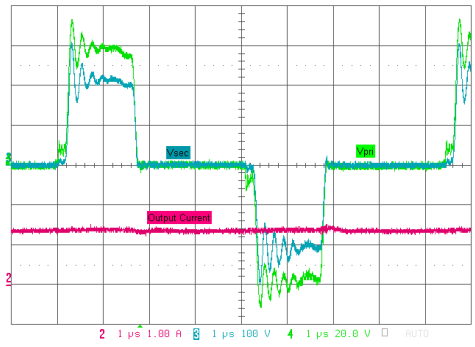
Figure 4.6: Experimental Results of Output Current, V_{DS} and V_{GS} of Switch D

To examine the switching process of the full bridge at steady state, the reference of the DC/DC converter was changed from rectified sinusoid to pure DC, then the DC/DC converter output to pure DC voltage. Figure 4.3, Figure 4.4, Figure 4.5 and Figure 4.6 show the output current, V_{DS} and V_{GS} of switches A, B, C and D. The load is 52Ω resistor and the output current of these figure are 0.1A, 1.1A 1.8A and 2.9A, so these figures show the load of 0.5Watt, 62Watts, 182Watts and 440Watts. At light load, all the switches are turned on under "hard switching." As the load increases, all the switches are turned on under "soft switching," which is zero voltage switching. That is to say, before the V_{GS} goes to high, V_{DS} already goes to zero.

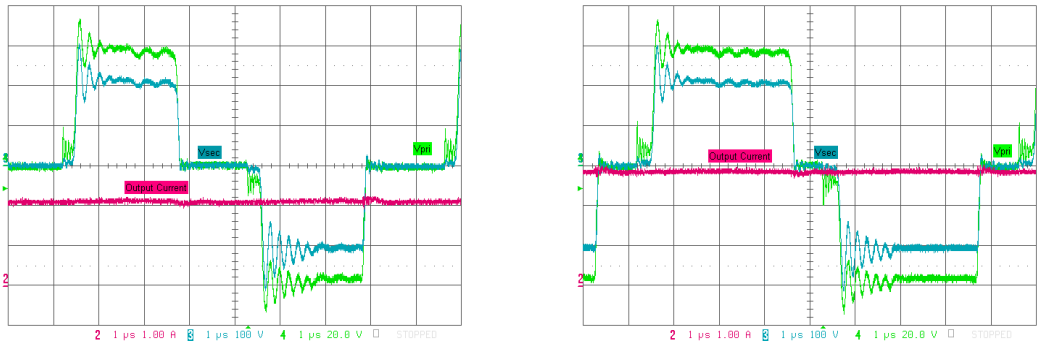
The transition time or the dead time was set to be 200ns as a constant. Therefore, at light load, the dead time is so long that V_{DS} goes back in Figure 4.3(b), and so short at high load that V_{DS} has not fully reached zero in Figure 4.5(d) and Figure 4.6(d). To solve this problem, a more adaptive delay time will be applied.



(a)



(b)



(b) (c)

Figure 4.7: Experimental Results of Output Current, Transformer Primary and Secondary-Side Voltage

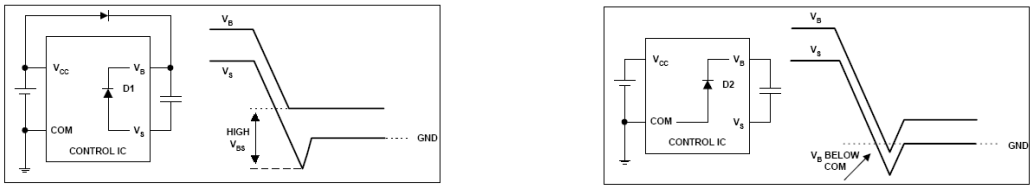
Figure 4.7 shows the voltage of primary side and secondary side of the transformer with the increasing of output current. Without any snubbers on the secondary side and with an improper choice of clamping diodes on the primary side, the ringing is still a problem. To conquer it, a fast recovery schottky diode will be applied. A resistor and capacitor in series can damp the ringing further. The experiment's results show that this method will cause extra power loss and thermal problems.

The small steps on the primary side of the transformer are caused by leakage inductance of the transformer. The leakage inductance will store energy during the conduction mode. During the freewheeling mode, the stored energy will help to oscillate the voltage of the other diagonal switches' voltage to zero and facilitated the ZVS [41, 42].

Due to the optimized transformer and zero voltage switching, the overall efficiency is greater than 93 percent at 480Watts.

4.2 Trouble Shooting

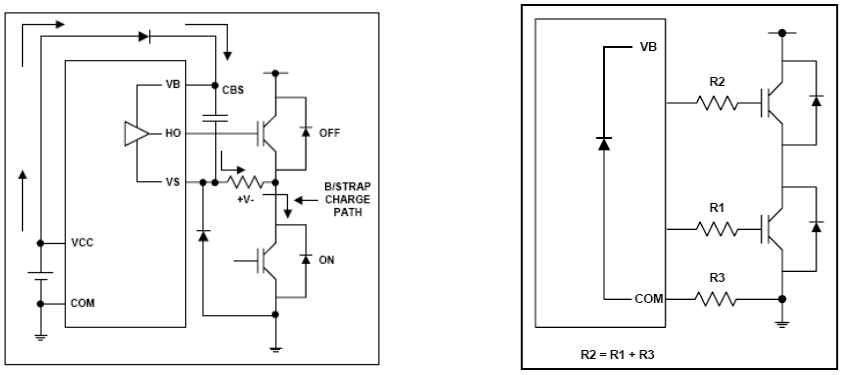
During the experiments, the high side of Driver IC IR2110 is latched up when the load increases. Due to the stay inductance on the trace between the high side and low side of MOSFET, V_S will undershoot less than zero as shown in Figure 4.8(a). When $V_{BS,\,MAX}$>25V, then the diode D_1 inside the driver will be latched up or even broken down. If V_B undershoots to a negative value, then diode D_2 will conduct, as shown in Figure 4.8(b). Without any resistor in series, D_2 will latch up or breakdown soon [47].



(a) Ideal Bootstrap Circuit (b) Practical Bootstrap Circuit with Floating Supply

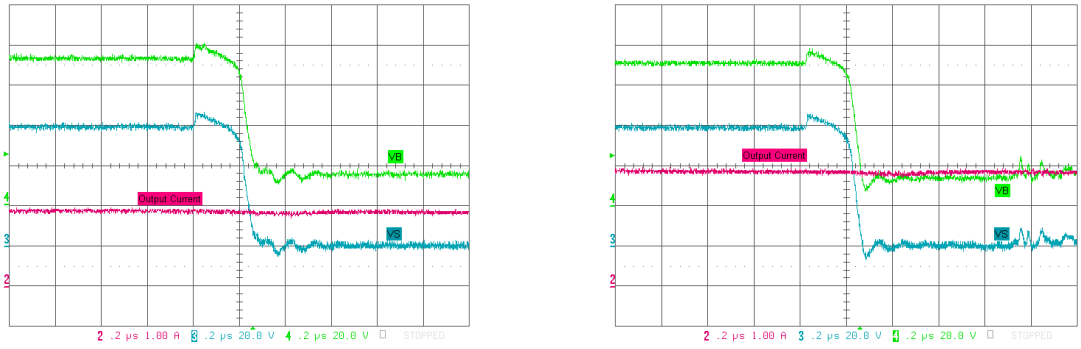
Figure 4.8: Ring Effect of V_B and V_S on Driver IC IR2110 [47]

To damp the ringing of V_S and V_B, two methods were applied as shown in Figure 4.9. Experiment results show that the undershoot is damped, shown in Figure 4.10.



(a) (b)

Figure 4.9: Two Methods of Vs Undershoot Immunity [47]



(a) (b)

Figure 4.10: Experimental Results of Output Current, V_B and V_S

The undershoot of V_B and V_S will be exaggerated as the load increases, which is shown in Figure 4.10. The undershoot of V_B does not reach zero, and V_{BS} is constant as 17V<25V, with enough margin. To make the system stable at even the higher load, the undershoot of V_B and V_S should be confined strictly.

CHAPTER FIVE: CONCLUSION

5.1 Summary

A new control approach for a solar-based inverter that tracks the maximum available power and produces a near unity power factor is presented. It is shown that the new approach produces excellent signal-to-noise ratio for the feedback signals, ensuring reliable and robust maximum power tracking while tightly regulating the sinusoidal waveform of AC current supplied to the utility grid with almost unity power factor. Employing a feed-forward compensation technique coupled with one stage of DC/DC power conversion, the proposed inverter system is simplified when compared to conventional inverter deigns.

Average mode simulation results clearly show that the overall system is stable under solar array and utility grid changes. Switching mode simulation results show that ZVT is possible only when enough energy is stored in the commutation inductor. A trade-off is needed to widen the ZVT range of each cycle and reduce the turn's ratio of the transformer. Clamping diodes on the primary side will reduce the ringing on the transformer caused by the parasitic parameter of switches and leakage inductance of the transformer. Properly choosing the value of output filter can minimize the zero-crossing distortion of the output current.

A prototype of DC/DC converter applies UCC3895 full-bridge phase-shift controller. A detailed design procedure of controller, transformer, inductor and driving circuits is given. All of the key components are properly identified and selected.

Experimental results of the DC/DC converter show that ZVT of all the bridge switches and the rectified sinusoid current of DC/DC converter and sinusoid output current of the inverter.

Clamping diodes reduce the ring and overshoot of the transformer voltage. Due to the stray inductance, the driving circuit may fail. Properly damping the ringing on the driving circuit is needed.

5.2 Future Work

Future work will focus on the control loop design and analysis for a robust system stability that specifically deals with the non-linearity of the array source and the resonant behavior of the line-filter. A more complicated controller will be designed, including feed-forward compensation, a DSP-based MPT controller and protection modules. The final design of the inverter will be modularized, which will make the inverter easily connected in series and parallel.

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