STUDY OF OXIDE BREAKDOWN, HOT CARRIER AND NBTI EFFECTS ON MOS DEVICE AND CIRCUIT RELIABILITY

by

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ABSTRACT

As CMOS device sizes shrink, the channel electric field becomes higher and the hot carrier (HC) effect becomes more significant. When the oxide is scaled down to less than 3 nm, gate oxide breakdown (BD) often takes place. As a result, oxide trapping and interface generation cause long term performance drift and related reliability problems in devices and circuits.

The RF front-end circuits include low noise amplifier (LNA), local oscillator (LO) and mixer. It is desirable for a LNA to achieve high gain with low noise figure, a LO to generate low noise signal with sufficient output power, wide tuning range, and high stability, and a mixer to up-convert or down-convert the signal with good linearity. However, the RF front-end circuit performance is very sensitive to the variation of device parameters. The experimental results show that device performance is degraded significantly subject to HC stress and BD. Therefore, RF front-end performance is degraded by HC and BD effects.

With scaling and increasing chip power dissipation, operating temperatures for device have also been increasing. Another reliability concern, which is the negative bias temperature instability (NBTI) caused by the interface traps under high temperature and negative gate voltage bias, arises when the operation temperature of devices increases. NBTI has received much attention in recent year and it is found that N_{IT} is present for all stress conditions and N_{OT} is found to occur at high V_G. Therefore, the probability of BD in pMOSFET increases with temperature since trapped charges during the NBTI process increase, thus resulting in percolation, a main cause of oxide degradation. The above effects can cause significant degradations in transistors, thus leading to the shifts of RF performance.

This dissertation focuses on the following aspects:

(1) RF performance degradation in nMOSFET and pMOSFET due to hot carrier and soft breakdown effects are examined experimentally and will be used for circuit application in the future.

(2) A modeling method to analyze the gate oxide breakdown effects on RF nMOSFET has been proposed. The device performance drifts due to gate oxide breakdown are examined, breakdown spot resistance and total gate capacitance are extracted before and after stress for 0.16 um CMOS technology.

(3) LC voltage controlled oscillator (VCO) performance degradation due to gate oxide breakdown effect is evaluated.

(4) NBTI, HCI and BD combined effects on RF performance degradation are investigated. A physical picture illustrating the NBTI induced BD process is presented. A model to evaluate the time-to-failure (TTF) during NBTI is developed. DCIV method is used to extract the densities of N_{IT} and N_{OT}. Measurements show that there is direct correlation between the steplike increase in the gate current and the oxide-trapped charge (N_{OT}). However, Breakdown has nothing to do with interface traps (N_{IT}).

(5) It is found that the degradation due to NSH stress is more severe than that of NS stress at high temperature. A model aiming to evaluate the stress-induced degradation is also developed.

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CHAPTER ONE: INTRODUCTION

1.1 Motivation

With the continued progress in wireless communications in recent years, it is desirable to integrate the RF front-end with the baseband building blocks of communication circuits into a single chip. As CMOS technology advances, CMOS is becoming attractive for system-on-a-chip (SOC) implementation.

Due to continued scaling, deep sub-micrometer CMOS transistors can produce a cutoff frequency (f_T) over 150 GHz and a noise figure (NF) lower than 0.5 dB [1]. This not only promises gigabit integration, gigahertz clock rate, and system on a chip, but also arouses great expectations for CMOS RF circuits at 1-5 GHz, where the dominant technologies are currently silicon bipolar and GaAs.

On the other hand, when the oxide is scaled down to less than 3 nm, hot carrier (HCI) stress and soft breakdown (SBD) induced device degradation often take place[2]-[4], and they pose a limit to the device scaling. These two problems are related to the continuous increase of the electrical fields in both oxide and silicon. The latter is due to the fact that, under the influence of the high lateral fields in short-channel MOSFETs, electrons and holes in the channel and pinch off regions of the transistor can gain sufficient energy to surmount or tunnel through the energy barrier between the silicon and the oxide. This leads to the injection of a gate current into the oxide, which will cause changes in transconductance, threshold voltage, and drive currents of the MOSFET. The increased random thermal motion of carriers in the channel after hot carrier stress increases the channel noise, a critical factor in the low noise amplifier design. Moreover, long

time stress may lead to the increase of gate leakage current and the decrease of breakdown resistance and total gate capacitance, which will result in some circuit failures.

With scaling and increasing chip power dissipation, operating temperatures for device have also been increasing. Another reliability concern, which is the negative bias temperature instability (NBTI) caused by the interface traps and fixed charge under high temperature and negative gate voltage bias, arises when the operation temperature of devices increases. NBTI has received much attention in recent year and it is found that N_{IT} is present for all stress conditions and N_{OT} is found to occur at high V_G [55] . Therefore, the probability of BD in pMOSFET increases with temperature since trapped charges during the NBTI process increase, thus resulting in percolation, a main cause of oxide degradation [56]. The above effects can cause significant degradations in transistors, thus leading to the shifts of RF performance.

Moreover, the scaling down of the devices is in return accompanied with small dimension effects. New physical mechanisms need to be taken into account. Even though the severe gate leakage in an ultra-thin gate oxide does not cause problems for an individual MOSFET, the leakage current is still a big problem to the entire chip for the battery operation. Anyway, other advantages of ultra-thin gated and short channel MOSFETs, such as large drive current and large transconductance due to the scaling-down of the gate area and better oxide breakdown characteristic due to the direct tunneling nature [6], make them still a good choice.

1.2 Goals of this Research

As discussed above, the performance drifts due to soft breakdown, hot carrier stress and

NBTI could be examined by the main transistor parameter drifts, including transconductance degradation, threshold voltage and mobility shift. My research focuses on these issues and tries to solve problems as bellows:

(1) RF performance degradation in nMOSFET and pMOSFET due to hot carrier and soft breakdown effects.

(2) Modeling method to analyze the gate oxide breakdown effect on RF nMOSFET.

(3) LC voltage controlled oscillator (VCO) degradation due to gate oxide breakdown effect.

(4) The NBTI along with BD and HCI effects on RF performance.

1.3 Dissertation Outline

First of all, hot-carrier (HC), soft-breakdown (SBD) and negative bias temperature instability (NBTI) effects will be reviewed in Chapter 2. Mechanisms of the above phenomena are discussed.

In Chapter 3, the experimental phenomena for HC and SBD effects on CMOS transistors are shown.

The modeling method used to study SBD will be introduced in Chapter 4. This modeling method focuses on an improved f_T model equation and a physics-based small-signal equivalent circuit of the nMOS transistor after breakdown. The modeling method used for SBD can be extended to the analysis of degradation in pMOSFET due to HC and SBD effects. LC voltage controlled oscillator (VCO) degradation due to soft breakdown effect is then discussed in Chapter 5.

In Chapter 6, the discussion of the NSH and NS effects is given. The NBTI along with BD and HCI effects on RF performance are shown.

The conclusion and future work are discussed in Chapter 7.

CHAPTER TWO: FUNDAMENTALS OF RELIABILITY ISSUES

2.1 Introduction

When continuously downscaling device geometry into deep sub-micron range, a cut-off frequency (f_T) of CMOS transistor as high as 150 GHz has been reported [1]. Therefore, RF-CMOS is expected to replace the silicon bipolar transistors and GaAs MESFET's in RF front-end IC's for mobile telecommunication devices in the near future. RF-CMOS is very attractive compared to the silicon bipolar transistor and GaAs MESFET's due to its lower manufacturing costs, lower power consumption and high integratability. However, hot carrier (HC) stress and soft breakdown (SBD) induced device degradation pose a limit to the device scaling. Moreover, transistor aging and SBD induced degradation will seriously reduce the design margin of the RF circuits. It is important to understand the impact of stress on the RF circuit performance using deep sub-micron processes.

Hot-carrier effect and gate oxide breakdown are the two critical issues of deep sub-micron CMOS device and circuit reliability [31]. These two problems are related to the continuous increase of the electrical fields in both oxide and silicon. The latter is due to the fact that, under the influence of the high lateral fields in short-channel MOSFETs, electrons and holes in the channel and pinch off regions of the transistor can gain sufficient energy to surmount or tunnel through the energy barrier between the silicon and the oxide. This leads to the injection of a gate current into the oxide, which will cause changes in transconductance, threshold voltage, and drive currents of the MOSFET. The increased random thermal motion of carriers in the channel after hot carrier stress increases the channel noise, a critical factor in the low noise amplifier

design. Compared with hard breakdown, soft breakdown becomes more prevalent for thinner oxides and for oxide stress at relatively lower voltages [20]. Moreover, hot carrier injection triggers more soft breakdowns in addition to conventional FN injection [32].

Besides, another reliability concern, which is the negative bias temperature instability (NBTI) caused by the interface traps and fixed charge under high temperature and negative gate voltage bias, arises when the operation temperature of devices increases. The above effects can cause significant degradations in transistors, thus leading to the shifts of RF performance.

In this chapter, physical mechanism of hot-carrier, soft breakdown and negative bias temperature instability will be reviewed.

2.2 Soft Breakdown of Ultra-Thin Gate Oxide

Gate oxide breakdown has been one of the central topics of CMOS reliability. When the oxide is scaled down to thinner than 5 nm, it experiences two types of breakdown, soft (SBD) and hard (HBD). SBD may take place more often than HBD. Extensive studies on the breakdown mechanisms have been conducted in association with the studies on defect generation, such as anode hole injection, hydrogen release, and so forth, yet there being many controversies. Two lifetime prediction models (E and 1/E) seem to be able unified with more assumptions. Figure 2.1 shows the SBD and HBD modes for ultra-thin gate oxide MOSFETs.

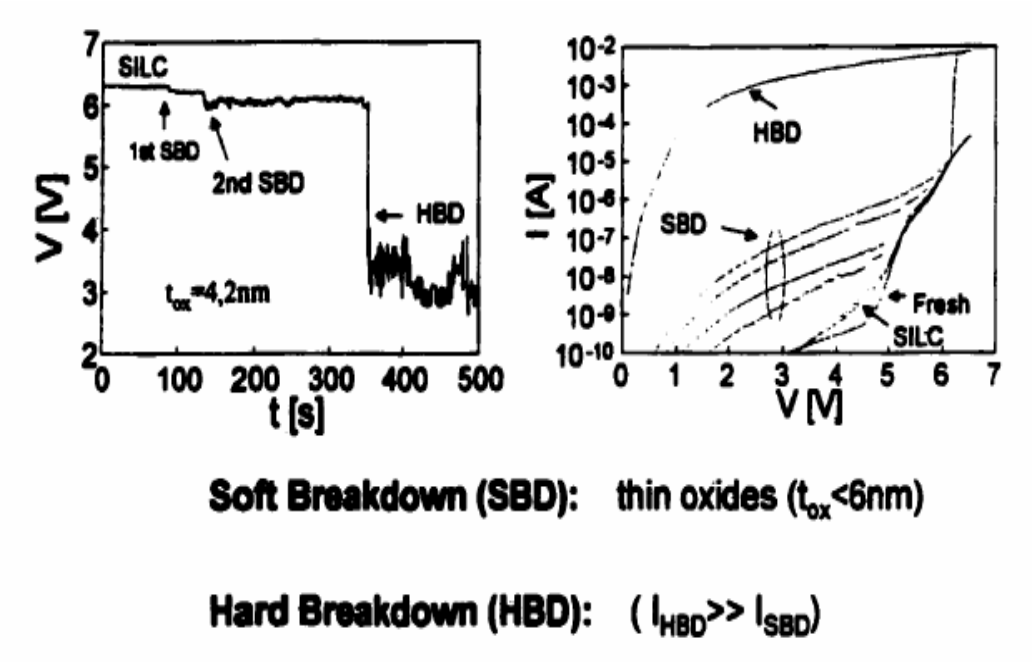


Fig. 2.1 SBD and HBD

From Figure 2.1, there are some similarities and differences between SBD and HBD. They are all caused by defect generation and are triggered by the same type of defect paths, but the post-breakdown I-V characteristics are very different, including the current level and shape of I-V. HBD always cause device failure, but SBD can be sometimes tolerated.

Another radical concern is the breakdown influence on transistor performance. Like the significant performance degradation by HBD, SBD also affects the performance of deep submicron CMOS. Accelerated stresses under real operation biasing mode at both gate and drain terminals has been done to show how SBD degrade devices. This work is important for better understanding the new reliability issues arising from the ultra-thin gate oxide.

The occurrence of soft breakdown is identified by the telegram noise signal. It begins with an abrupt oxide conductance change that is orders of magnitude smaller than that associated with HBD and repeats it somehow later on. It is sometimes called quasi-breakdown. Initially, SBD

was defined as an oxide breakdown without the lateral propagation of the breakdown spot due to thermal damage [7]. Two main features of this breakdown mode are:

(1) A huge leakage current in the direct tunneling voltage range, that shares some major aspects with the HBD mode;

(2) A significant increase of the noise level, sometimes in the form of large multilevel current or voltage fluctuations. It is shown in Figure 2.2.

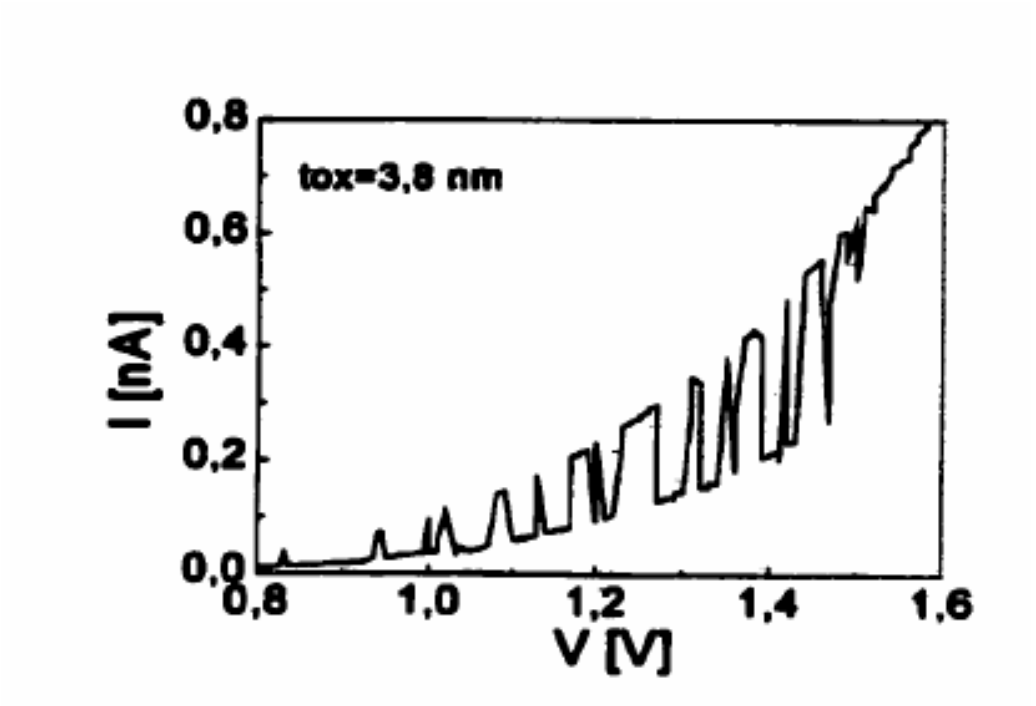


Fig. 2.2 Fluctuations in the SBD

It is widely accepted that the oxide SBD is caused by the formation of some low resistance paths in the oxide and that these paths are related to the defects generated during electrical stress. It is unclear though what kind of microscopic structure develops within the oxide at the SBD

spots and therefore, which theoretical model is suitable to solve the conduction problem. Several models have been proposed and they are mainly based on tunneling, hopping, and percolation mechanism, respectively.

Another question is that if SBD and HBD of ultra-thin gate oxides are really different failure mechanisms. They do have a common physical origin by means of a statistical analysis. Being triggerd by identical microscopic defects, these breakdown modes can be actually considered to be the same mechanism. In particular, it is shown that the SBD conduction path is not the precursor of the final HBD event, which generally appears at a different spatial location. The huge distinction between the soft and hard post breakdown I-V characteristics is attributed to differences in the breakdown spot area and to point conduct energy tunneling effects. For SBD, the very narrow spot constriction does not allow conducting modes of HBD and the current is due to tunneling through an area controlled energy barrier.

In the early studies, ultra-thin gate oxides experiencing SBD was not revealed to fail. It was shown that for large area devices the gate current and substrate current as a function of the gate voltage after SBD are stable and unique curves; only for the smaller devices both currents become unstable. People explained this difference with the different energy available for discharging in the SBD path. It is also shown that the SBD detection strongly depends on the test structures. In a recent study, the only noticeable signature of SBD was found to be an increase in the off current due to enhanced gate-induced drain leakage (GIDL). We believe that the reason all these studies did not observe the appreciable device degradation after SBD is because too big/thick oxides or unsuitable biasing-condition/test-structures were used.

2.3 Physical Mechanisms of hot carrier injection

Hot carrier effects in silicon VLSI circuits represent phenomena that are brought about by high-energy carriers created by the channel electric field. Because the device size is shrinking, the channel electric filed becomes higher and higher. The carriers in the channel gain enough energy and become “hot”. Main interest has focused on channel hot-electron (CHE) injection.

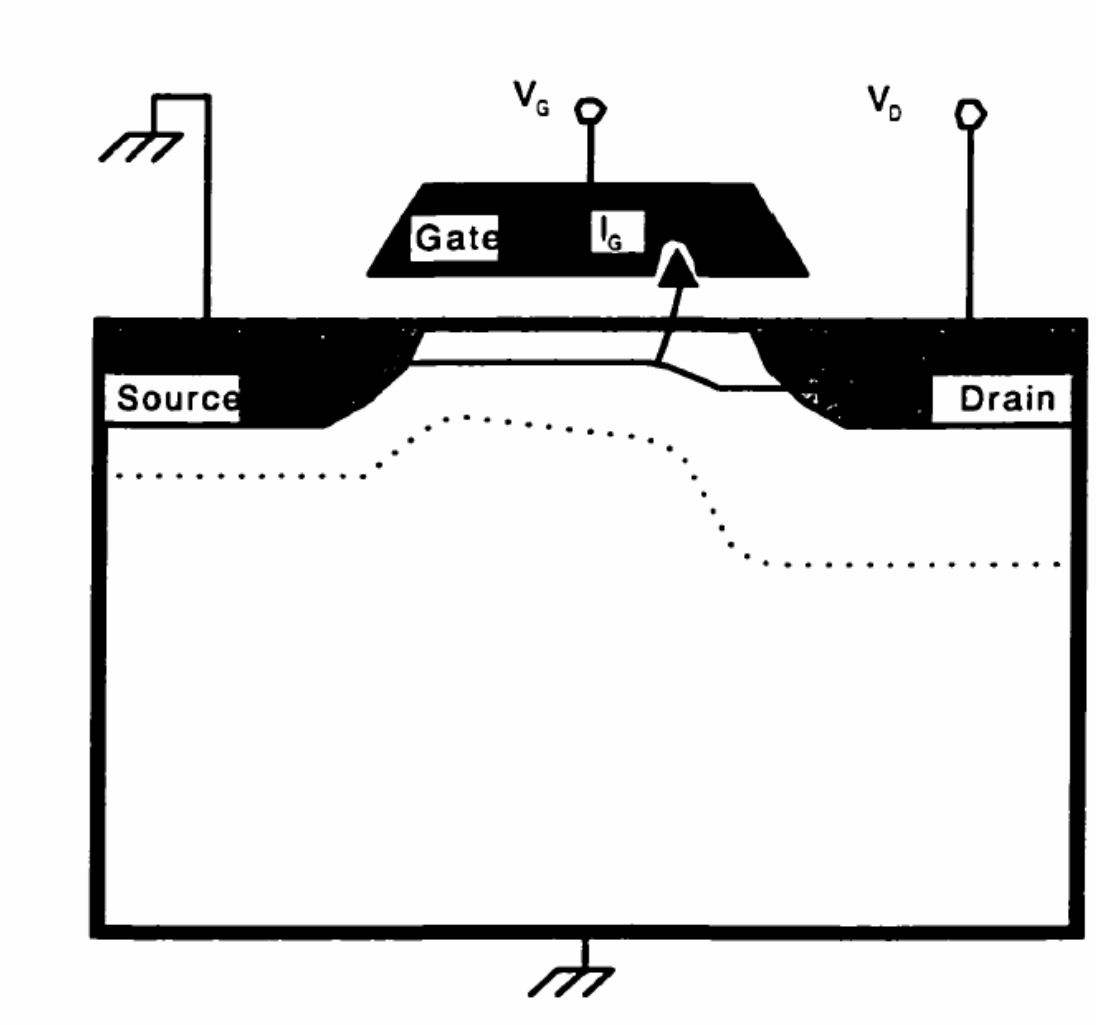


Fig. 2.3 Schematic diagram of channel hot-electron (CHE) injection

However, there are several injection mechanisms that account for the causes of VLSI circuit

degradation besides CHE injection. Each injection mechanism is discussed and clarified below by comparing with that due to CHE injection:

(1)Channel hot-electron (CHE) injection [33], [34]: as shown in Fig. 2.3, some "lucky" electrons from the channel can escape by obtaining sufficient energy to surmount the Si-SiO_2 barrier without suffering any energy-losing collision. These electrons are called "channel hot electrons", forming the main part of gate current. These electrons also cause a significant degradation of the oxide and the Si-SiO_2 interface, especially at low temperature.

(2)Drain avalanche hot-carrier (DAHC) injection: as shown in Fig. 2.4, if V_D is large, reduction of V_G intensifies the electric field at the drain to the point where avalanche multiplication due to impact ionization may substantially increase the supply of both hot electrons and hot holes. They are injected into the gate in the same way as CHE, which gives rise to the most severe degradation around room temperature.

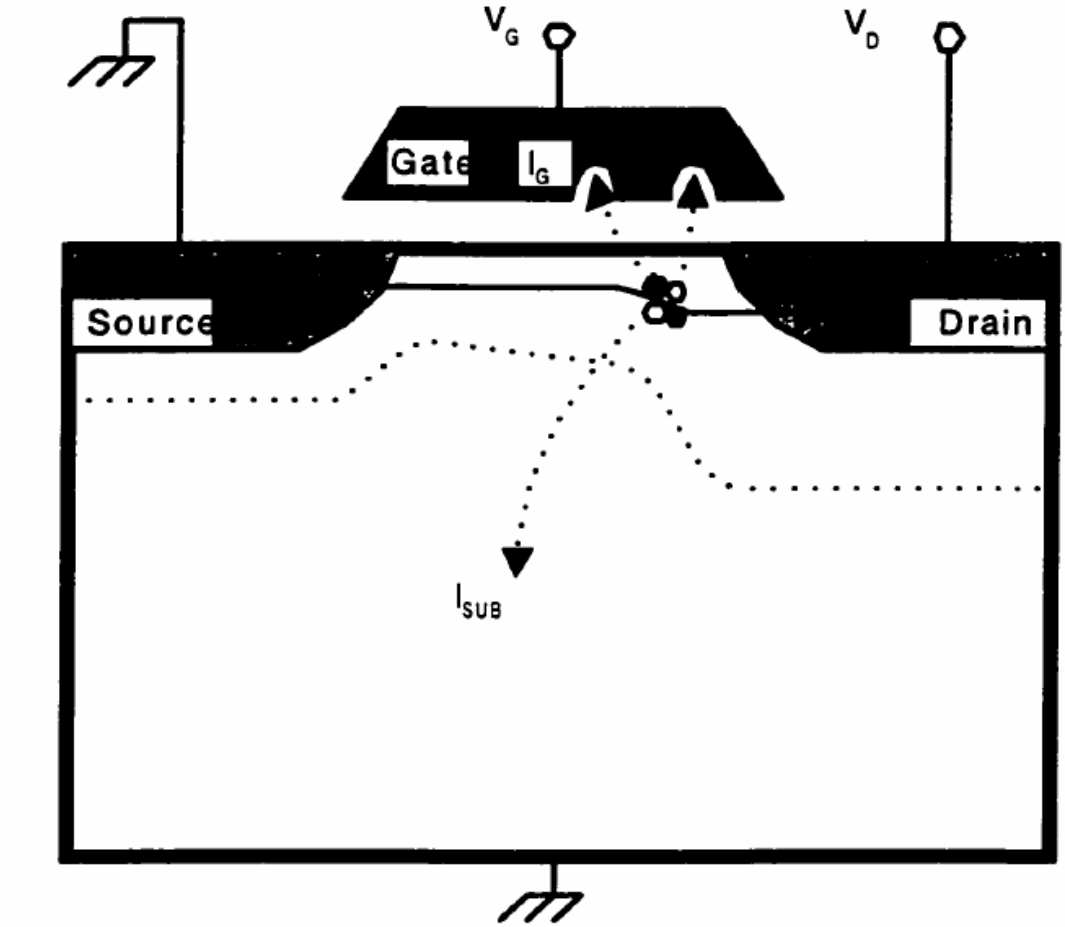


Fig. 2.4 Drain avalanche hot-carrier injection mechanism

(3) Secondary generated hot-electron (SGHE) injection: as shown in Fig. 2.5, when the electric field is very high, the generated hot carriers are able to cause secondary impact ionization in the depletion region during its journey to the substrate. The electrons generated due to secondary impact ionization can also be injected into the gate and cause degradation. It only becomes a problem in ultra-small devices.

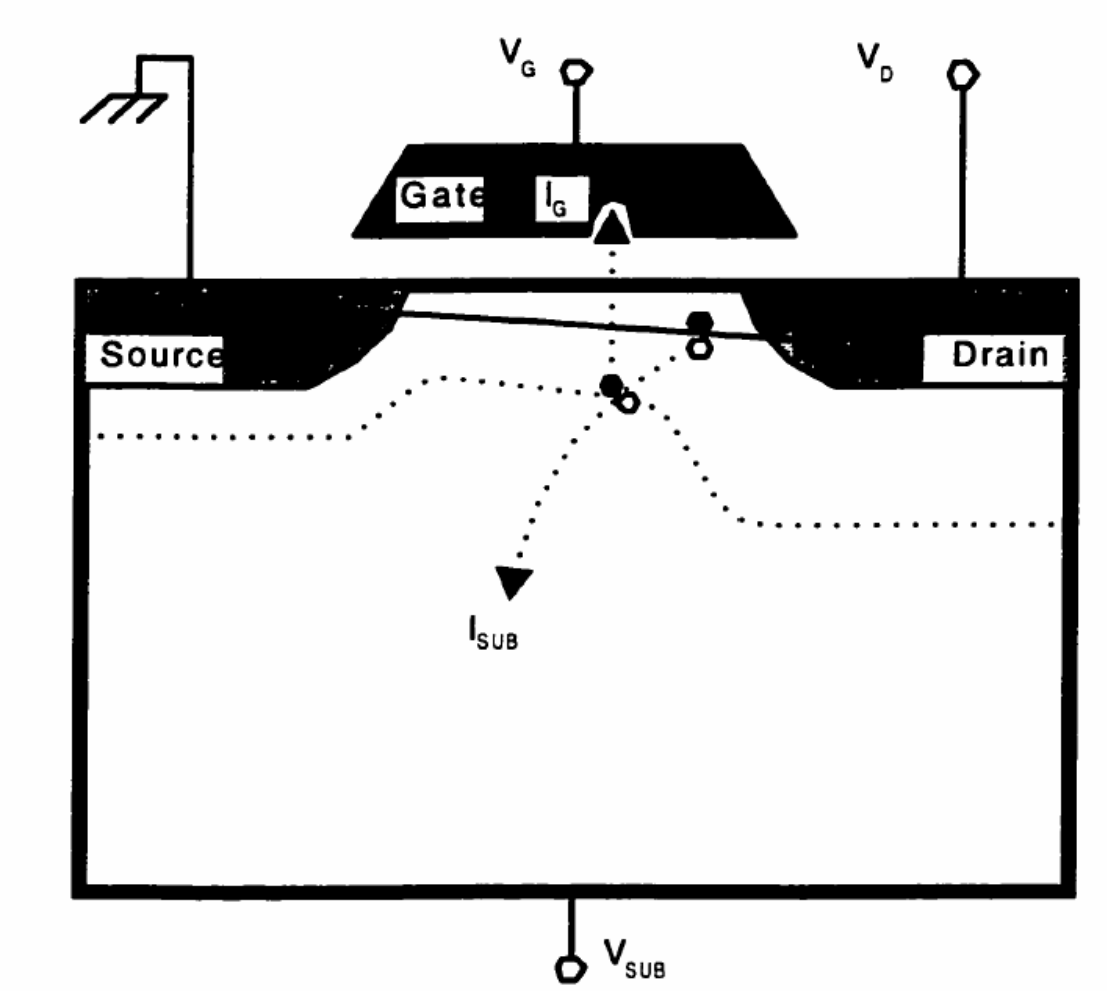


Fig. 2.5 Substrate current induced hot-electron injection mechanism

(4) Substrate hot-electron (SHE) injection: as shown in Fig. 2.6, hot carrier injection is one-dimensional. Thus analysis of electron and hole trapping in SiO_2 is simpler than that of drain avalanche injection. Hot carriers are thermally and/or radiatively generated or injected from the forward-biased p-n junction into the substrate high-field region to investigate gate insulator

qualities (Fig. 2.7a).

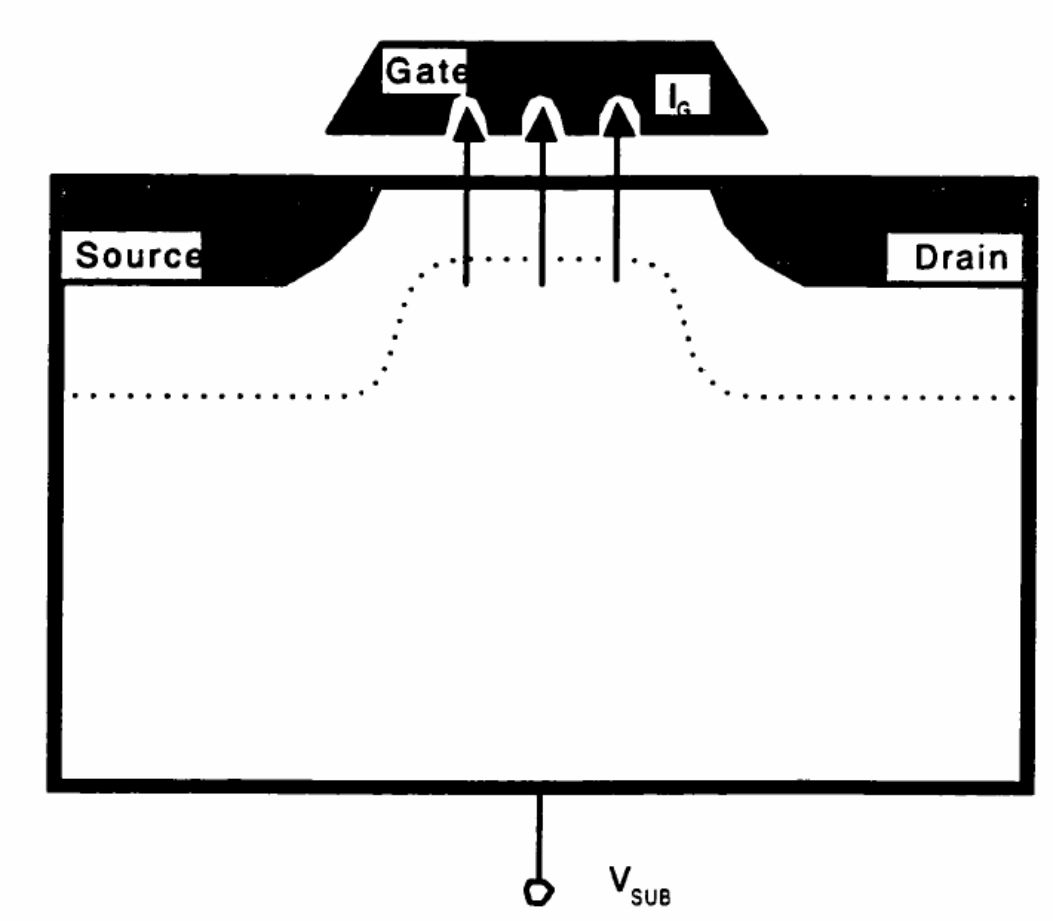


Fig. 2.6 Schematic diagram of substrate hot-electron (SHE) injection

(5)Fowler-Nordheim (F-N) tunneling injection: hot electrons are injected from the channel inversion layer into the high-field gate dielectrics (Fig. 2.7b). This injection mechanism is used in EEPROM devices and also is a significant cause of dielectric breakdown in thin insulators.

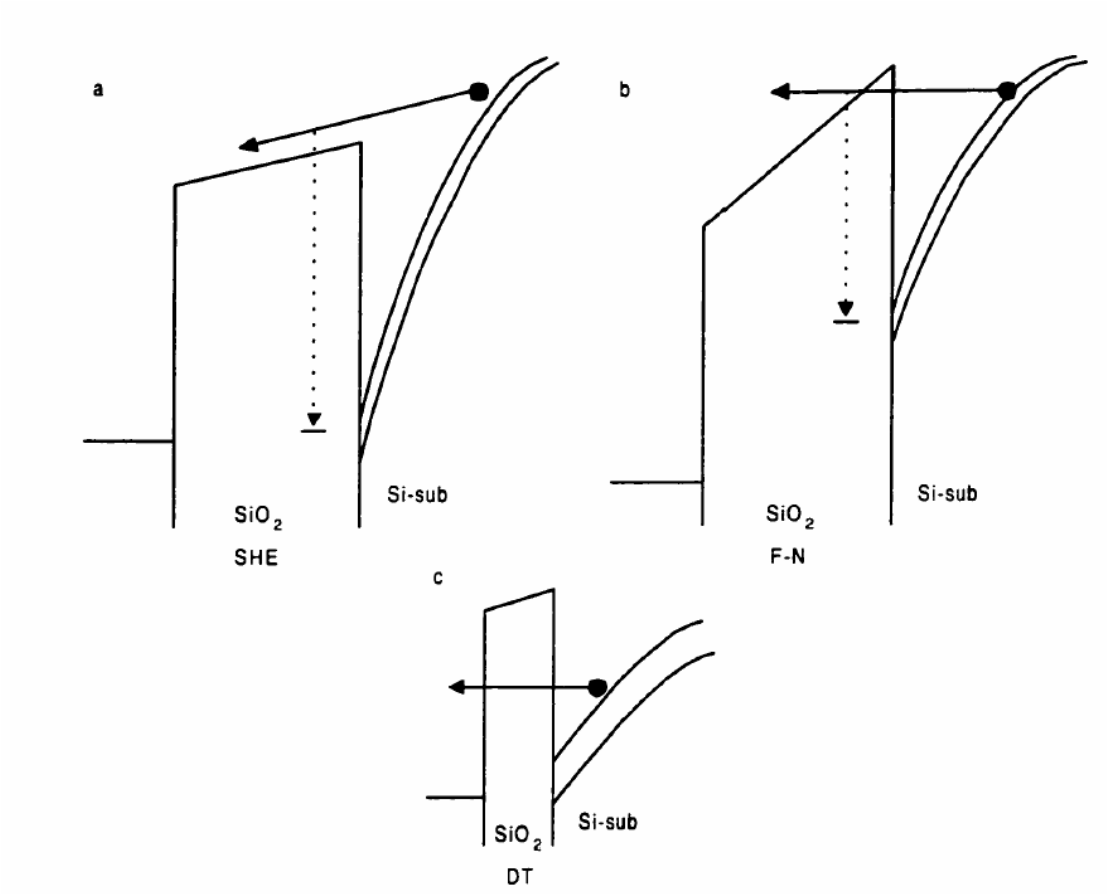


Fig. 2.7 Injection mechanisms: (a) substrate hot-electron injection; (b) Fowler-Nordheim tunnel injection; (c) direct tunnel injection

(6) Direct tunneling (DT) injection: small geometry MOS devices having thin gate insulators (less than 5 nm) may suffer from degradation due to this injection (Fig. 2.7c).

For deep-submicron devices under normal operation conditions (digital and analog), the injection mechanisms involved most are channel hot-electron injection and drain avalanche

hot-carrier injection. For the devices with very thin gate oxide, direct tunneling injection should also be considered.

2.4 Physics of negative bias temperature instability

One of the major temperature-induced reliability issues for p-channel MOSFET is the negative bias temperature instability (NBTI), which is caused by the interface traps under high temperature and negative gate voltage bias.

The overall electrochemical reaction at the interface of pure oxide is of the following form at Si-SiO2 interface [43]:

$$\mathrm{Si-H+O_3-Si-O-Si+h^+ \leftrightarrow Si\square+O_3-Si-OH^+-Si} \tag{2.1}$$

The interface state (Si·) is generated from the dissociation of hydrogen terminated trivalent Si bonds (Si-H) by holes (h^+) in the Si inversion layer. The released hydrogenated species (H^+) diffuse and are trapped near the oxide interface resulting in the positive oxide charges (Si-OH^+-Si). Experiments show that the positively charged hydrogen (H^+) reacts with the SiO_2lattice to form an OH group bonded to an oxide atom [44], leaving a trivalent Si atom (Si_0^+) in the oxide and one trivalent Si_s at the Si surface. The Si_0^+ forms the fixed positive charge (N_{OT}) and the Si_s forms the interface trap (N_{IT}). NBTI stress causes N_{IT} and N_{OT} shifts, contributing mainly to the shift in device characteristics. The N_{IT} and N_{OT} charge shifts are given by

$$\Delta N_{IT}(E_{ox},T,t,t_{ox}) = 9\times10^{-4} E_{ox}^{1.5} t^{0.25} \exp(-0.2/kT)/t_{ox} \tag{2.2}$$

$$\Delta N_{OT}(E_{ox},T,t) = 490 E_{ox}^{1.5} t^{0.14} \exp(-0.15/kT) \tag{2.3}$$

where E_{ox} is the electric field in the oxide, T is temperature, t is stress time, t_{ox} is the thickness of

oxide, k is the Boltzman constant. The NBTI degradation is thermally activated and, therefore, is sensitive to temperature. It degrades more severely the higher the temperature.

Constant high voltage at the drain terminal in real pMOS device results in hot carrier injection. The NBTI effect becomes stronger with negative gate bias, which accelerates thermally generated holes towards the Si/SiO_2 surface, thus increasing NBTI sensitivity.

A fraction of NBTI degradation can be recovered by annealing at high temperatures if the NBTI stress voltage is removed. The electric field applied during anneal can play a role in the recovery of NBTI degradation. Positive bias anneals exhibit the largest recovery in device characteristics [52]. Although it has not been reported yet, however, based on the historical results it is expected that this recovery to be unstable and for the original degradation to reappear soon after reapplication of the stress condition, assuming that hydrogen does not play a reversible role under this condition.

Since NBTI occurs for negative gate voltages, it is particularly detrimental for p-MOSFETs with either p^+ or n^+ poly-Si gates. However, recent data suggest that buried channel (BC) p-MOSFETs are significantly less susceptible to NBTI [53]. The improved reliability in buried-channel compared to surface-channel devices is attributed to the naturally reduced oxide field for the same gate voltage due to the work function difference of n^+ gates compared to p^+ gates and no boron diffusion from the n^+ gate. Also, the effective oxide is thicker in buried- than in surface-channel devices [54]. Thus their use can improve NBTI and $1/f$ noise, though suffering from worse short-channel effects and difficulty in manufacturing due to variance control issues. Currently the majority of digital CMOS technology requires surface channel devices, with this trend continuing into the future. Scaling of technology results in a significant increase in the susceptibility to NBTI degradation. Hence it may ultimately limit device lifetime, since NBTI is

more severe than hot carrier stress for thin oxides at low electric fields.

CHAPTER THREE: HOT CARRIER AND SOFT BREAKDOWN EFFECTS ON CMOS DEVICES

3.1 Hot-Carrier Device Degradation for MOSFET

The damage due to hot-carrier stressing in n-channel devices can fully be explained by the presence of three different damage mechanisms occurring during both dc and ac operation: interface states created at low and mid-gate voltages, oxide electron traps created under conditions of hole injection into the oxide, and oxide electron traps created under conditions of hot-electron injection.

(1) In the low gate voltage range (even below V_T), where the gate current is hole-dominated, three damage species are found-interface states, trapped holes, and neutral electron traps. When stress at low V_g is followed by a brief electron injection phase (stressed at high V_g -conditions of electron injection into the oxide), the neutral electron traps are filled and the trapped holes neutralized, effectively exposing the damage;

(2)At V_g corresponding to the substrate current peak (in the mid-V_g range), both holes and electrons are injected into the oxide. Interfacial trapped holes act as precursors to and transform into interface states when electron are injected into the oxide and are trapped at these sites. The electron-hole link in the formation of interface states is demonstrated in the conditions of maximum substrate current, approximated $V_g = V_d / 2$;

(3)At high gate bias, an electronic gate current-generated oxide trap damage is created. Electron traps and a small amount of interface states are created.

It has been shown that the device degradation is dominated by the increase of interface traps at

mid-gate biases ($V_g = V_d / 2$), close to the maximum substrate current condition on which the characterization for NMOS aging is carried out conventionally.

Electron trapping dominate the damage due to hot-carrier stressing in p-channel device, which is also modeled as the shortening of effective channel length. It was also reported that elevated electric fields cause hole instead of electron trapping, which in turn cause interface state generation. The characterization for PMOS aging is usually made on the condition of maximum gate leakage current.

3.2 Hot-Carrier Life Time Model

Hot carrier induced device degradation in MOS is usually measured by the change in transconductance $\Delta g_m / g_m$, drain current $\Delta I_d / I_d$, and threshold voltage shift ΔVt, etc. We can generalize the degradation by using the symbol ΔD.

The model for degradation under DC bias stress conditions is first developed. Then it is extended to AC bias conditions using quasi-static approximation.

3.2.1 NMOS DC Lifetime Model

For n-channel MOSFETs under a DC stress condition, the amount of degradation as a function of time is given by [35]

$$\Delta D = (A.t)^n \tag{3.1}$$

The proportionality constant A describes the degradation rate as a function of hot carriers

in the MOS channel and is related to substrate current

$$A = \frac{I_{ds}}{H.W}.(\frac{I_{sub}}{I_{ds}})^m \tag{3.2}$$

where H is a constant, and W is the device width.

We define a parameter called *Age*, which will be used to quantify the amount of hot carrier stress:

$$Age = A.t \tag{3.3}$$

3.2.2 PMOS DC Lifetime Model

For p-channel MOSFETs under a DC stress condition, the amount of degradation as a function of time is given by [35]

$$\Delta D = (B.t)^n \tag{3.4}$$

Note that the exponent n for PMOS is generally not equal to the n for NMOS.

The expression for B is

$$B = W_g.\frac{1}{H_g}.(\frac{I_g}{W})^{m_g} + (1 - W_g).\frac{I_{ds}}{H.W}(\frac{I_{sub}}{I_{ds}})^m \tag{3.5}$$

The formula for B allows the degradation in PMOS to be either caused by gate current injection into oxide (Wg=1) or channel hot carrier injection (Wg=0). Wg is the weighting coefficient.

The *Age* for PMOS is calculated using

$$Age = B.t \tag{3.6}$$

The parameters H, m, H_g and m_g have a V_{gd} dependence [35]. There are two implementation options for them:

$$X = X_0 + X_{gd}.V_{gd} \tag{3.7}$$

$$X = 10^{X_0 + \sum_{i=1}^{10} X_{gdi}.V_{gd}^i} \tag{3.8}$$

where X represents H, m, H_g, and m_g.

The parameters mentioned so far, such as A_i, E_{crit}, l_c, H, m and their counterparts for PMOS, can have length- or width-dependent sensitivity parameters. These sensitivity parameter names are the parameter names with subscript l, w or p:

$$P = P_0 + P_l.(\frac{1}{L_{eff}} - \frac{1}{L_{ref}}) + P_W.(\frac{1}{W_{eff}} - \frac{1}{W_{ref}}) + P_P.(\frac{1}{L_{eff}} - \frac{1}{L_{ref}}).(\frac{1}{W_{eff}} - \frac{1}{W_{ref}}) \tag{3.9}$$

where P0 is the length- and width-independent parameter. Pl, Pw, Pp are length- and width-dependent parameters respectively. L_{eff} and W_{eff} are the effective channel length and width from SPICE. L_{ref} and W_{ref} are the reference channel length and width.

3.2.3 AC Lifetime Model

Using a quasi-static method, under AC bias conditions, the *Age* for NMOS is modified to

$$Age = N.\int_0^T \frac{I_{ds}}{H.W}.(\frac{I_{sub}}{I_{ds}})^m dt \tag{3.10}$$

where I_{ds} and I_{sub} are time-varying quantities, and the integral is evaluated for the period T. N is the number of times this period is repeated.

For PMOS, the definition of *Age* under an AC condition is a weighted sum of degradation caused by channel hot electron and gate current injection:

$$Age = N.\int_0^T [W_g.\frac{1}{H_g}.(\frac{I_g}{W})^{m_g} + (1 - W_g).\frac{I_{ds}}{H.W}.(\frac{I_{sub}}{I_{ds}})^m]dt \tag{3.11}$$

3.3 HC and SBD Effects on nMOSFET

In previous chapters, we discuss the mechanisms of hot carrier and soft breakdown. Thus, the acceleration condition for hot carrier and soft breakdown must be determined. The electric field acceleration and temperature acceleration are two conventional test methods. The former one is closely related to the breakdown process and thus is employed more often. Two stress methods, constant voltage stress (CVS) and constant current stress (CCS), are commonly used. The CVS method resembles better the real operation of the devices.

In this work, experimental evidence of the impact of SBD, along with the hot carrier injection, on the RF circuits is presented.

The devices used in this work are 0.16 μm CMOS transistors. The oxide thickness is 2.4 nm and total channel width is 50 μm. Many transistors are tested to verify the physical effect. The wafer is tested with a Cascade 12000 Probe Station and an Agilent 4156B Semiconductor Parametric Analyzer for dc measurements, while the RF experiments up to 10 GHz are carried out using an Agilent 8510C Network Analyzer. Equipments in the experiment for RF characterization include: Agilent 8510C Network analyzer, HP 8517B (45MHz-50GHz) S-parameter test set, HP 83651B (10 MHz-50GHz) 8360B series synthesized sweeper, Summit 12751 Cascade Microtech Probe Station and related softwares. The stress condition is on maximum I_{sub} conditions: V_{GS} = V_{DS} =2.6 V, and the testing condition is the device normally working condition: V_{GS} = 0.85 V and V_{DS} =1.5 V The source and bulk are grounded. S-parameters are measured in the common source-bulk configuration. On-wafer dummy structures are used to calibrate the pad parasites.

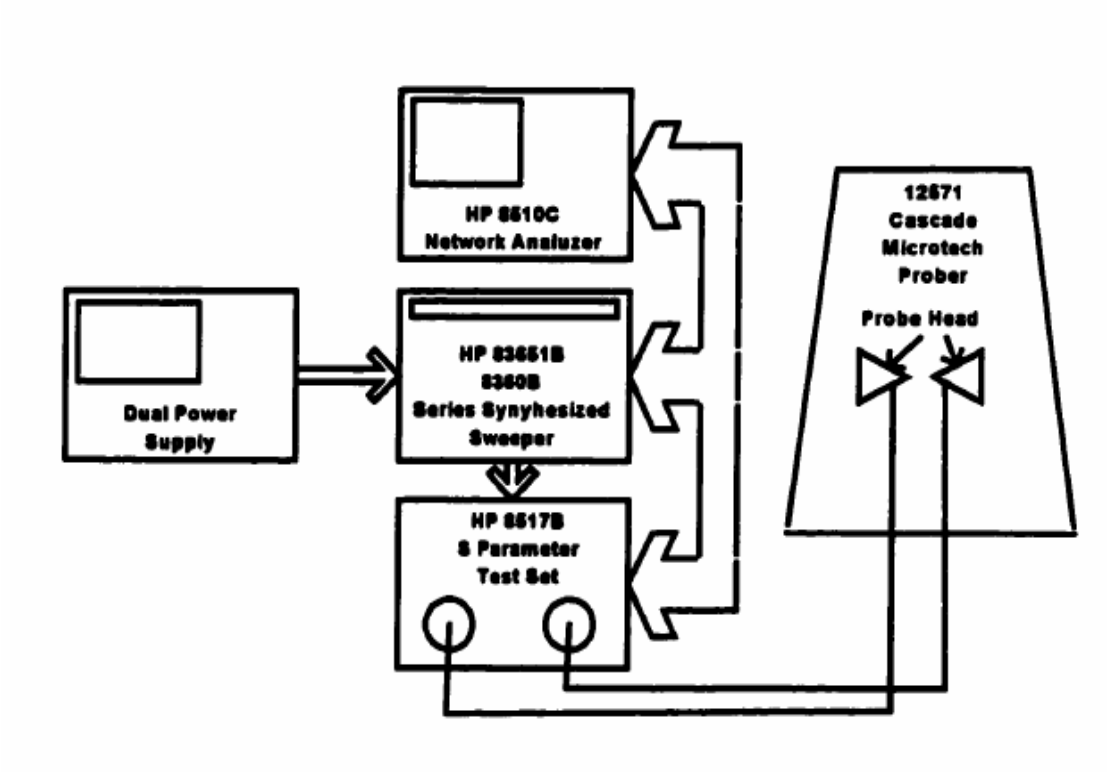


Fig. 3.1 On-wafer s-parameter measurement system

Typical setup for network analyzer measurements at the probe tips connects the HP 8517B test set through cables to the probe heads, as shown in Figure 3.1. In order to get good accuracy, the cables should have low reflections and good repeatability. Two 0.086-inch semi-rigid coaxial cables (26 inches long) are used for the connection between the test set. A good system check is to compare the uncorrected return loss of a short or an open at the probe tips, with the return loss of a 50-ohm load at the probe tips. There should be at least approximately 6 dB of return loss difference between the short or open and the load [8]-[9].

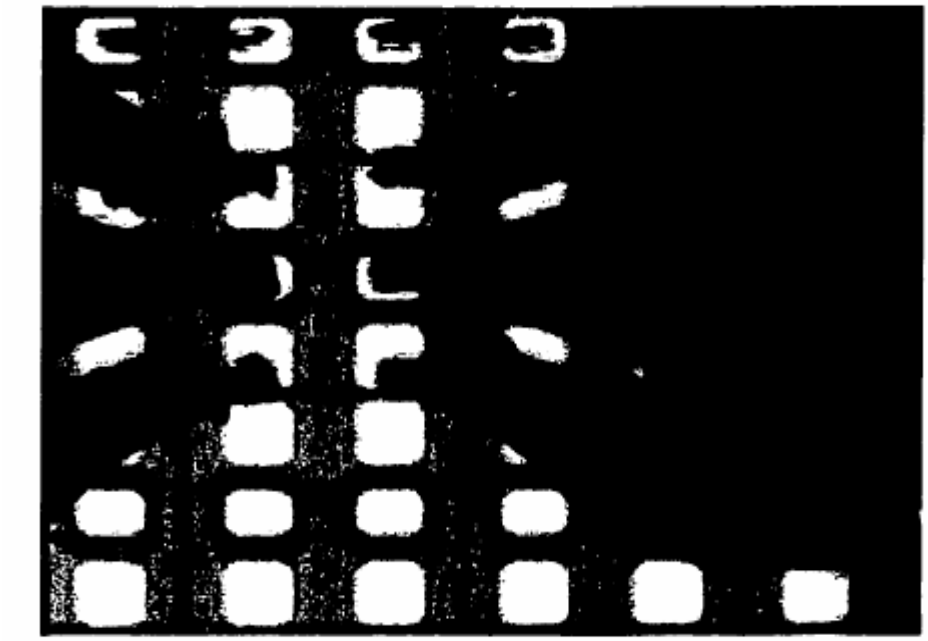


Fig. 3.2 MOSFET testing pad configuration and Cascade probe tip

The S-parameters of single 10/0.16 um and 20/0.16 and 50/0.16 NMOSFET (Tox=24A) in the Lucent CMOS 0.16 um process (lot number 32163) were characterized on a cascade probe station, from which f_T was deduced. The FETs was laid out with ground-signal-ground pad configuration (Figure 3.2), which is suitable for Cascade Microtech probes. Before measurements, the probes are first calibrated by using Cascade Microtech supplied calibration standards (ISS 101-190 LRM). Then on-wafer calibrations are made using the on-wafer Short-open-load-through devices to remove the pad parasitic.

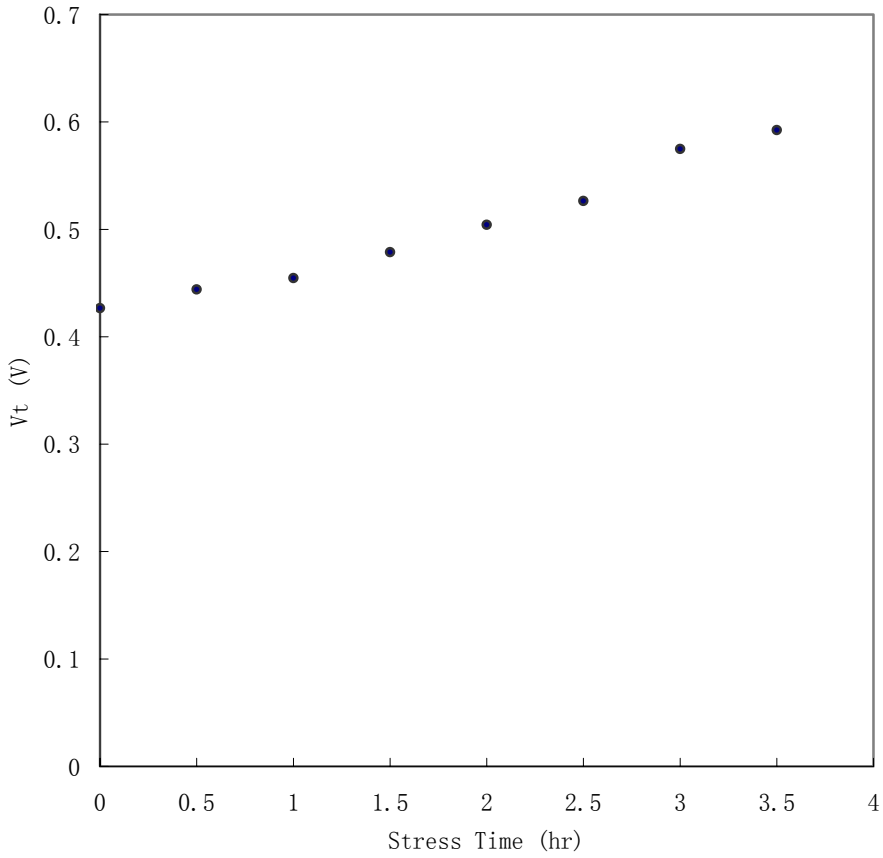


Fig. 3.3 Threshold voltage degradation for NMOSFET

For transistor parameters, it is shown in Fig. 3.3 that for N-channel devices, the measured threshold voltage increases with stress time because of electron trapping. In Fig. 3.4, the measured mobility decreases due to the increase of interface state generation. This is verified by the degradation of the extracted parameters of BSIM3v3 model.

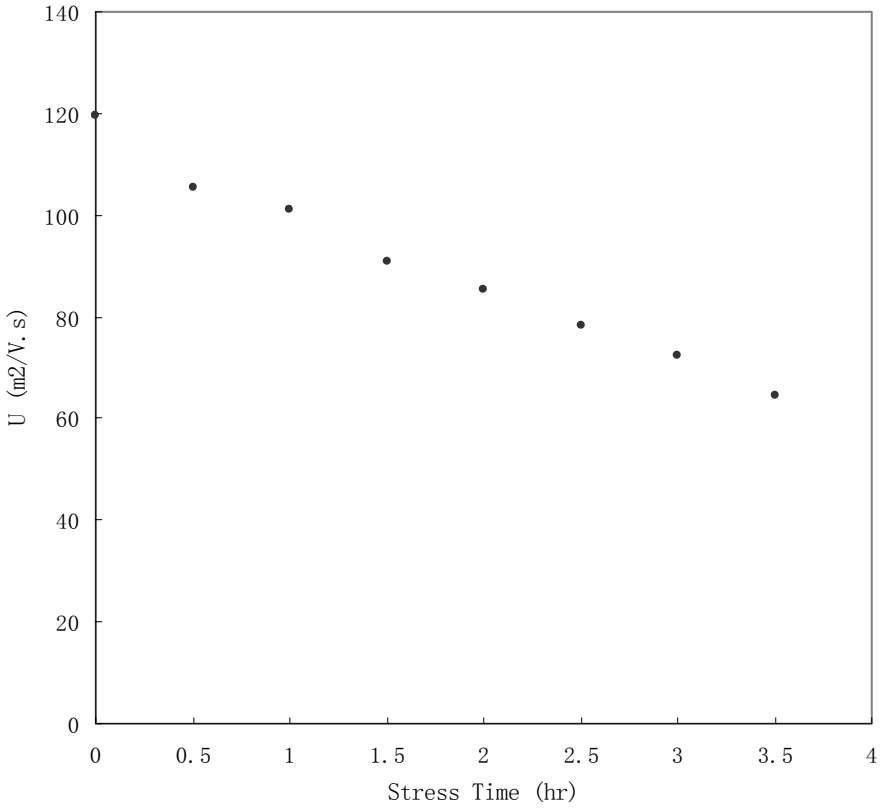


Fig. 3.4 Mobility degradation

Fig. 3.5 shows the measured transconductance g_m degrades with stress time, and it can be seen that the transconductance decreases by 27% over 3.5 hour stress.

The transconductance degradation would in turn impact the gain and other performance of the circuits.

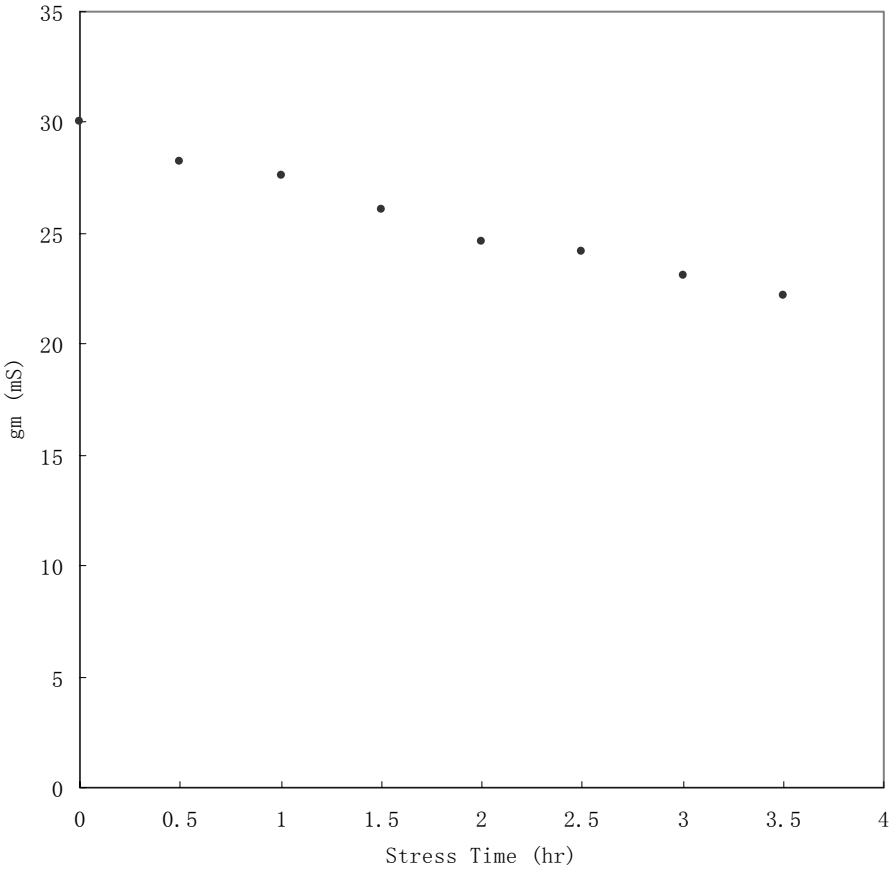


Fig. 3.5 Transcondcutance degradation

3.4 HC and SBD Effects on pMOSFET

Stringent requirements for low noise performance in telecommunication receiver circuits may also demand the use of pMOSFETs in the front end. However, as technology is scaling, deep submicron devices are subject to high vertical and lateral electric field that often deteriorate the RF performance. It is our understanding that our work is the first attempt to investigate hot

carrier (HC) and soft breakdown (SBD) effects on RF performance of pMOS transistors.

The devices used in this work are 0.16 μm pMOSFETs. The oxide thickness is 2.4 nm and channel width is 50 μm. Many transistors are measured to verify the physical effect. The wafer is tested with a Cascade 12000 Probe Station and an Agilent 4156B Semiconductor Parametric Analyzer for dc measurements, while the RF experiments up to 10 GHz are carried out using an Agilent 8510C Network Analyzer. For hot carrier and soft breakdown, the gate and drain voltages for overstress are carefully set at $V_G = V_D = -2.6$ V and then measured at $V_G = -0.85$ V and $V_D = -1.5$ V. The source and bulk are grounded. The transistor models are extracted from device measurements using BSIMPro software. S-parameters are measured in the common source-bulk configuration. On-wafer dummy structures are used to calibrate the pad parasites.

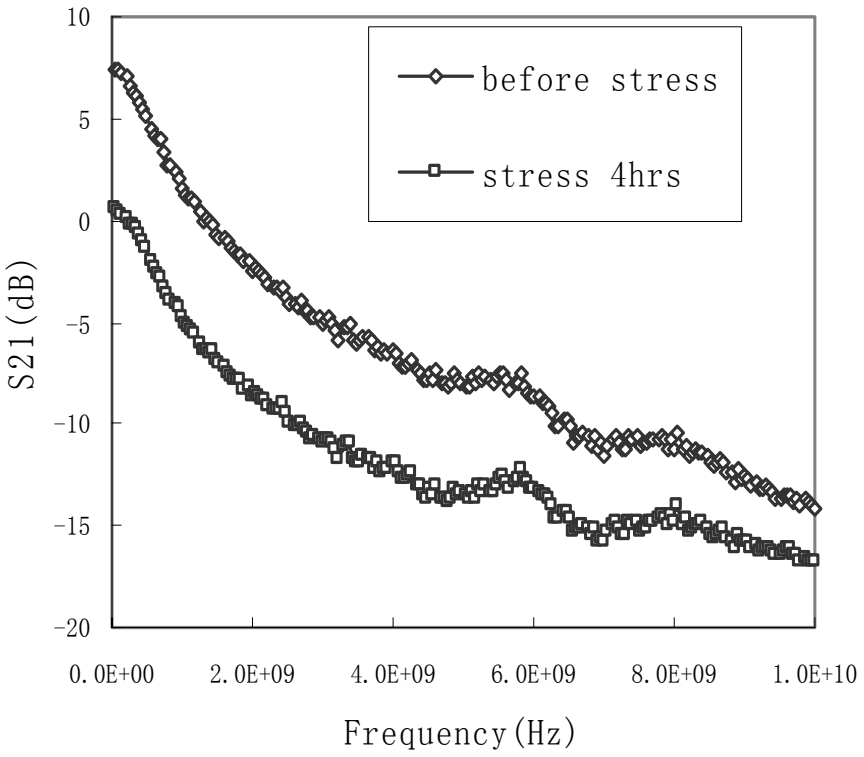


Fig. 3.6 Measured S_{21} versus frequency (fresh device, stressed after 4 hours)

The S-parameters of the devices are measured and cut-off frequency (f_T) is extracted before and after stress. All S-parameters degrade after stress. From the experimental data, $S_{11}$and S_{21} degrade significantly after stress. Fig. 3.6 shows the effect of the stress on the forward transmission scattering parameter (S_{21}). It can be seen that there is a decrease of about 7 dB in magnitude of S_{21}; this is due to the decrease in g_m. The Normalized cut-off frequency degradation is shown in Fig. 3.7. The percentage of degradation of f_T due to hot carrier and soft breakdown increases with stress. It is interesting to note that it saturates after a stress of about 2 hours when it reaches 15% degradation.

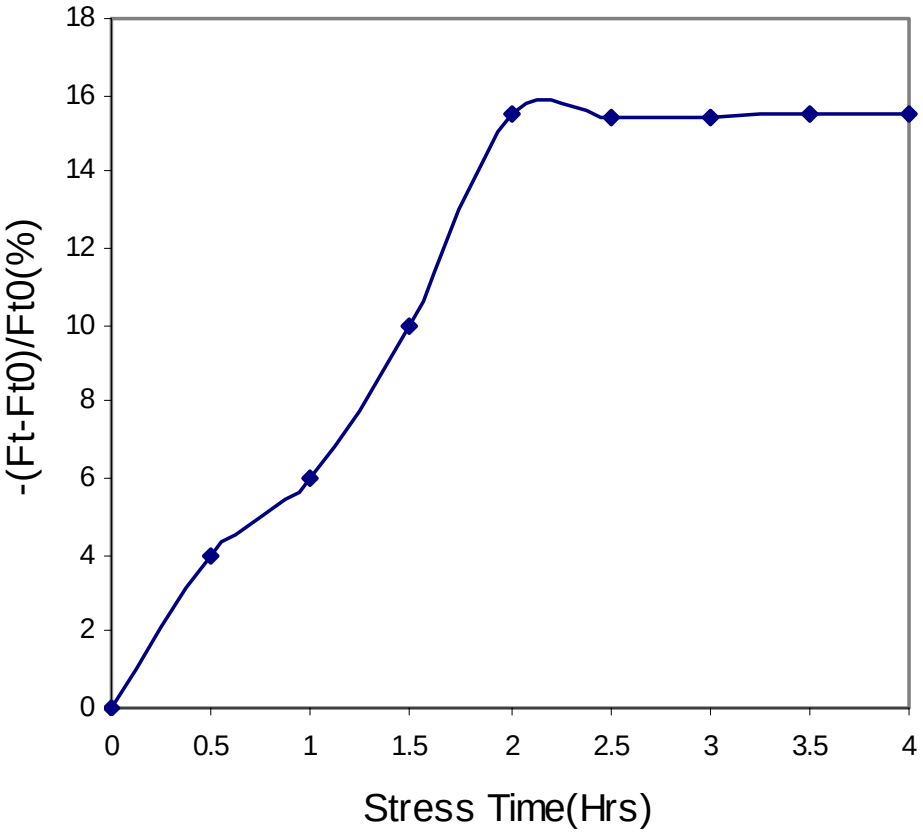


Fig. 3.7 Normalized f_T versus time due to hot carrier and soft breakdown

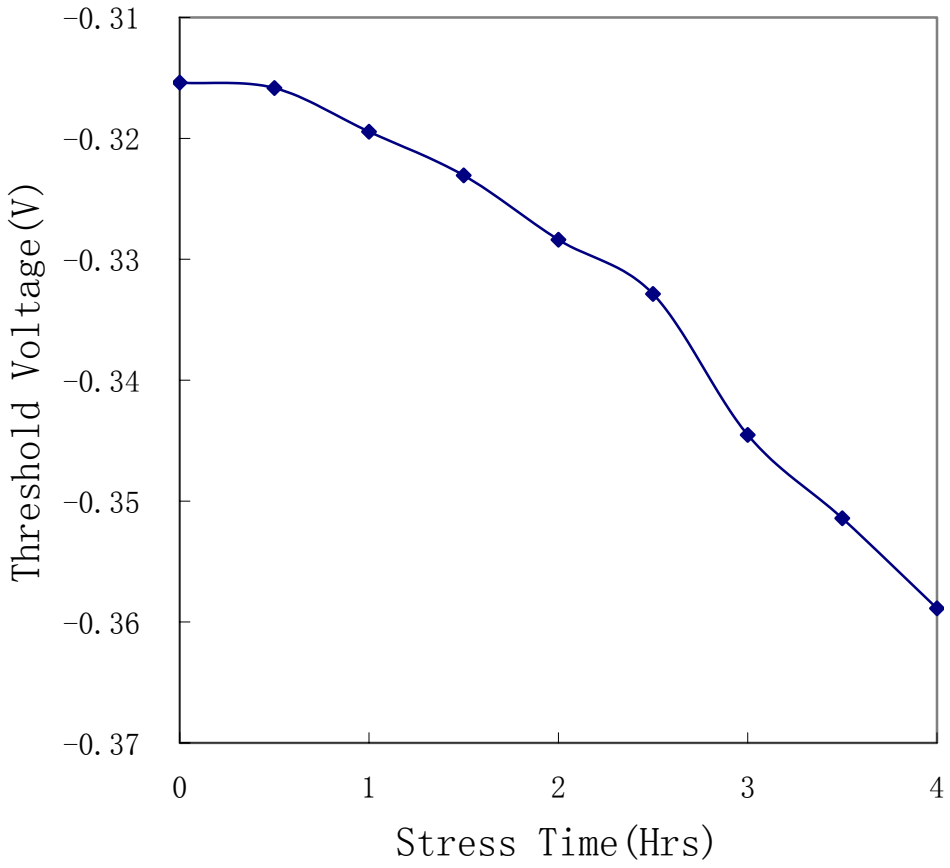


Fig. 3.8 Threshold voltage degradation versus stress time

For pMOS transistors, the threshold voltage will shift positively due to hot carrier stress. The reason is that electrons are injected and trapped in the gate oxide near the drain [36]. However, a negative shift in threshold voltage is observed in pMOS transistors after hot carrier and soft breakdown stress, as shown in Fig. 3.8. This can be explained that during hot carrier and soft breakdown stress, hot electrons and hot holes are generated by the high lateral electric field and the high vertical field leads to the hot-hole trapping. After breakdown, many conducting path form in the gate oxide .This is also a favorable condition for hole-trapping. By referring to the equation for V_T [14]:

$$V_T = -\frac{Q_{ox}}{C_{ox}} - \frac{Q_d}{C_{ox}} + \phi_{ms} + 2\phi_{FB} \tag{3.12}$$

It can be seen that Q_{ox} increases due to hole-trapping, and this leads to the negative shift in threshold voltage in pMOS transistors.

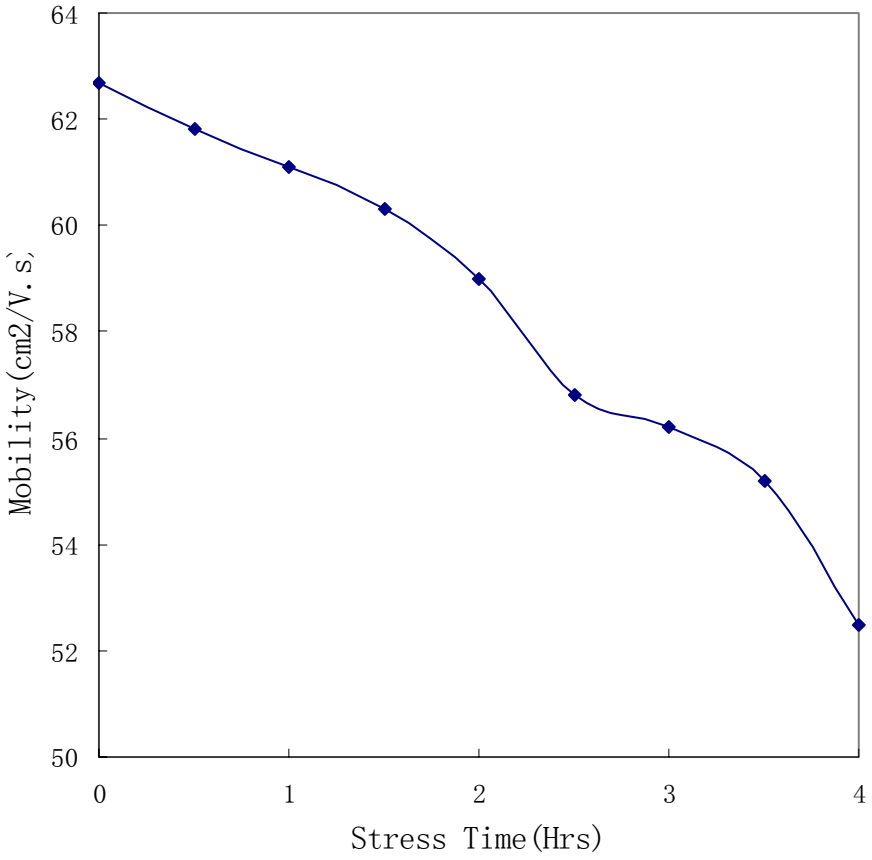


Fig. 3.9 The mobility degradation versus stress time

In Fig. 3.9, the measured mobility degradation is shown. It can be seen that measured mobility decreases due to the interface state generation.

While traditionally bipolar and compound substrate devices are used for high frequency

RF and microwave circuits, as technology is scaling down and the cutoff frequency of the MOS devices are going up, CMOS technology becomes attractive as well. However, as it has been demonstrated though measurements, soft breakdown and hot carrier effect on the MOS devices appears as a pitfall reducing the cutoff frequency. Moreover, increase of threshold voltage and decrease of mobility reduce the transconductance of the device that degrade the performance of a circuit. As an example, lower transconductance reduces the gain of the amplifiers.

3.5 Conclusion

In chapter 3, the impact of HC and SBD stress on the CMOS RF device has been examined using 0.16 μm CMOS technology. Device parameters of 0.16 um CMOS technology were measured before and after stress for nMOSFET and pMOSFET. HC and SBD stress reduces the cutoff frequency, the measured mobility of nMOSFET and pMOSFET both decreases, there is a positive shift for nMOSFET and negative shift for pMOSFET.

CHAPTER FOUR: GATE OXIDE BREAKDOWN AND MODELING METHOD

4.1 Introduction

Due to continued scaling, deep sub-micrometer CMOS transistors can result in a cutoff frequency (f_T) over 150 GHz and noise figure lower than 0.5 dB [1]. On the other hand, when the oxide is scaled down to less than 3 nm, soft breakdown (SBD) is more likely to take place [2]-[4]. Nowadays, the oxide has already been scaled down to 1.2 nm [5], so it is essential to study the oxide breakdown effect on deep sub-micrometer RF MOS transistors and circuits.

In Chapter 2, physical mechanism of soft breakdown is introduced. Then, the in-house stress experiment procedures will be described in this section. An improved f_T model equation accounting for oxide breakdown has been developed [57]. A small-signal equivalent circuit of the MOSFET after breakdown is employed for accurate parameter extraction using *Y*-parameters converted from measured *S*-parameters. Data measured on the MOS transistor biased in the linear region before and after breakdown are used to extract the breakdown spot resistance and total gate capacitance. This methodology provides critical information about the impact brought by gate oxide breakdown.

4.2 RF device characterization by Measurement to evaluate SBD effect

The RF parameters of MOSFETs are affected by SBD effects. The experiments were performed on the same wafer. The devices used in this work are 0.16 μm CMOS transistors. The oxide thickness is 2.4 nm and total channel width is 50 μm. Many transistors are tested to verify the physical effect. The wafer is tested with a Cascade 12000 Probe Station and an Agilent 4156B Semiconductor Parametric Analyzer for dc measurements, while the RF experiments up to 10 GHz are carried out using an Agilent 8510C Network Analyzer. It is found that the breakdown voltage is about 3 V. For soft breakdown, the accelerated stress is carefully set at V_G = 2.6 V, and V_D =0 V. The source and bulk are grounded. S-parameters are measured in the common source-bulk configuration. On-wafer dummy structures are used to calibrate the pad parasites.

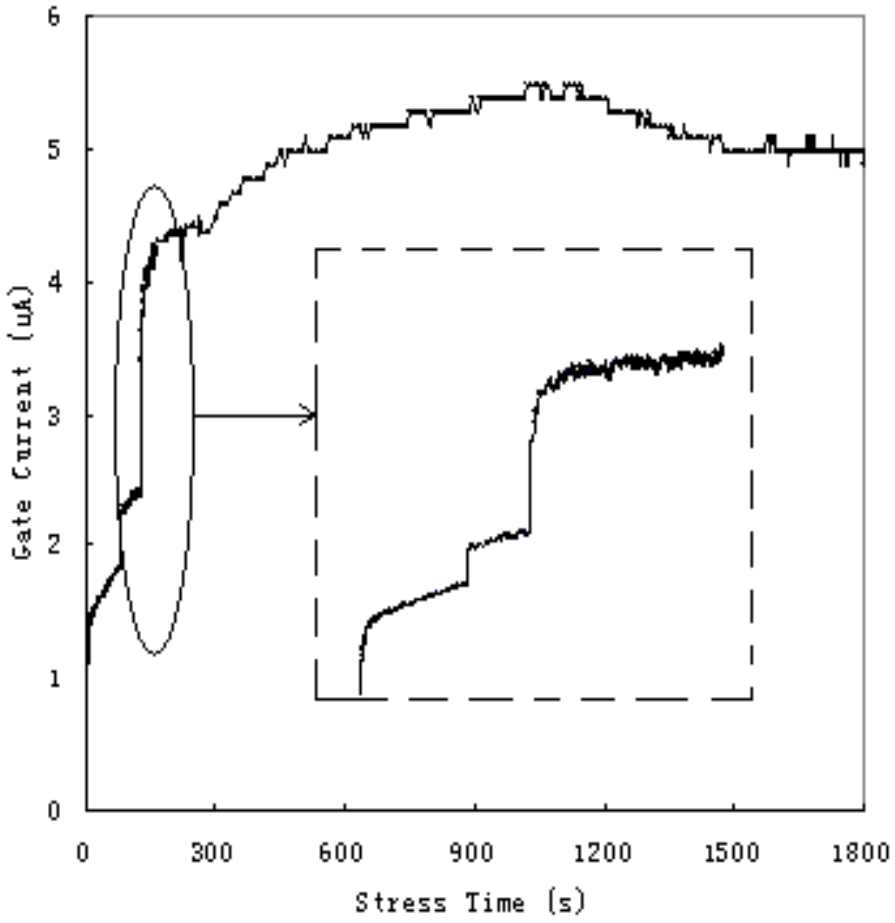


Fig. 4.1 Gate current versus time

A typical time-dependent dielectric breakdown (TDDB) result is shown in Fig. 4.1 .It can be seen that the gate current increases drastically after the device is stressed about 80 s and 120 s, which indicates the occurrences of gate oxide breakdown. The S-parameters of the devices are measured.

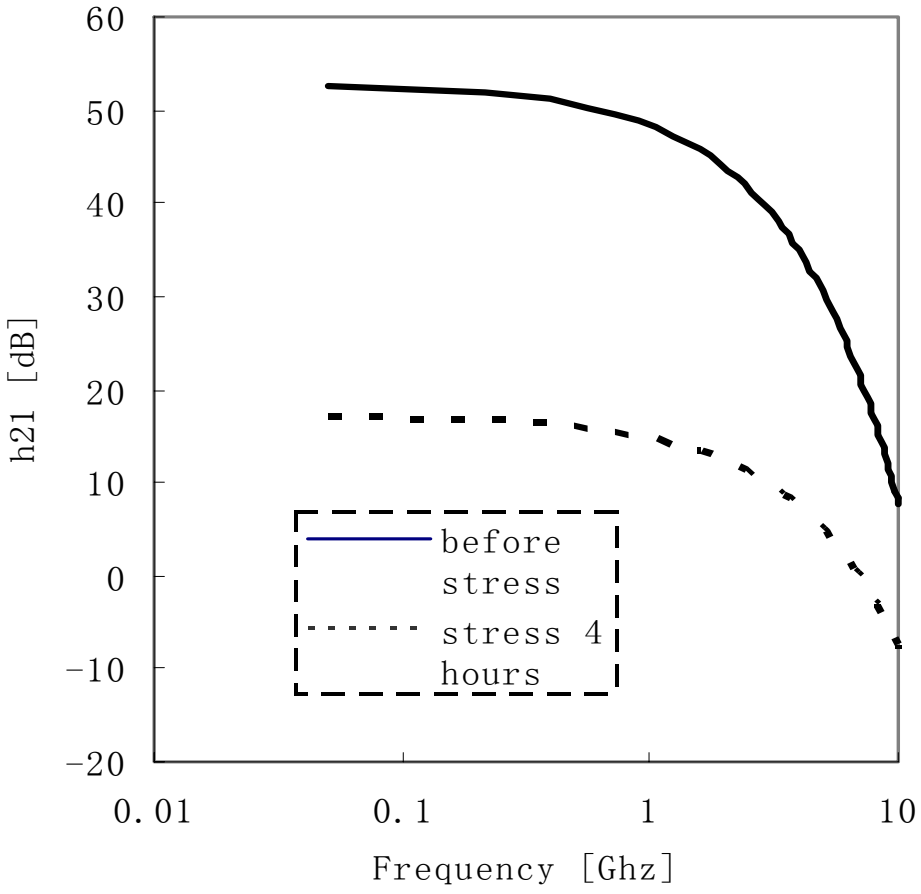


Fig. 4.2 Current gain h_{21} as a function of the frequency (before stress and stress 4 hours)

The current gain h_{21} and cutoff frequency are extracted before and after stress. h_{21} decreases

with an increase of frequency at very high frequencies. After breakdown, there is a large drop in h_{21}, as shown in Fig. 4.2. The normalized cutoff frequency degradation is displayed in Fig. 4.3. The percentage of degradation of f_T due to oxide breakdown increases with stress. It is interesting to note that the degradation saturates after 2 hours of stress when it reaches 25 % degradation. This may be explained by the fact that the gate leakage current increases gradually after breakdown and is limited by the parasitic resistance , hence, there are less conducting paths formed in the gate oxide after 2 hours' stress, leading to fewer degradation effects on f_T .

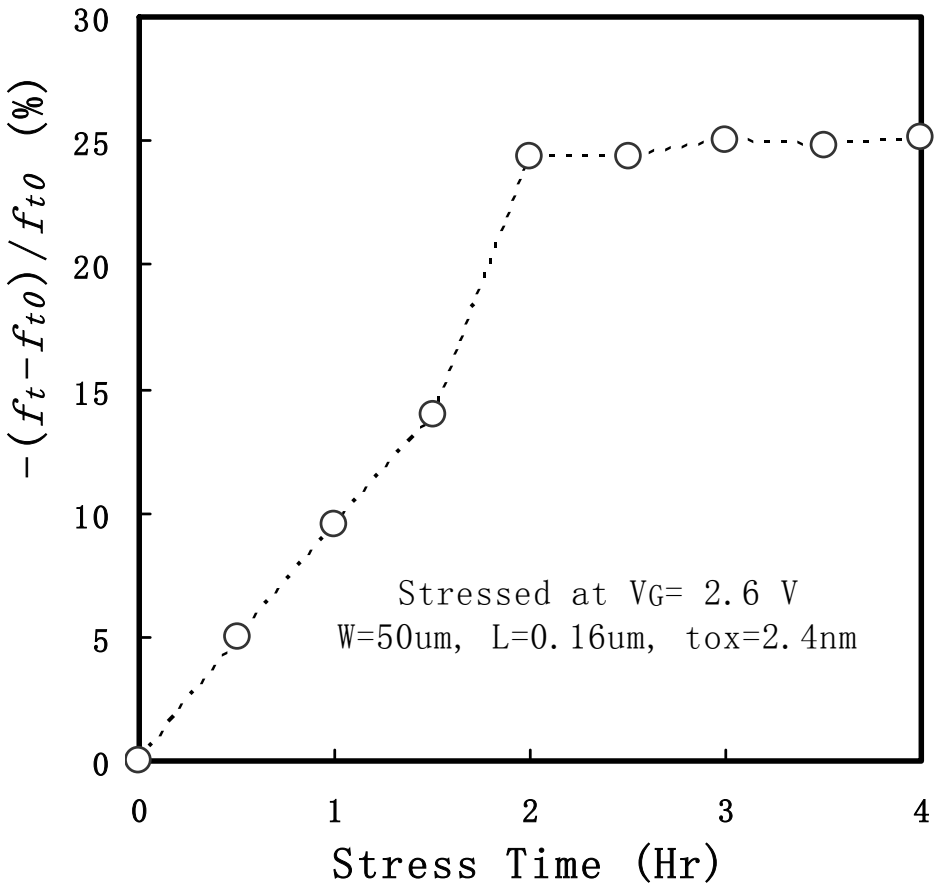


Fig. 4.3 Normalized f_T versus time due to Soft Breakdown

4.3 Model and Parameter Extraction

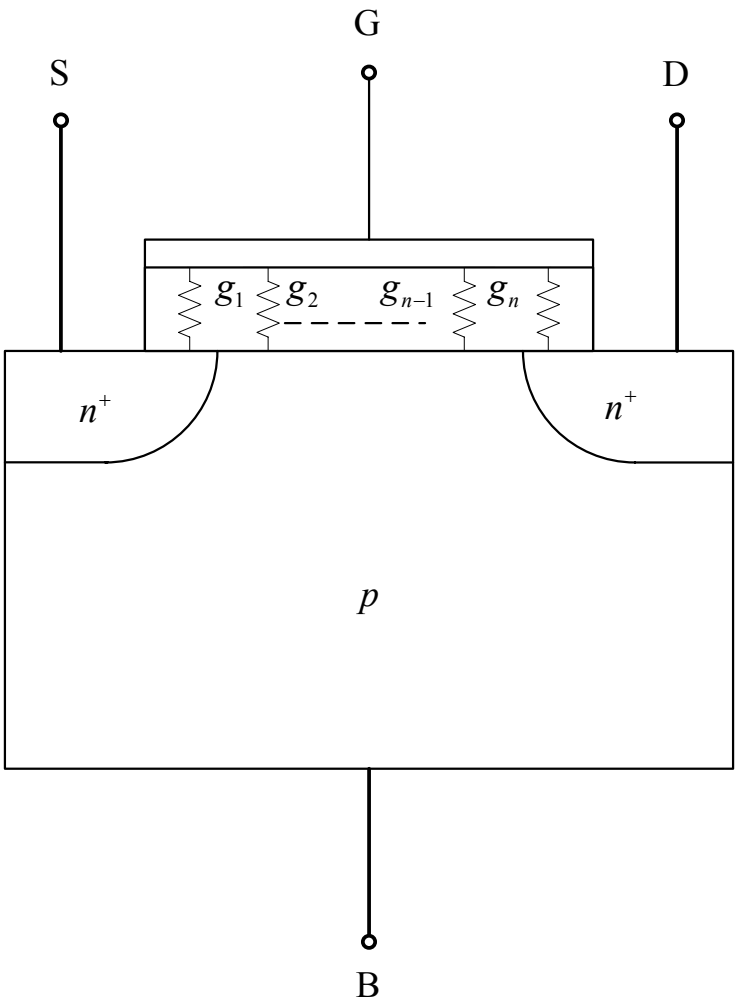


Fig. 4.4 Distribution of breakdown conductances inside oxide after breakdown

In 4.2, some experimental results of SBD stress are given, we can then use these results to find more parameters that are related to circuit performance.

When a device is stressed by an applied voltage, an oxide film loses its insulating properties and traps are generated within the oxide that increase the leakage current through the film. Eventually, these traps complete some conducting paths that bridge the two electrodes across the

oxide [11]-[13]. At a given time, assume the number of conducting paths inside the gate oxide is *n*, and each of the conducting paths is associated with a conductance $g_i, i = 1, 2, ...n$, these conducting paths divide the resistance R_{ds} between drain and source into many parts. This situation is illustrated in Fig.4.4. As stress time increases, more and more conducting paths form, and gate leakage current increases. In this case, the well-known equation for f_T [14] needs to be re-examined.

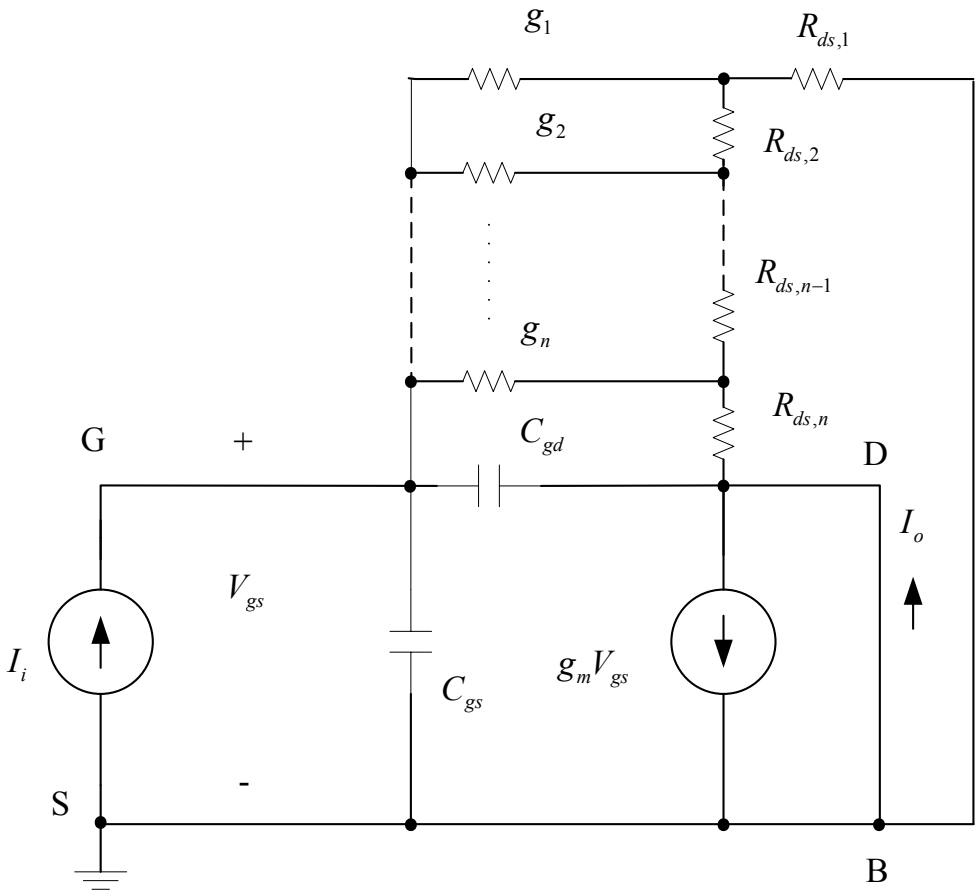


Fig. 4.5 Equivalent small-signal circuit of the nMOS transistor after breakdown

In order to evaluate the impact of breakdown on RF performance of nMOS transistor, cutoff frequency after breakdown should be calculated. The equivalent small signal equivalent circuit of

the nMOS transistor after breakdown is shown in Fig. 4.5.

Without considering the parasitics, expression for the cut-off frequency is derived in the following matter [14]: Place a short circuit across the output, apply a sinusoidal current that has an effective value I_i to the input, and determine the expression for the current I_o in the short-circuit. After breakdown, the input current become

$$I_i = \left(j\varpi \left(C_{gs} + C_{gd} \right) + \left(g_1 + g_2 ... + g_n \right) \right) V_{gs} \tag{4.1}$$

where, $g_0 = g_1 + g_2 + ...g_n$.

The short-circuit output current is given by

$$I_o = g_m V_{gs} \tag{4.2}$$

The magnitude of the current gain becomes

$$|\frac{I_i}{I_o}| = |\frac{g_m}{g_0 + j\omega(C_{gs} + C_{gd})}| \tag{4.3}$$

Regardless of the hardness and location of breakdown, accounting for the gate oxide breakdown, the frequency at which the magnitude of the current gain is unity is therefore found to be at the f_T as

$$f_T = \frac{\sqrt{g_m^2 - g_0^2}}{2\pi(C_{gs} + C_{gd})}, \tag{4.4}$$

when $g_0 = 0$, (4.4) reduces to the conventional expression

This equation reveals the relationship between breakdown conductance and cut-off frequency quantitatively, which shows the degree of device degradation depending on hardness of breakdown. For soft breakdown, the breakdown spot resistance is around 10^6 Ω [15], which is

equivalent to $g_0 \sim 10^{-6} S$, but g_m has the magnitude of $10^{-3} S$, it means soft breakdown spot resistance will not affect cutoff frequency significantly. But if hard breakdown occurs, since the breakdown spot resistance of hard breakdown is around 10^3 Ω, the magnitude of g_0 can be comparable to that of g_m, the cutoff frequency will be greatly affected. Reduction of f_T limits the use of such devices in high frequency circuits and degradation of g_m degrade the performance of RF circuits.

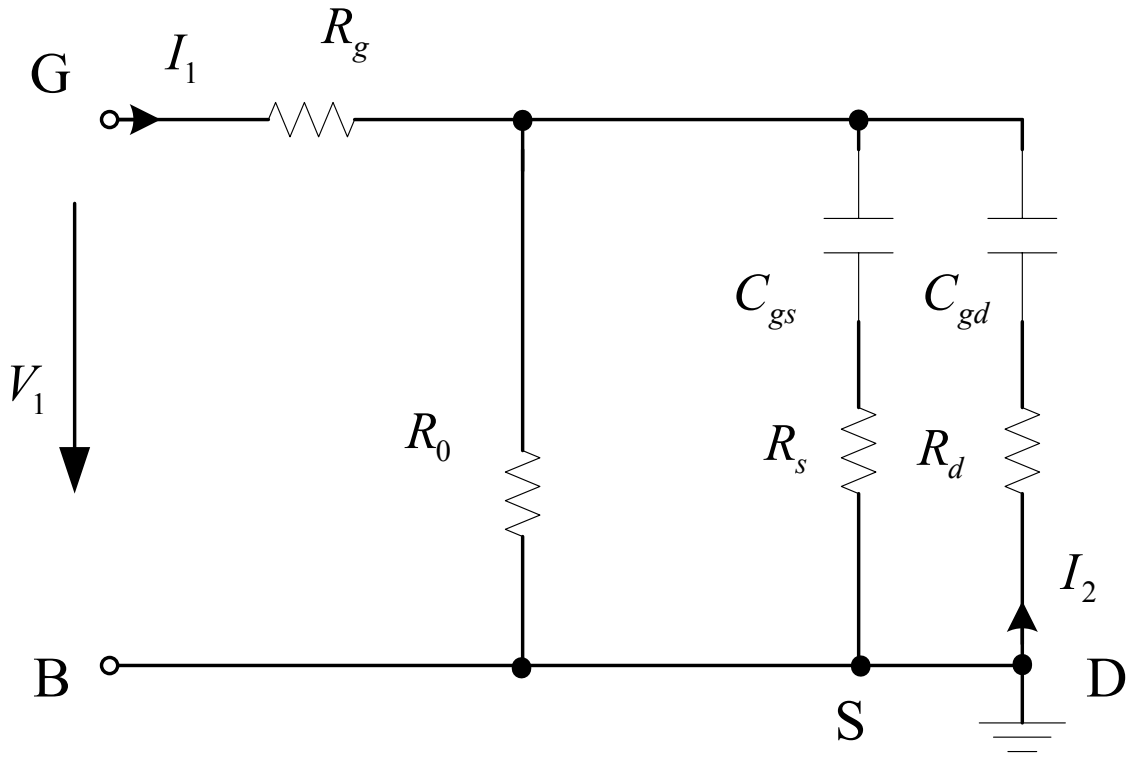


Fig. 4.6 Small-signal equivalent circuit after breakdown for calculation of Y_{11} in the linear region ($V_{DS} = 0$ V)

The parameters in (4.4) have been extracted following the procedures in [16]. Small-signal equivalent circuit that has been used for the calculation of Y_{11} in the linear region is given in Fig.

4.6. The breakdown equivalent resistance R_0 is added to the equivalent circuit, and also the external components such as R_g, R_d and R_s are considered so that accurate parameter extraction can be implemented. The input admittance Y_{11} can be expressed as:

$$Y_{11} = \left(R_g + \left(\frac{1}{R_0} + \left(\frac{1}{R_s + \frac{1}{j\omega C_{gs}}} + \frac{1}{R_d + \frac{1}{j\omega C_{gd}}} \right) \right)^{-1} \right)^{-1} \tag{4.5}$$

where $R_0 = 1/g_0$.

If it is expanded, (4.5) has many higher order terms. By using assumptions in [16], some of the higher order terms are negligible, and (4.5) can be simplified to:

$$Y_{11} \cong \frac{1}{R_0} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d) + j\omega C_{gg} \tag{4.6}$$

$$R_0 = \left| \frac{1}{\mathrm{Re}\,al(Y_{11}) - \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d)} \right|_{(BD)} \tag{4.7}$$

$$C_{gg} = \left| \frac{\mathrm{Im}\, g(Y_{11})}{\omega} \right| \tag{4.8}$$

Note that (4.6) is the expression of Y_{11} after breakdown, while the expression of Y_{11} before breakdown is given as follows:

$$Y_{11} = j\omega C_{gg} + \omega^2 (C_{gg}^2 R_g + C_{gs}^2 R_s + C_{gd}^2 R_d) \tag{4.9}$$

Because $R_g, R_s,$ and R_d are dominated by the resistive poly-silicon and diffusion layers and treated as bias- , stress- and frequency-independent. They can be extracted from the Y-parameters before breakdown [15].

$$R_g = \left| \frac{\mathrm{Re}\,al(Y_{12})}{\mathrm{Im}\,ag(Y_{12}).\mathrm{Im}\,ag(Y_{11})} \right|_{(FRESH)} \tag{4.10}$$

Due to the symmetry reasons,

$$R_d = R_s = \left| \frac{\mathrm{Re}\,al(Y_{21}) - \mathrm{Re}\,al(Y_{12})}{\mathrm{Im}\,ag(Y_{12})^2} \right|_{(FRESH)} \tag{4.11}$$

After breakdown, since the transistor is operating in the linear region with $V_{DS} = 0\,\mathrm{V}$, C_{gd} is approximately equal to C_{gs}, from equation (8)

$$C_{gd} = C_{gs} \cong \frac{C_{gg}}{2} \tag{4.12}$$

Using (4.7) and (4.8), R_0 and C_{gg} can be obtained from the *Y*-parameters converted from *S*-parameters.

The comparison of the real part and imaginary part of Y_{11} before and after breakdown is given in Fig. 7 and Fig. 8. It is seen that stress affects *Y*-parameters, especially the real part [17]. The change of real part of Y_{11} represents the breakdown effect on the gate oxide resistance. The change of imaginary part of Y_{11} demonstrates the effect of breakdown on the gate oxide capacitance. The defective region in the oxide around the BD spot leads to an increase of the MOSFET threshold voltage and decreases the channel electron mobility thus depressing the real part of Y_{11} and f_T, and also the transconductance is decreased, resulting in further degradation in f_T.

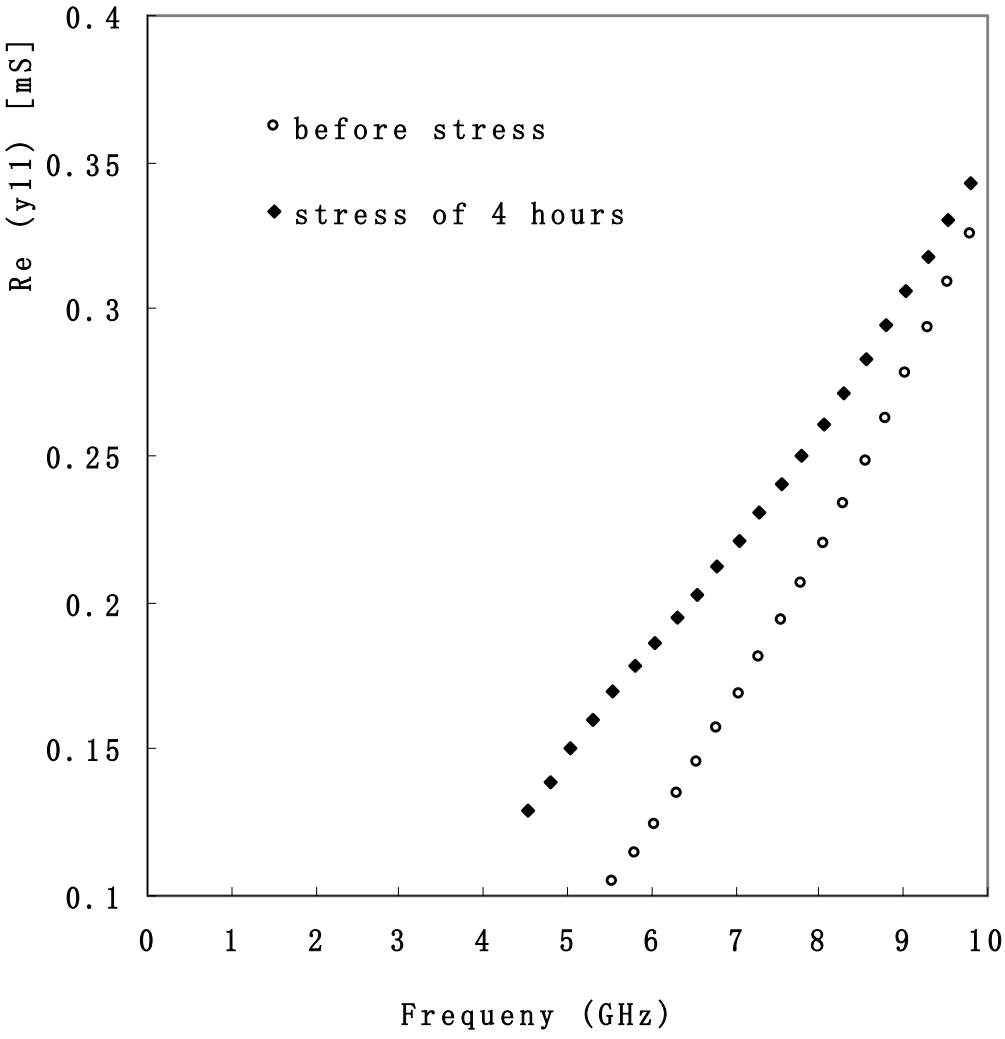


Fig. 4.7 Real part of Y_{11} as a function of the frequency before and after stress

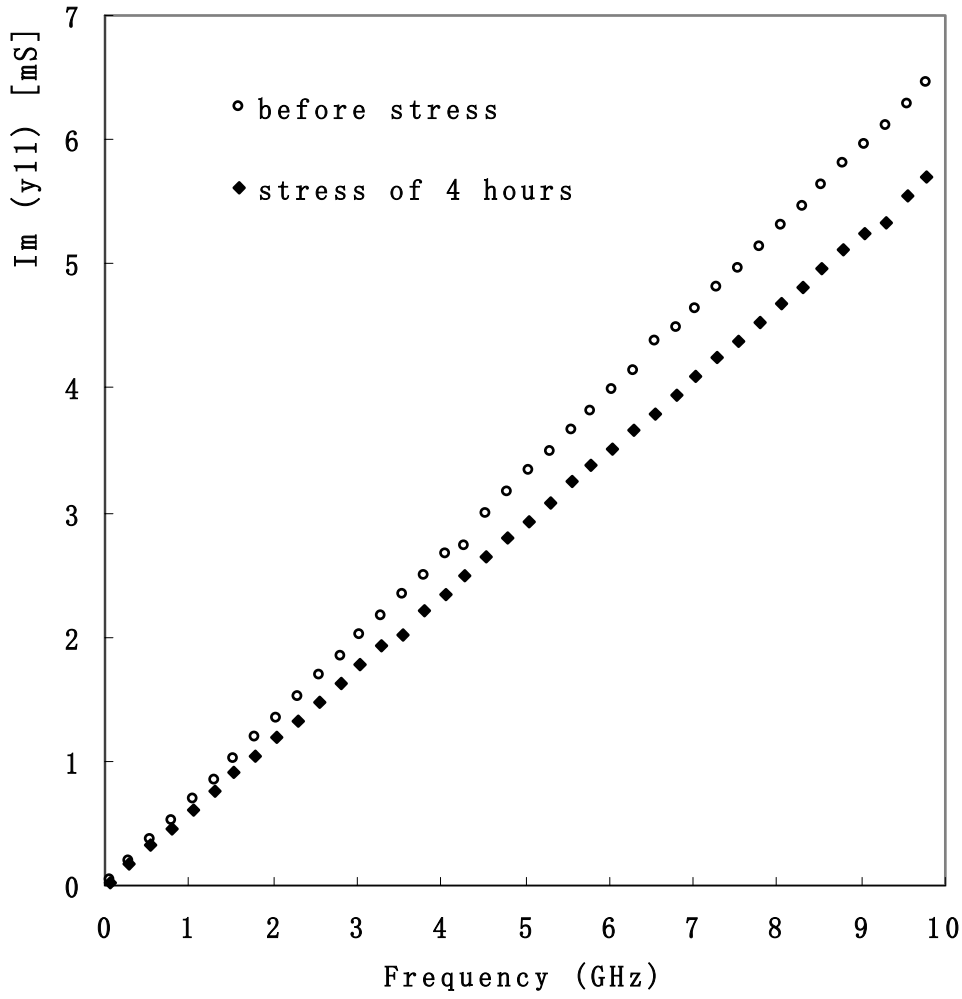


Fig. 4.8 Imaginary part of Y_{11} as a function of the frequency before and after stress

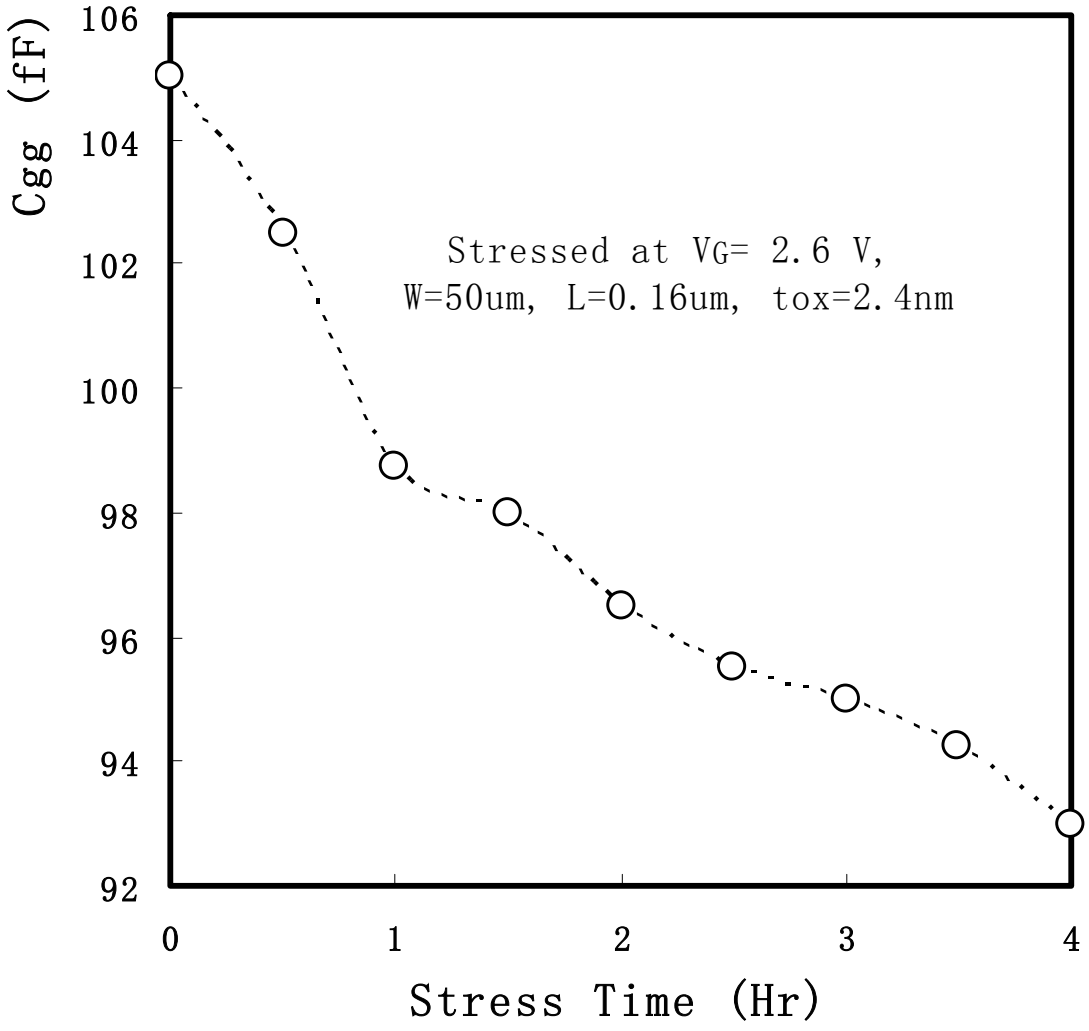


Fig. 4.9 R_0 versus stress time

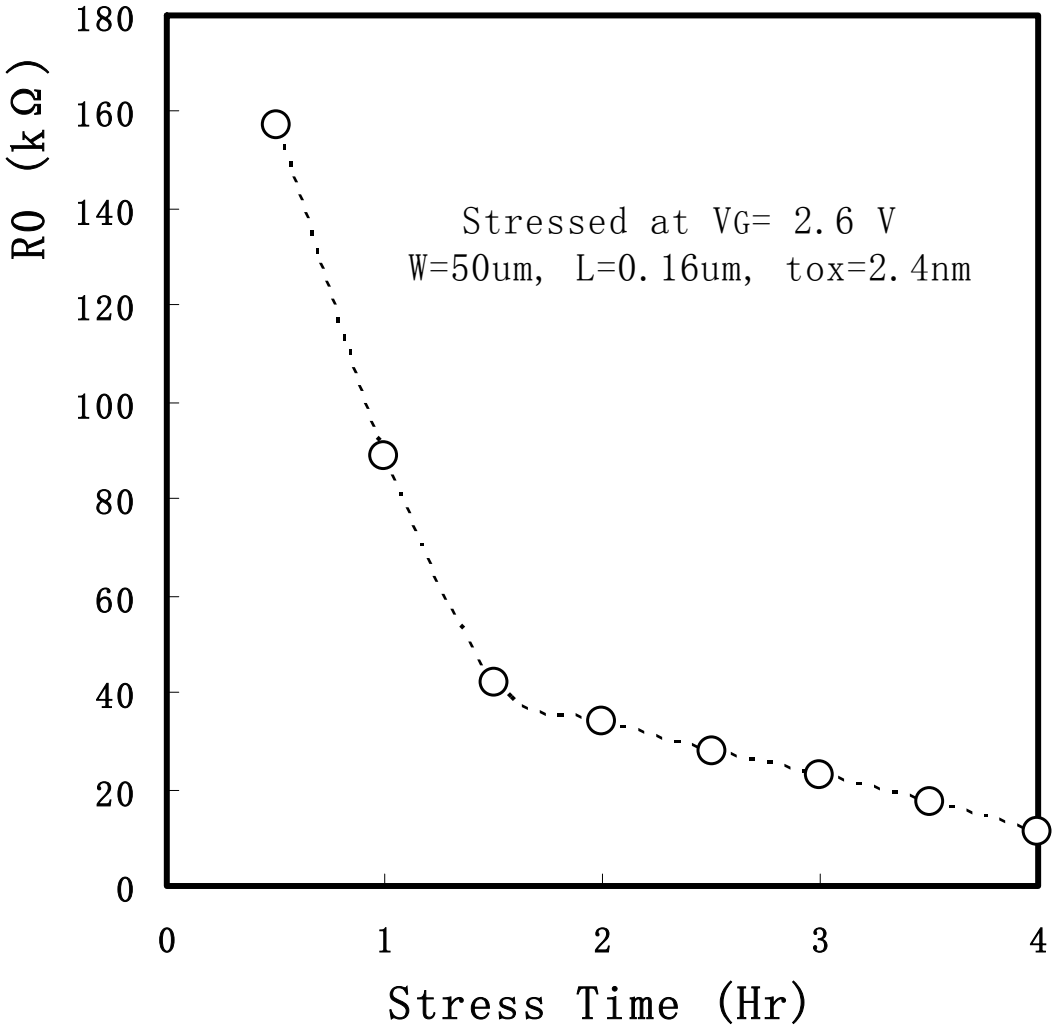


Fig. 4.10 C_{gg} versus stress time

Using (4.10), (4.11), in the range of 5GHz to 10GHz, $R_g, R_s,$ and R_d are extracted from the Y-parameters converted from *S*-parameters before breakdown: $R_g = 8.12\,\Omega$, $R_d = R_s = 1.24\,\Omega$, they are bias- , stress- and frequency-independent. C_{gg}, C_{gd} and C_{gs} can be extracted from (4.8) and (4.12). R_0 is thus available from (4.7). From Fig. 4.9, it can be seen that the breakdown

spot resistance decreases to 11 kΩ. C_{gg} versus stress time is shown in Fig. 4.10. The gate oxide capacitance C_{gg} decreases with stress time due to formation of conducting paths caused by traps which degrades the integrity of gate oxide. In [18] it is found that the area of an oxide defective region around the BD spot is much larger than the BD conductive path. It is explained that the neighboring region around the BD spot also loses the capability to hold charges. Figure 4.10 shows that in every half of an hour the gate capacitance reduces about 2 %, which corresponds to an effective gate oxide area reduction in the order of 10^{-9} cm^2. This is consistent with [18], where the area of the damaged region of each BD spot is around 10^{-10} cm^2 and multiple breakdowns give the effective damage area greater than 10^{-10} cm^2. The decrease of C_{gg} may result in an increase of f_T, however, the decrease of the transconductance g_m (not shown here) is faster than that of gate oxide capacitance C_{gg}, in addition, the breakdown conductance also increases with stress time, thus leading to the degradation of f_T. From Fig.4.9 and Fig. 4.10, note that the degradation of R_0 and C_{gg} slows down after 2 hours of stress. This observation is consistent with the saturation of cutoff frequency degradation after 2 hours of stress. These degradations would degrade the RF circuit performance dramatically. The VCO performance degradations will be shown in the following chapter.

4.4 Conclusion

In this Chapter, an improved f_T model equation accounting for oxide breakdown has been

developed. A small-signal equivalent circuit of the MOSFET after breakdown is employed for accurate parameter extraction using *Y*-parameters converted from measured *S*-parameters. Data measured on the MOS transistor biased in the linear region before and after breakdown are used to extract the breakdown spot resistance and total gate capacitance.

CHAPTER FIVE: RF PERFORMANCE DEGRADATION DUE TO BREAKDOWN EFFECT

5.1 Introduction

In previous chapters, mechanism of breakdown and its effect on sub-micron MOSFETs were discussed. We can expect that the MOSFETs performance degradations would in turn affect the circuit performance.

Phase noise and timing jitter were shown to be important performance specifications. Particularly critical in PLL systems is the phase noise of the VCO. A high "Q" off chip resonant element is often the most desirable design option. But for highly integrated system a fully monolithic, on-chip solution to the VCO may be required.

Due to their relatively good phase noise, ease of implementation, and differential operation, cross-coupled inductance–capacitance *(LC)* oscillators play an important role in high-frequency circuit design.

As we know, VCO phase noise is the main contribution to the whole PLL phase noise out of the PLL bandwidth. It would be critical for the whole systems. In this chapter, we will focus on LC oscillator phase noise and analyze the soft breakdown effect on LC oscillator.

5.2 PLL Noise Model

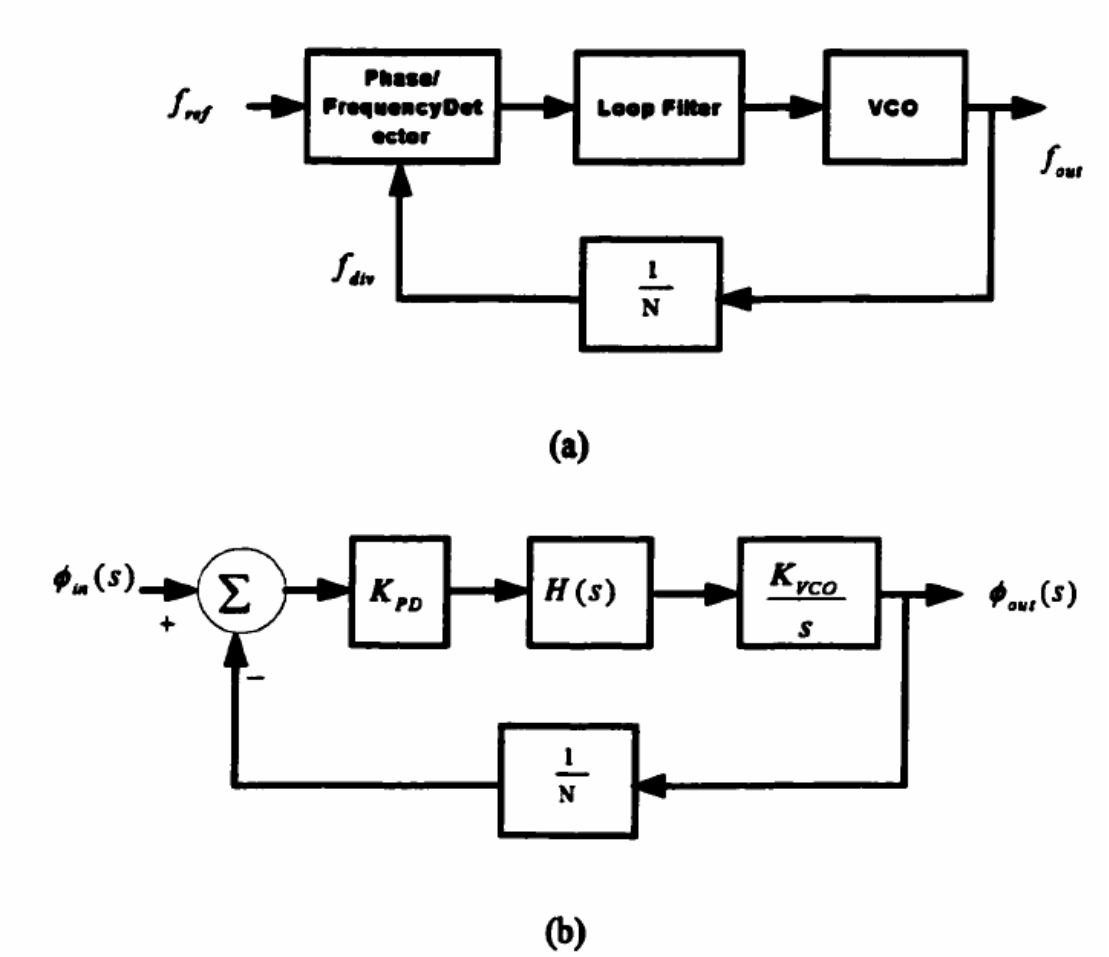


Fig. 5.1 (a) Typical PLL blocks (b) Equivalent phase domain LTI model

Fig. 5.1(a) shows a typical PLL composed of phase detector, a loop filter with the transfer function, H(s), a voltage controlled oscillator (VCO), and a frequency divider denoted as /N. The phase detector output is proportional to the phase difference between its two inputs. One input V_{in} is from the reference input signal, usually from the low phase noise crystal oscillator, the other is from output of frequency divider whose frequency is 1/N of the VCO output V_{out}. Under

the locked condition, the negative feedback adjusts the dc value of the VCO control voltage in such a way that the two inputs of the phase detector have constant phase deference and hence are at exactly the same frequencies. For this to happen, the VCO output frequency has to be N times larger than the input frequency.

Properties of the PLL in the locked condition can be analyzed using the equivalent phase-domain linear time-invariant (LTI) model shown in Fig. 5.1 (b). K_{PD} is the gain of the phase detector in volts/radian, and K_{VCO} is the VCO gain in Hz/volts. Because phase is the integral of the frequency and the VCO output frequency is proportional to the control voltage, the VCO works as an ideal integrator when the output is phase. Therefore its frequency response is $K_{VCO/S}$. The frequency divider divides the VCO output phase by N, so is modeled as an attenuator of a factor of N in phase domain. The phase domain transfer function for the PLL is :

$$\frac{\phi_{out}}{\phi_{in}} = \frac{NK_{PD}K_{VCO}H(s)}{Ns + K_{PD}K_{VCO}H(s)} \tag{5.1}$$

Usually VCO phase noise dominates the out of the band phase noise and input phase noise dominates the in band phase noise. The other components such as frequency divider, phase detector and charge pump, contribute relatively much less phase noise to the whole loop [18].

In order to simplify the analysis, we consider two specified cases: first order loop and higher order loop.

5.2.1. First Order Loop

In a first order loop, there is no explicit loop filter, that is, H(s)=1, we have:

$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{s + K_{PD}K_{VCO}} = \frac{1}{1 + \frac{s}{\omega_{loop}}} \tag{5.2}$$

where $\omega_{loop} = K_{PD}K_{VCO}$ is the loop bandwidth.

It is very clear that in a first order loop, the only way to reduce phase noise is to increase the loop bandwidth.

5.2.2Higher Order Loop

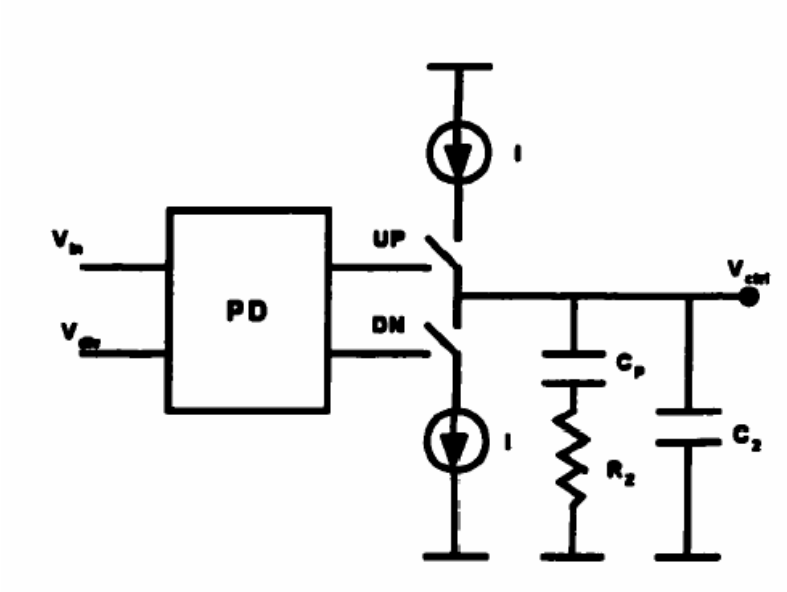


Fig. 5.2 Higher order loop

For first order loop, we can see from (5.2), there is a strong coupling between the bandwidth and the steady phase error. To overcome this, we need to increase the order of the loop. As shown in Fig. 5.2, a filter is introduced in the forward path of the loop. The static error does not disappear unless an extra ideal integrator is also introduced in the forward path. The static phase error can be eliminated by introducing a pole at the origin.

In the charge pump PLL, the phase detector has two edge-sensitive inputs and two outputs called UP and DN. If the VCO runs at a lower frequency than the input, the UP signal will be dominant. This will inject charge into the charge pump capacitor, C_P, which in turn results in an increase in the out put control voltage V_{ctrl}, to adjust the VCO frequency. As long as the dynamics of the loop are much slower than the signal, the charge pump can be treated as a continuous time integrator. Usually a zero is introduced by adding a resistor in series with the charge pump capacitor to improve the stability of the loop. If the two inputs do not have the right relationship, the output voltage grows without bound. Therefore, there is no static phase error can persist under lock condition. Two integrations in the forward path guarantee zero phase error of the loop. We can see that PD/CP architecture has two advantages over the low pass architecture, one is zero steady-state phase error, and the other is the larger capture range limited by the VCO tuning range.

Fig. 5.2 is valid for PD/CP PLL as long as CP switches much faster than the loop dynamics. The combined PD/CP and loop filter transfer function is:

$$K_{CP}H(s) = \frac{I}{2\pi C_p}.\frac{f_Z s + 1}{s} \tag{5.3}$$

where $f_Z = \frac{1}{R_Z C_P}$ is the zero frequency. From (3.1) and (3.3),

$$\frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{(f_Z s + 1)N}{1 + f_Z s + \frac{s^2}{\frac{IK_{VCO}}{2\pi N C_P}}} \tag{5.4}$$

This is the transfer function versus frequency. And the x-axis is the offset frequency from carrier when we look at the voltage power spectrum [19]. The transfer function is about N when

offset frequency is small, and is about $\frac{IK_{VCO}f_Z}{2\pi C_P\omega}$ when offset frequency is very high. The PLL transfer function is shown in Fig. 5.3.

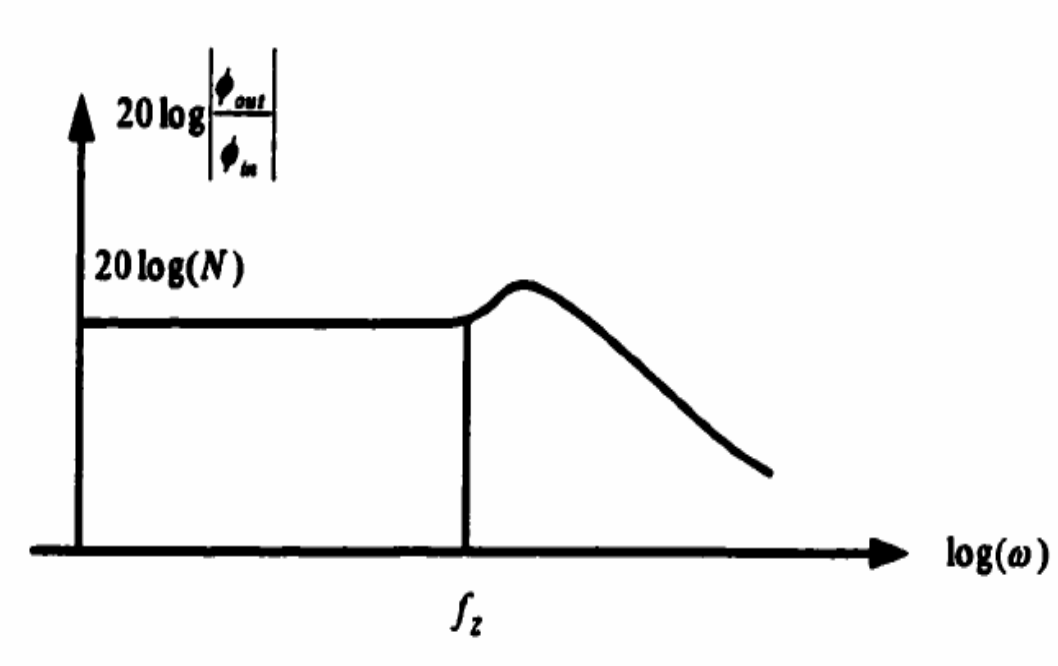


Fig. 5.3 Transfer function of a higher order PLL.

5.2.3 Noise Properties of PLL Blocks

In order to study the noise properties of the PLL, we need to briefly discuss the noise properties of the PLL blocks.

(1) VCO Noise

It is possible to reduce VCO noise using amplitude enhancement and symmetry

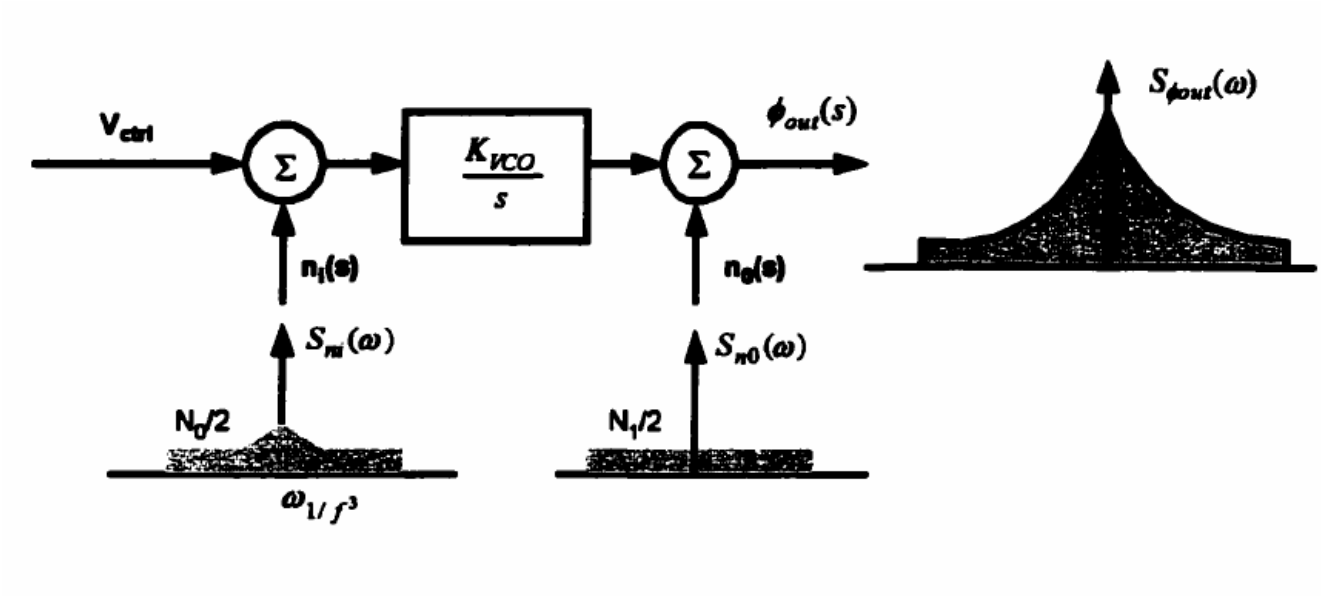


Fig. 5.4 Noise model for VCO

adjustment techniques.

The VCO noise can be modeled using a noiseless VCO with an additive noise source at its input and output, as shown in Fig. 5.4. The input source, $n_i(s)$, has white and 1/f noise that will generate $1/f^2$ and $1/f^3$ regions in the output because VCO works as an ideal integrator. The output added source, $n_o(s)$, models the output noise floor.

The output PSD can be calculated using (5.5)

$$S_{\phi out}(\omega) = \frac{K_{VCO}^2}{\omega^2} S_{ni}(\omega) + \frac{N_1}{2} \tag{5.5}$$

And (5.5) can be shown as:

$$S_{\phi out}(\omega) = 2\frac{N_0 K_{VCO}^2}{\omega^2}(1 + \frac{\omega_{1/f^2}}{\omega}) + \frac{N_1}{2} \tag{5.6}$$

where ω_{1/f^2} is the flicker noise corner of the input noise source $n_i(s)$ and equal to $1/f^3$ noise order of VCO, which is smaller than the actual device 1/f noise order.

It should be noted that the spectrum of the output voltage is related to the spectrum of the phase through a non-linear phase modulation. Therefore, the spectrum of the output voltage will not grow without bound.

(2) Frequency Divider Noise

Frequency divider may have a significant contribution to the total loop phase noise depending on the implementation. If an input is $\cos[\omega t + \phi(t)]$, and is applied to an ideal 1/N frequency divider, the output will have a fundamental component of $\cos[\omega t / N + \phi(t) / N]$. Apparently, an ideal frequency divider reduces the phase noise by a factor of 20 log (N). However, it does not reduce the noise floor induced bye thermal noise because thermal noise is not included in the discussion above.

The actual frequency divider, however, introduce excess noise to the loop. Digital counters, the important blocks to implement frequency dividers, can introduce significant additive noise in the form of white and flicker noise [20] [21]. A frequency divider can't directly introduce integrated noise ($1/f^2$ and $1/f^3$ noise) because its noise sources are outside of the feedback loop of the VCO.

Synchronization frequency dividers are less noisy than asynchronization frequency dividers because the noise can't accumulate from stages of counters.

(3) Phase Detector Noise

Phase detectors can be designed to contribute very small noise to the PLL because they are operated in lower frequencies. Usually, phase detector is not a major source of noise in a PLL .

5.3 LC Oscillator analysis

5.3.1 Tank Amplitude

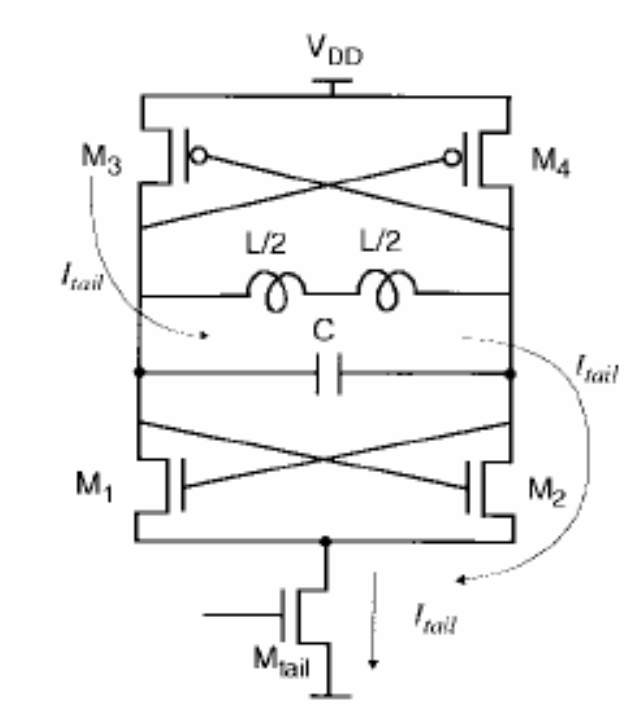


Fig. 5.5 Current flow when the stage is switched to one side.

Tank voltage amplitude has an important effect on the phase noise, as emphasized by the presence of $q_{\max}$ in the denominator of the expression for the single-sideband phase noise [22]:

$$\Im(\Delta\omega) = 10.\log_{10}\left(\frac{\overline{i_n^2}/\Delta f}{q_{\max}^2}\cdot\frac{\Gamma_{rms}^2}{2\omega^2}\right) \tag{5.7}$$

where $\overline{i_n^2}/\Delta f$ is the power spectral density of the parallel current noise, Γ_{ms}^2 is the rms value of the impulse sensitivity function (ISF) associated with that noise source, $q_{\max}$ is the maximum signal charge swing, and $\Delta\omega$ is the offset frequency from the carrier.

A simple expression for the tank amplitude can be obtained assuming that the current in the differential stage switches quickly from one side to another. Fig. 5.5 shows the current flowing in the complementary cross-coupled differential *LC* oscillator [23] when it is completely switched to one side. As the tank voltage changes, the direction of the current flow through the tank reverses. The differential pair thus can be modeled as a current source switching between I_{tail} and $-I_{tail}$ in parallel with a resistance–inductance–capacitance *(RLC)* tank, as shown in Fig. 5.6. R_{eq} is the equivalent parallel resistance of the tank.

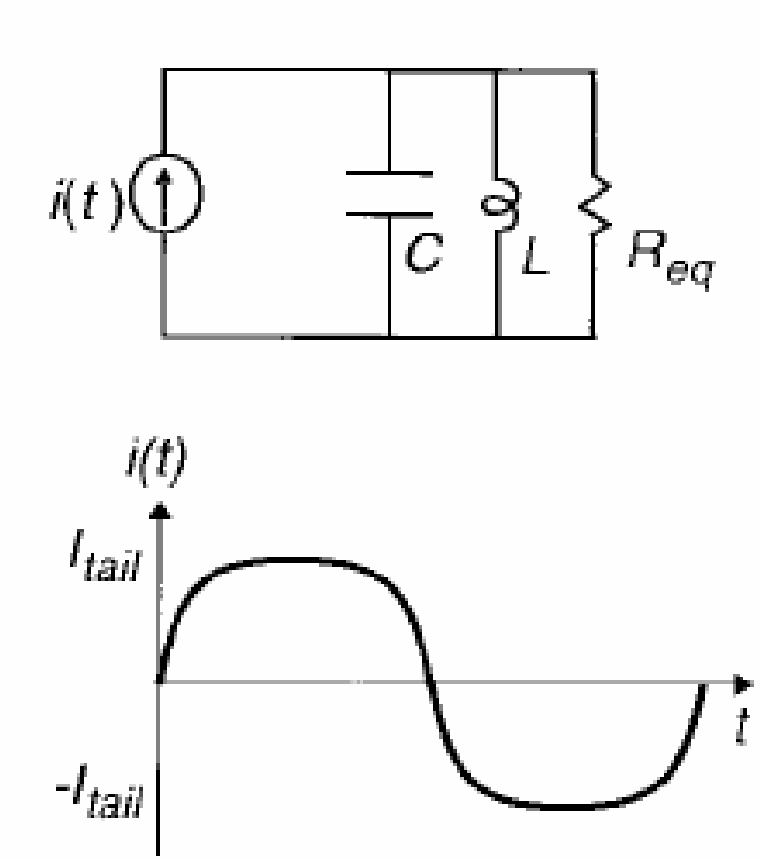


Fig. 5.6 Differential equivalent circuit

At the frequency of resonance, the admittances of the L and C cancel, leaving R_{eq} Harmonics of the input current are strongly attenuated by the LC tank, leaving the fundamental of the input current to induce a differential voltage swing of amplitude $(4/\pi)I_{tail}R_{eq}$ across the tank if one assumes a rectangular current waveform. At high frequencies, the current waveform may be approximated more closely by a sinusoid due to finite switching time and limited gain. In such cases, the tank amplitude can be better approximated as

$$V_{\tan k} \approx I_{tail}R_{eq} \tag{5.8}$$

This mode of operation is referred to as the *current-limited* regime of operation since, in this

regime, the tank amplitude is solely determined by the tail-current source and the tank equivalent resistance.

5.3.2 Gate Oxide Breakdown on Oscillator

A differential LC voltage controlled oscillator (VCO), as shown in Fig. 5.7, is evaluated for gate oxide breakdown. An inductor with a finite quality factor (Q of 10) and a pair of transistors used as varactors make the LC tank. The nMOS transistors used for the varactors have the same sizes as the measured devices. The smallest possible active transistors to support a sustained oscillation are used to ensure that the capacitance for the LC tank mainly comes from the varactors. The capacitance of a varactor and the control voltage V_{ctr} has a nonlinear relationship [24][25]. Nevertheless, the value of the control voltage determines the tank capacitance, and hence the frequency of oscillation by:

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}. \tag{5.9}$$

The BSIM3v3 model of a fresh transistor used for the simulation is extracted from the DC measurements performed by the semiconductor parameter analyzer along with the BSIMpro software. Transient simulation is performed using the fresh transistor model and the frequency of oscillation is found 4.9 GHz. Using (5.9) the value of the gate capacitance of the varactor transistor is 104 fF. The gate capacitance of a fresh device is found 105 fF by the capacitance extraction procedure presented in Chapter 2. Thus, the procedure is verified.

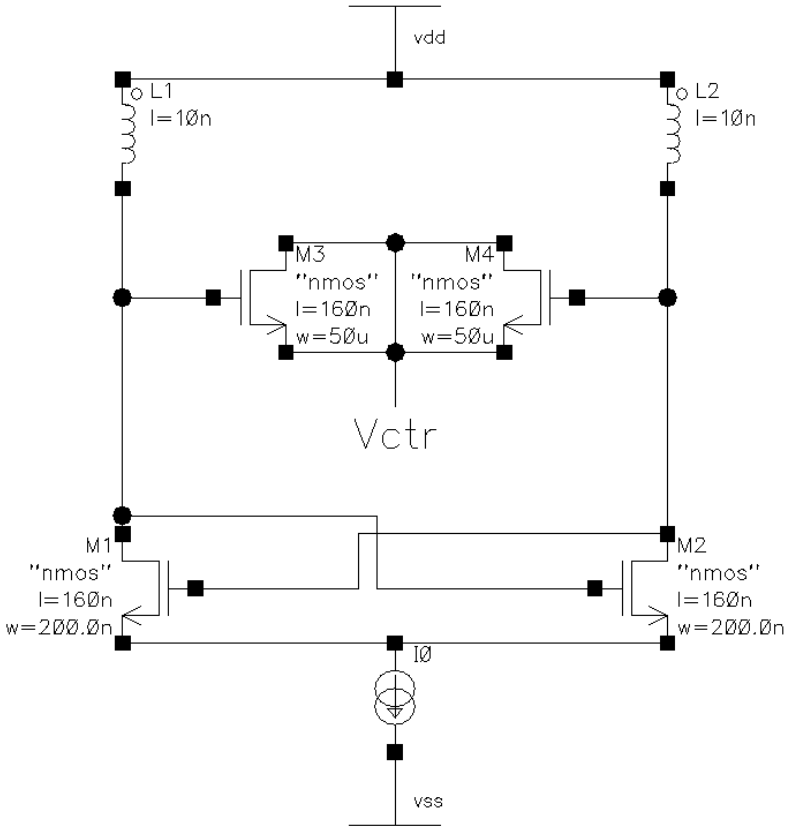


Fig. 5.7: Oscillator used for simulation.

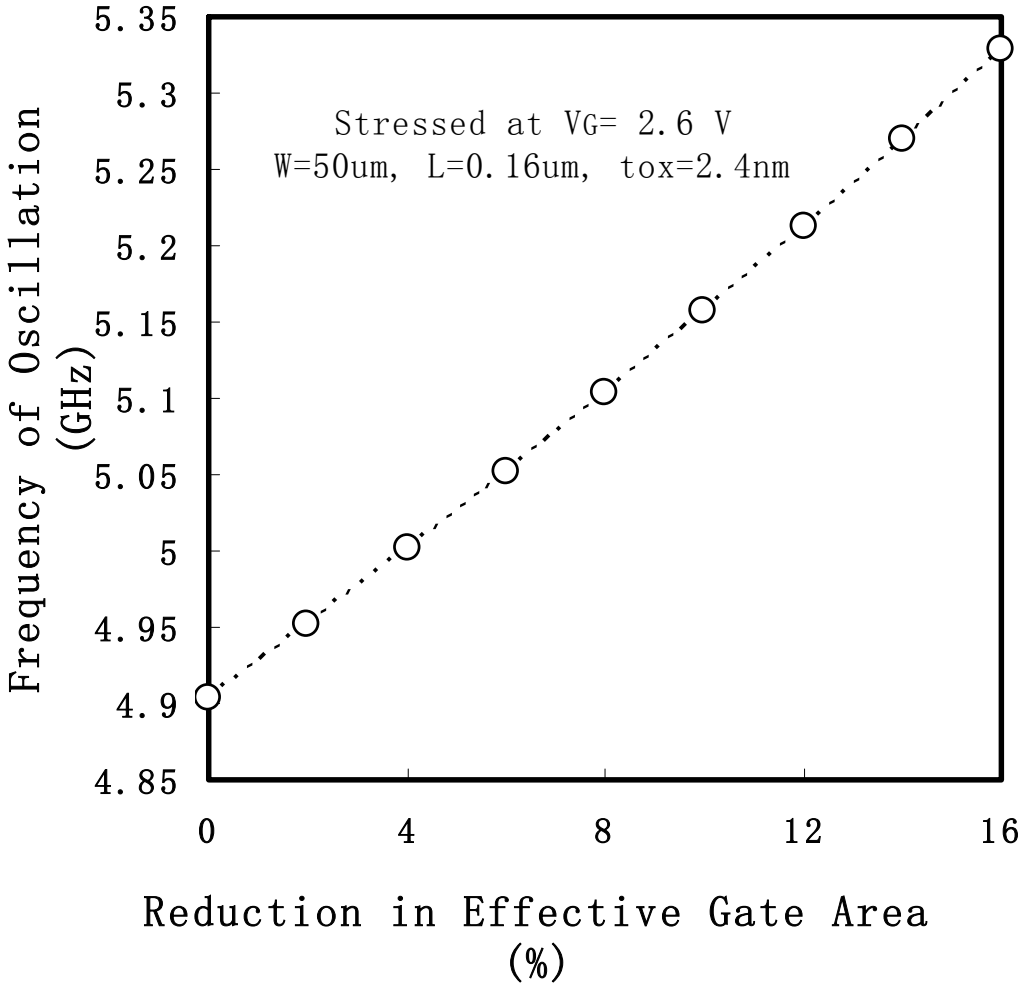
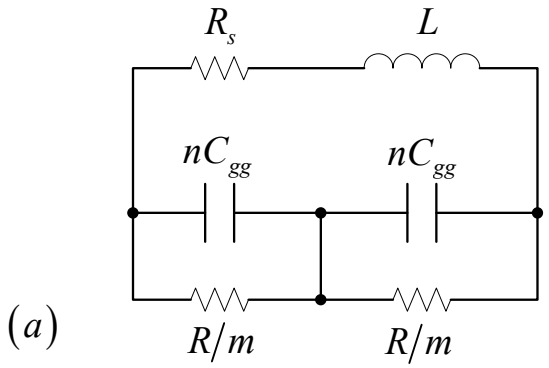


Fig. 5.8: Frequency of oscillation versus reduction in effective gate area.

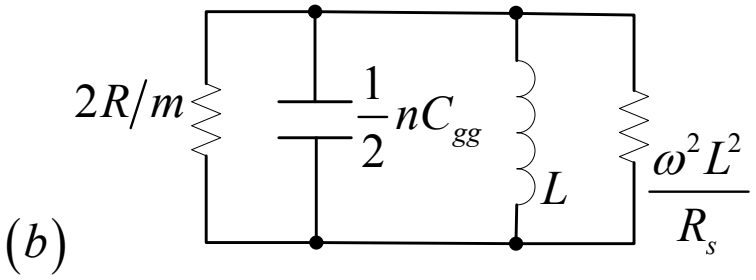
The VCO supply voltage is 2 V and the DC bias across the varactor is also about 2 V. An oscillator is usually designed to have a high amplitude of oscillation for a superior performance of a mixer in the following stage. It also keeps the phase noise of the oscillator low. However, the increased amplitude of oscillation and the high gate bias voltage put the MOS varactors under increased stress, which may trigger the gate oxide breakdown. The oxide breakdown has twofold effects on the varactors; it reduces the MOS capacitance and deteriorates its quality

factor due to increased oxide conductance. The BSIM3 model for the transistors obtained by BSIMPro software through DC measurements under different stress conditions do not account for capacitance change after breakdown. Here, 'wwl' in the BSIM3 model is used to account for such capacitance reduction effect. The parameter 'wwl' is otherwise unused in our simulation. The decrease of gate capacitance due to a decrease in the effective gate area increases the frequency of oscillation as shown in Fig. 5.8. Negative supply voltage of V_{SS} is used as V_{ctr} during the simulation.

It is common to layout a big transistor with multiple fingers. Since the number of conducting paths due to the soft breakdown is a statistical phenomenon, let us assume that some m fingers out of total n are broken in a varactor transistor. R is the resistance parallel to the breakdown finger. R_s is the resistance in series with the inductor L due to its finite quality factor. Therefore, the LC tank can be modeled by Fig. 5.9(a). Through impedance transformation the equivalent tank is obtained in Fig. 5.9(b).



(a)



(b)

Fig. 5.9: (a) The LC tank, and (b) its equivalent circuit

Thus, the equivalent parallel resistance of the tank is

$$R_{eq} = \frac{2\omega^2 RL}{m\omega^2 L^2 + 2RR_s}. \tag{5.10}$$

As the number of breakdown fingers increases, the oscillator operates in current limited region, and its amplitude of oscillation is given by [26]:

$$V_m = I_{tail} R_{eq} = \frac{2I_{tail}\omega^2 RL}{m\omega^2 L^2 + 2RR_s} \tag{5.11}$$

The phase noise of the oscillator can be expressed by the Leeson's model [27] as

$$\Im(\omega_m) = \frac{1}{V_m^2} \cdot \frac{kT}{C} \cdot \frac{\omega_0}{Q} \cdot \frac{1}{\omega_m^2} \tag{5.12}$$

If the breakdown spot resistance due to soft breakdown is in the order of MΩ, the simulation results show that it has very little effects on the amplitude of the oscillation. However, as the hardness of breakdown increases, this resistance can be as low as few kΩ [15]. As a consequence, the amplitude decreases and the phase noise deteriorates significantly according to (5.11). Simulations have been performed to evaluate the amplitude and the settling time of the oscillator with different numbers of fingers experiencing breakdown. Simulation results are summarized in

Table 5.1. Five 10 μm fingers for the varactor transistor and a 10 kΩ breakdown spot resistance for a broken finger are used for simulation.

Table 5.1: Effects of decreased R_0 on oscillator performance

Number of Fingers Breakdown	Amplitude (V)	Settling Time (nS)
Fresh	2.10	4.14
1	1.73	4.73
2	1.43	5.76
3	1.17	7.97
4	0.95	12.22
5	0.74	31.60

5.4 Conclusion

In chapter 4 and 5, the impact of SBD stress on the CMOS RF device has been examined using 0.16 μm CMOS technology. The analytical equation of cutoff frequency including the gate

oxide breakdown is derived. SBD stress reduces the cutoff frequency and total gate oxide capacitance of MOS transistors. SBD spot resistance and total gate capacitance are extracted from the measured S-parameters and then verified with the SpectreRF model file. The decrease in gate capacitance results in an increase in frequency of oscillation of an LC oscillator, and breakdown has significant effect on the amplitude of oscillation.

CHAPTER SIX: NBTI EFFECTS ON RF PERFORMANCE

6.1 Introduction

With the smaller dimensions for each successive generation of transistors for improving speed and functionality, the higher power dissipation, which results in heat flux to be removed to the ambient, is required. Using MEDICI simulation, the temperature at the gate-drain opening for the bulk devices was estimated to be 315 K [37]. While for the silicon-on-insulator devices, the simulated temperature was up to 550 K. The packaging and surrounding environment also affect the operation temperature of devices in the real case. One of the major temperature-induced reliability issues for p-channel MOSFET is the negative bias temperature instability (NBTI), which is caused by the interface traps and fixed charge under high temperature and negative gate voltage bias. Besides the NBTI effects, the pMOS in real circuits also suffers from gate oxide breakdown (BD) due to high vertical field in the oxide and hot carriers injection (HCI) because of high lateral field in short-channel MOSFETs, when the application of high voltages to the drain of device [38]-[42]. The combined NBTI, BD and HCI effects cause significant degradation in our experiments. And also the RF performance degradation due to stress should also be considered.

Even though much is known about the NBTI effects on the device characteristics, little is known of the interaction of NBTI with SBD and HCI, especially the impact on RF performance. In this dissertation, the effects of NBTI, SBD, and HCI have been analyzed. A model has been developed to evaluate the degradation. The NBTI with SBD, as well as NBTI with SBD and HCI, have been examined experimentally. Measured performance, as well as the simulated results

obtained from Spectre-RF simulation with the developed models, is presented. Combined NBTI, SBD, and HCI effects on circuit are investigated. A summary is given finally.

6.2 NBTI effect induced gate oxide breakdown

6.2.1 NBTI physics

In NBTI physics, the overall electrochemical reaction at Si-SiO_2 interface is [43]:

$$\mathrm{Si-H+O_3-Si-O-Si+h^+ \leftrightarrow Si\square+O_3-Si-OH^+-Si} \tag{6.1}$$

The interface state (Si·) is generated from the dissociation of hydrogen terminated trivalent Si bonds (Si-H) by holes (h^+) in the Si inversion layer. The released hydrogenated species (H^+) diffuse and are trapped near the oxide interface resulting in the positive oxide charges (Si-OH^+-Si). Experiments show that the positively charged hydrogen (H^+) reacts with the SiO_2lattice to form an OH group bonded to an oxide atom [44], leaving a trivalent Si atom (Si_0^+) in the oxide and one trivalent Si_s at the Si surface. The Si_0^+ forms the fixed positive charge (N_{OT}) and the Si_s forms the interface trap (N_{IT}). NBTI stress causes N_{IT} and N_{OT} shifts, contributing mainly to the shift in device characteristics. The N_{IT} and N_{OT} charge shifts are given by:

$$\Delta N_{IT}(E_{ox},T,t,t_{ox}) = 9\times10^{-4} E_{ox}^{1.5} t^{0.25} \exp(-0.2/kT)/t_{ox} \tag{6.2}$$

$$\Delta N_{OT}(E_{ox},T,t) = 490 E_{ox}^{1.5} t^{0.14} \exp(-0.15/kT) \tag{6.3}$$

where E_{ox} is the electric field in the oxide, T is temperature, t is stress time, t_{ox} is the thickness of oxide, k is the Boltzmann constant. The NBTI degradation is thermally activated (See Eqs. (6.2)

and (6.3)) and, therefore, is sensitive to temperature. It degrades more severe under higher temperature. From equation (6.2), it is seen that the trapped charge increases with time and they can weaken Si-O and Si-Si bonds in SiO_2, serving as precursors bond sites that can be broken during stress.

6.2.2 Measurement results and discussion

The tested devices are 0.16×10 μm^2 LDD pMOSFETs with 24 Å oxide thickness. In our experiments, many transistors are tested to verify the physical effect. The wafer was tested with a Cascade 12000 Probe Station. Agilent 4156B Precision Semiconductor Parameter Analyzer was used for dc biasing and *I-V* characteristics measurement. Thermo-Chuck TP0315 was used to set the test temperature. The BSIM3 models are extracted by BSIMpro software at different temperature. The oxide breakdown voltage was first determined from the voltage ramp test. It was found that the breakdown voltage was about -3 V. For the NBTI-BD stress (NB), the gate-source stress voltage is –2.6 V and the drain is grounded. The source and bulk are grounded. The test temperature is set at 300K and 400K, respectively. The gate current was monitored and recorded with a computer-controlled test system. As long as the gate current reached the threshold value set beforehand, the stress will be interrupted automatically so that various transistor parameters can be measured. On-wafer measurements were implemented on the same device before and after stress at different temperature.

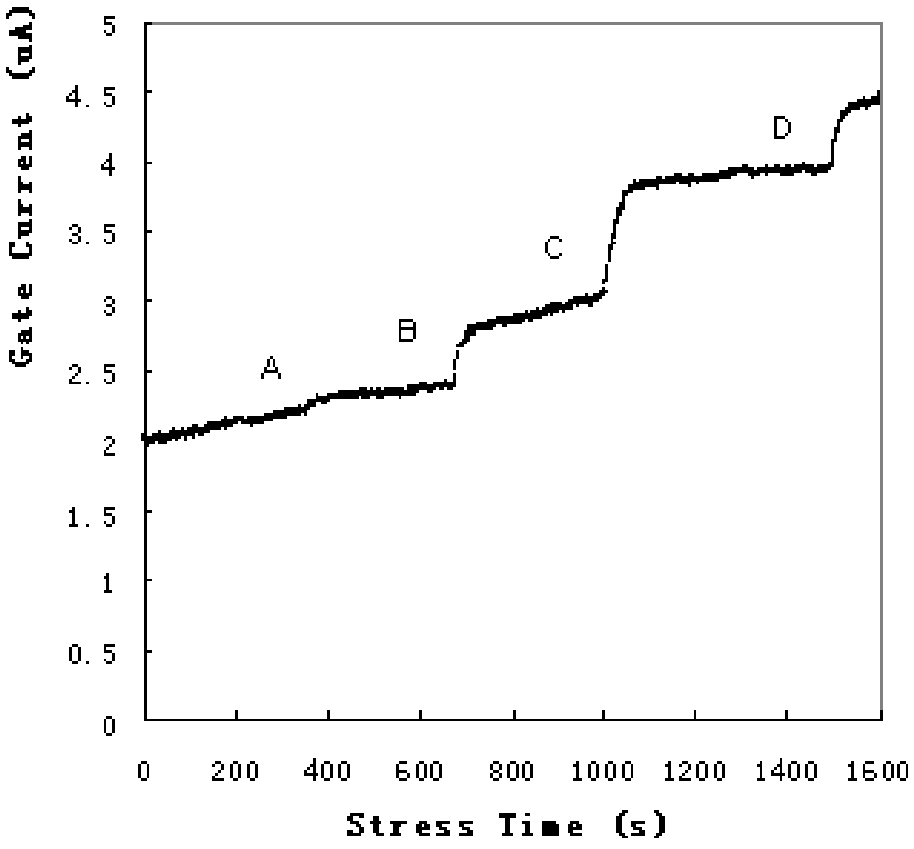


Fig. 6.1 Gate current evolution as a function of stress time

In Fig. 6.1, the gate current evolution as a function of stress time is shown. Multiple SBD events occur when the stress is stopped at A, B, C and D, respectively. The interface and oxide traps density are tracked by top-emitter direct current DCIV method [45-47]. The base and collector currents I_B and I_C versus V_G at $V_{pn} = 0.4$V are measured before stress and at each transit point (A, B, C, and D). The measured DC recombination current I_B flowing in the body terminal comes from the electron-hole recombination at the SiO_2/Si interface traps under the gate. The peak recombination current due to the recombination at a discrete interface trap level with a

density N_{IT}, based on the SRH recombination is given by

$$\Delta I_B = A_G q(n_i / 2)(c_{ns} c_{ps})^{1/2} \exp(V_{PN} / 2kT) N_{IT} \tag{6.4}$$

Since ΔV_{G-FB} is very sensitive to $\Delta N_{IT} + \Delta N_{OT}$, combing $\Delta I_B - V_G$ and $\Delta I_C - V_G$ the change of oxide charges ΔN_{OT} is then obtained,

$$\Delta N_{OT} = -(C_o / q)\Delta V_{G-FB} \tag{6.5}$$

where C_o is the oxide capacitance, and ΔN_{OT} is the stress-induced trap density. The prestress oxide charge density in the high-quality SiO_2 gate oxide is negligible, hence $\Delta N_{OT} \cong N_{OT}$. By using (6.4) and (6.5), ΔN_{IT} and ΔN_{OT} are thus available.

Fig. 6.2 shows the time dependence of the oxide and interface trap charge growth. For the first about 400 s, a negative oxide charging is observed. It can be explained that the reversal of the trapped oxide charge polarity during the stress is expected since, for the negative stress the gate current is dominated by the tunneling of the valence electrons from the p^+ polysilicon gate through the oxide, which is much larger than the hole current tunneling from the inverted *p*-type channel of the *n*-type substrate. Therefore, the generation rate for the negatively charged defects is larger than that for the positively charged effects. The large net positive oxide charge observed at long stress time suggests that there is a saturation value of density for these two kinds of defects, and the saturation value for the positively charged defects is larger. From Fig. 6.1 and Fig. 6.2, simultaneous sharp steplike increase in I_G and N_{OT} at A, B, C and D can be observed. Thus, a correlation between the abrupt change in I_G and N_{OT} is expected. The reason is that the thermally-excited carrier injected into the oxide weakened the bonds in SiO_2, thus triggering more SBD. SBDs at A, B, C and D change the distribution of the oxide field under the gate, leading to a nouniform trapping and recombination conditions under the gate. It significantly

changes the density of oxide trap charge. The N_{IT} dependence on the stress time shows a jump at about 1300 s, but there is no corresponding jump in I_G. Compared to some other experiments conducted under room temperature, it can be seen the time to breakdown in this experiment is much shorter than those of other experiments. It can attribute to the elevated temperature in this experiment.

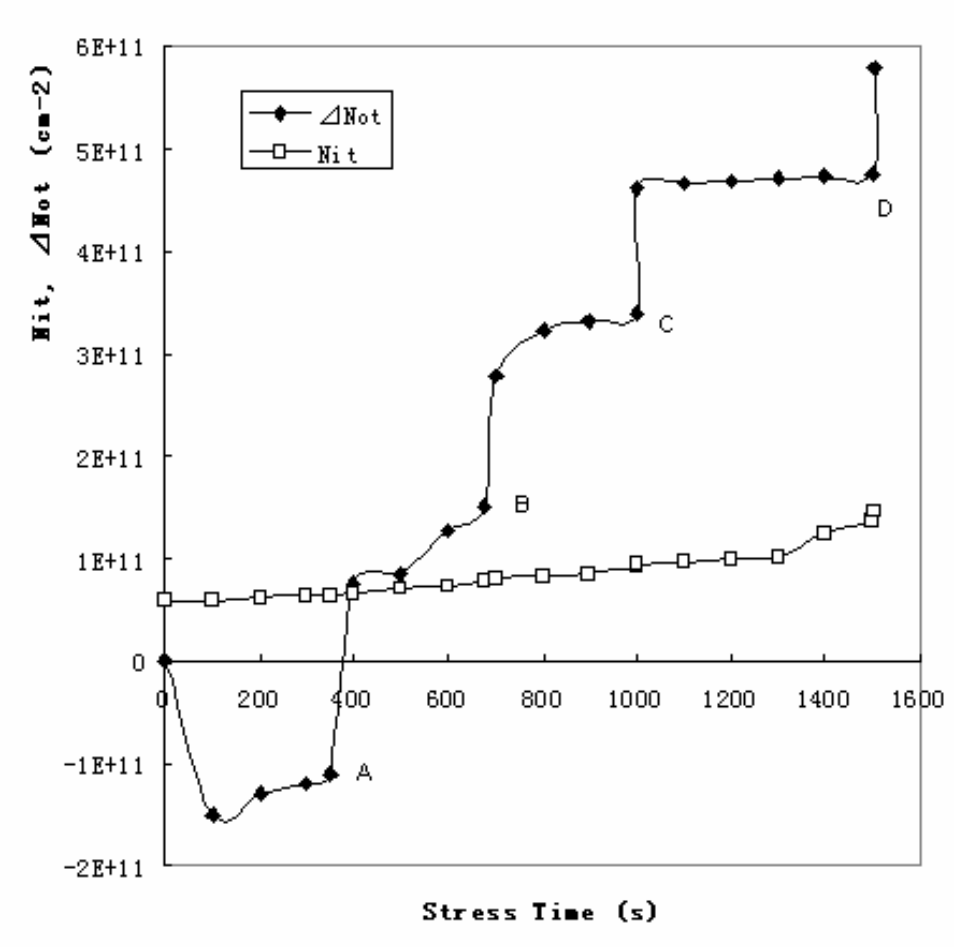


Fig. 6.2 The evolution of oxide and interface trap densities as a function of stress time

6.2.3 Analysis and Modeling

6.2.3.1 Energy band diagram of temperature-activated oxide trap charging

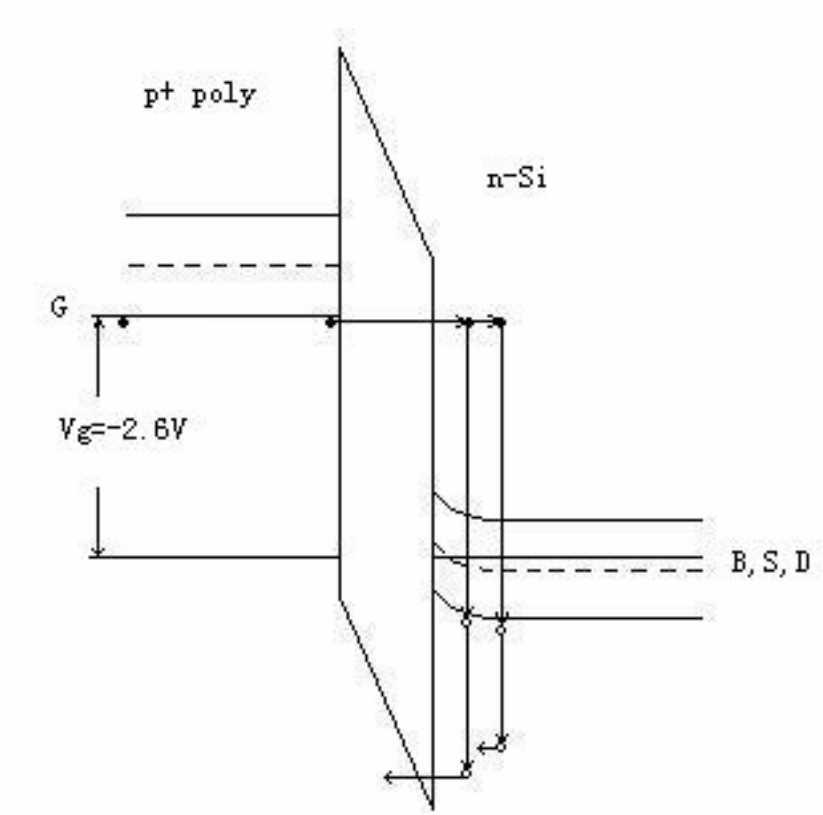


Fig. 6.3 Energy band diagram for p-MOSFET with *p*+ polysilicon gate biased at V_G=-2.6 V (T=400K).

In Fig. 6.3, the energy band diagram for p-MOSFET with gate biased at V_G=-2.6 V (T=400K) is shown. In this case, the gate current is dominated by the valence electrons tunneling from the *p*+ polysilicon gate into the inverted *p*-type channel of the *n*-type substrate. The hot holes in the *p*-type inversion channel layer can be generated by the injected electrons, and then they can be back injected into the SiO_2. It is proposed that the main mechanism responsible for hot hole generation is Auger process [48]. Due to the elevated temperature, the bandgap of

substrate decreases, which results in the higher probability that more hot holes can be excited and accelerate the NBTI process, leading to more oxide charging which triggers further breakdowns.

6.2.3.2 TTF analysis

Using the model proposed in [48], assume a percolation cell weakened by the NBTI induced trapped charge will make *vdt* attempts to break the bond, where *v* is the temperature dependent lattice vibration frequency. The differential number of broken bonds in the interval *dt* in the gate area A_G can be written as

$$\begin{aligned} dN(t) &= \nu A_G P \Delta N_{OT}(t) dt \\ &= \nu A_G \Delta N_{OT}(t) \exp(-\varepsilon_A / kT) dt \end{aligned} \tag{6.6}$$

where $P = \exp(-\varepsilon_A / kT) = \exp(-(E_A - \gamma E_{ox}) / kT)$ is the bond breaking probability, $\Delta N_{OT}(t)$ is the NBTI stress-induced oxide trap density at time t. For the device used here, the thickness of gate oxide is 24 Å, which is around the size of an effective percolation cell that can form a conducing path [49]. Therefore, only one broken percolation cell is necessary to trigger breakdown in the gate oxide, thus leading to a unity of integration of $dN(t)$ from $t_{stress} = 0$ to TTF (Time to Failure),

$$1 \cong \int_0^{TTF} \nu A_G \Delta N_{OT}(t) \exp(-\varepsilon_A / kT) dt \tag{6.7}$$

Substituting (6.5) into (6.7) yields

$$\begin{aligned} 1 &\cong 490 \int_0^{TTF} \nu A_G E_{ox}^{1.5} t^{0.14} \exp(-0.15 / kT) \exp(-\varepsilon_A / kT) dt \\ &= 490 E_{ox}^{1.5} \nu A_G \exp((-0.15 - \varepsilon_A) / kT) \frac{TTF^{1.14}}{1.14} \end{aligned} \tag{6.8}$$

$$\ln TTF = 0.87(0.15 + E_A - \gamma E_{ox}) / kT - 1.32 \ln E_{ox} + C \tag{6.9}$$

where $C = -5.33 - 0.87 \ln \nu A_G$

The above equation reveals the relationship between lifetime and Electrical field.

6.3 NBTI and soft breakdown effect (NS) versus NBTI with breakdown and HCI (NSH)

6.3.1 NBTI with breakdown and HCI (NSH)

Constant high voltage at the drain terminal in real pMOS device results in hot carrier injection. The NBTI effect becomes stronger with negative gate bias, which accelerates thermally generated holes towards the Si/SiO_2 surface, thus increasing NBTI sensitivity.

In the Thermochemical-1/E model, the device BD lifetime due to voltage stress is given as:

$$\tau_{BD} = \mathrm{K} \exp(\frac{G}{E_{ox}}) \exp(\frac{Q}{\kappa_B}(\frac{1}{300K} - \frac{1}{T})) \tag{6.10}$$

where K is a constant, ΔH_0 is the enthalpy of activation (usually referred to as activation energy). γ is the field acceleration parameter. γ for each defect type alone has the expected $1/T$ dependence.

The lifetime of SBD is area dependent and temperature activated. The lifetime of HCs degradation due to DC stress is modeled by Mistry [41]:

$$\tau_{HC} = (\frac{1}{AT}\int_0^T I_b^m dt)^{-1} \tag{6.11}$$

where A are constants, T is the period of ac stress waveform, I_b is substrate current. m is empirical factors. I_b is temperature dependant:

$$I_b = I_d \frac{A_i \lambda}{\varphi_i}(V_d - V_{dsat}) \exp(-\frac{\varphi_i}{\lambda E_m + 3\beta kT/2}) \tag{6.12}$$

where A_i and β is the coefficients, λ is carriers' mean free path, φ_i is the energy required to generate electron-hole pair, E_m is the maximum channel electric field in the direction of the channel current I_d.

Based on [49], a model, which represents the stressed device behaviors, is developed and shown in Fig. 6.4. The equivalent circuit includes the terminal resistances (R_g, R_d, R_s), substrate network equivalent resistances (R_{db}, R_{sb}, R_{dsb}), overlap additional capacitances (C_{gd0}, C_{gs0}), junction capacitances (*Cdb, Csb*), and two inter-terminal resistances (*Rgd, Rgs*). The intrinsic transistor is a BSIM3v3 model extracted from the fresh or stressed devices using BSIMpro at different temperature. Agilent 4156B is used as the I-V meter. *Cgd0* and *Cgs0* account for part of the intrinsic capacitances that are not correctly modeled in the compact intrinsic BSIM3v3 model. The post-breakdown nMOSFET RF characteristics can be completely explained by the resistor-like behavior of the breakdown path - *Rgs* and *Rgd* are used to account for BD paths between the gate and the source, the gate and the drain, respectively [50]. They are extracted from the Ig-Vg curve of the stressed device. A fitting line is inserted in the Ig-Vg curve, the slope is *1/Rgs+1/Rgd* and the intercept at Y-axis is *–Vd/Rgd*. Other parameters are extracted from Y-parameters that were converted from measured S-parameters. *Rbsd* and *Csb* are obtained by optimizing the entire model to fit measured Y-parameters. In the BSIM3v3 model, the parameters are temperature dependent.

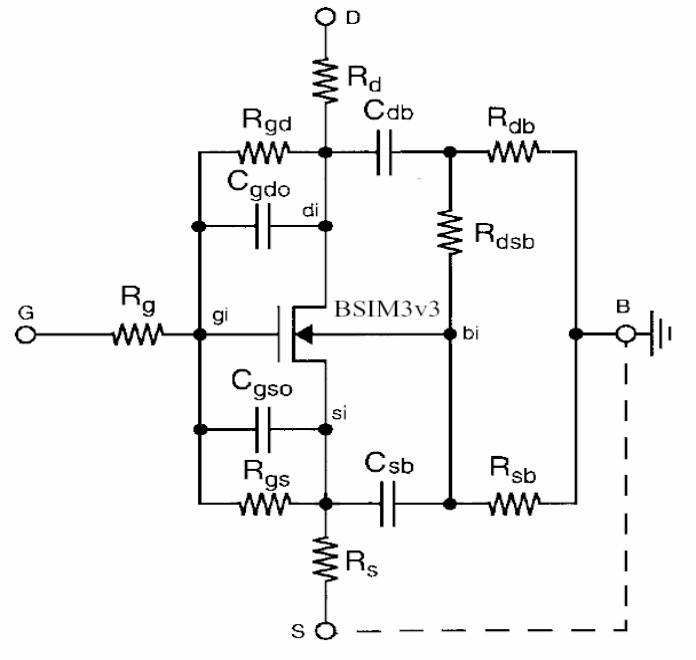


Fig. 6.4 Schematic of the sub-circuit model for a stressed RF MOSFET.

6.3.2 Experimental Work

The tested devices are 0.16×50 μm^2 LDD pMOSFETs with 24 Å oxide thickness. The wafer was tested in a Cascade 12000 Probe Station. Agilent 4156B Precision Semiconductor Parameter Analyzer was used for dc biasing and *I-V* characteristics measurement. S-parameters were measured up to 15 GHz using a HP8510 Network analyzer. The "open", "short", and "through" structures surrounding the device-under-test were used in this measurement for on-wafer parasitic de-embedding. The oxide breakdown voltage was first determined from the voltage ramp test. It was found that the breakdown voltage was about -3 V. Then, the gate-source and drain-source voltages were set at –2.8 V and –2.8 V respectively for the NBTI-SBD-HCI stress (NHS). While for the NBTI-SBD stress (NSS), the gate-source stress voltage was –2.8 V and drain was grounded. The source and bulk were grounded. Thermo-Chuck TP0315 was used to set

different test temperature (300, 320, 360, and 440 K). It has excellent temperature uniformity (± 0.5°C) of the chuck temperature over the entire temperature range. The gate current increased drastically after the device was stressed about 100 s at 300 K, which indicated the occurrences of gate oxide soft breakdown (SBD). While for higher test temperature, it took less time for the gate current to increase drastically (80 s for 320 K, 72 s for 360 K, 60 s for 440 K). Then, the stress was interrupted every 1800 s to measure various transistor parameters during dynamic at different temperature. On-wafer measurements were implemented on the same device before and after stress at different temperature. In the well-controlled experiments, many devices were measured and the results were averaged.

6.3.3 NSH and NS effects on MOSFET

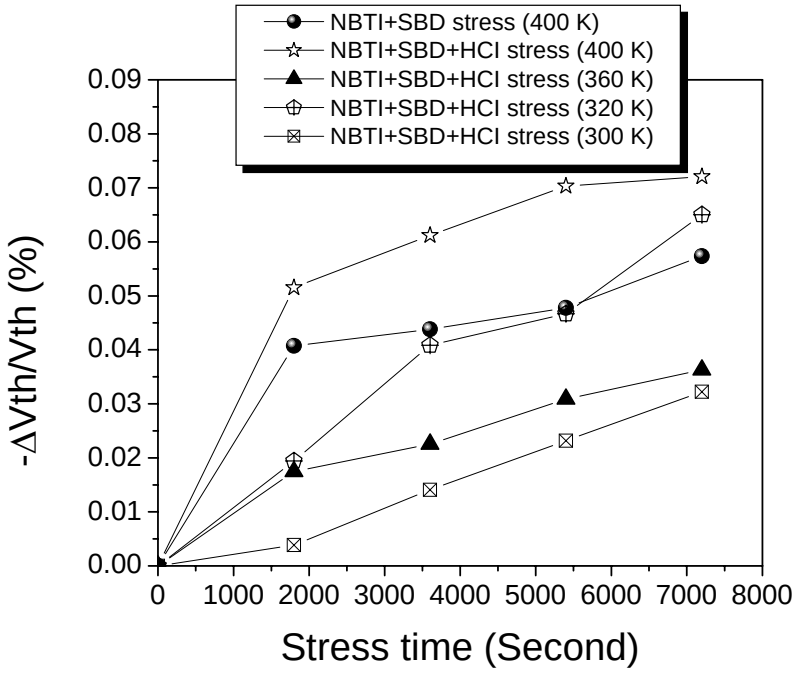


Fig. 6.5 (a) Threshold voltage degradation versus time

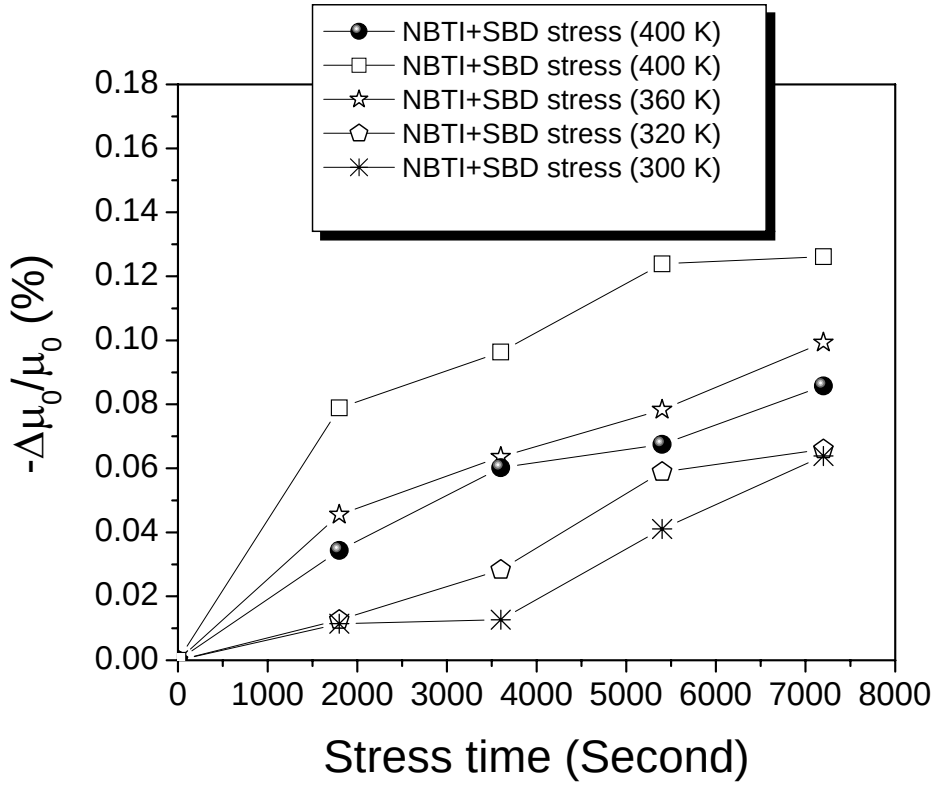


Fig. 6.5 (b) Mobility degradation versus time.

Even though much is known about the NBTI effects on the device characteristics, little is known of the interaction of NBTI with SBD and HCI, especially the impact on RF performance. Therefore, it is worth investigating the effects of NBTI, SBD, and HCI. The NBTI with SBD, as well as NBTI with SBD and HCI, have been examined experimentally. Measured performance, as well as the results obtained from Spectre-RF simulation with the developed model, will be presented here [58].

Fig. 6.5 displays the percentage change in threshold voltage (V_{th}) and mobility (μ) as a

function of stress time. For the NSH stress, the threshold voltage degradation increased with temperature and time. At 400K, the degradation due to NS stress is smaller than NSH stress. After 2 hours of stress, the threshold degradation is 7 % for NSH stress; while for NS stress, it is 5%. The mobility also showed the same tendency with time and temperature as threshold voltage. It reduces by 12.8 % after 2 hours of NSH stress at 400K, and 8% for NS stress at 400K.

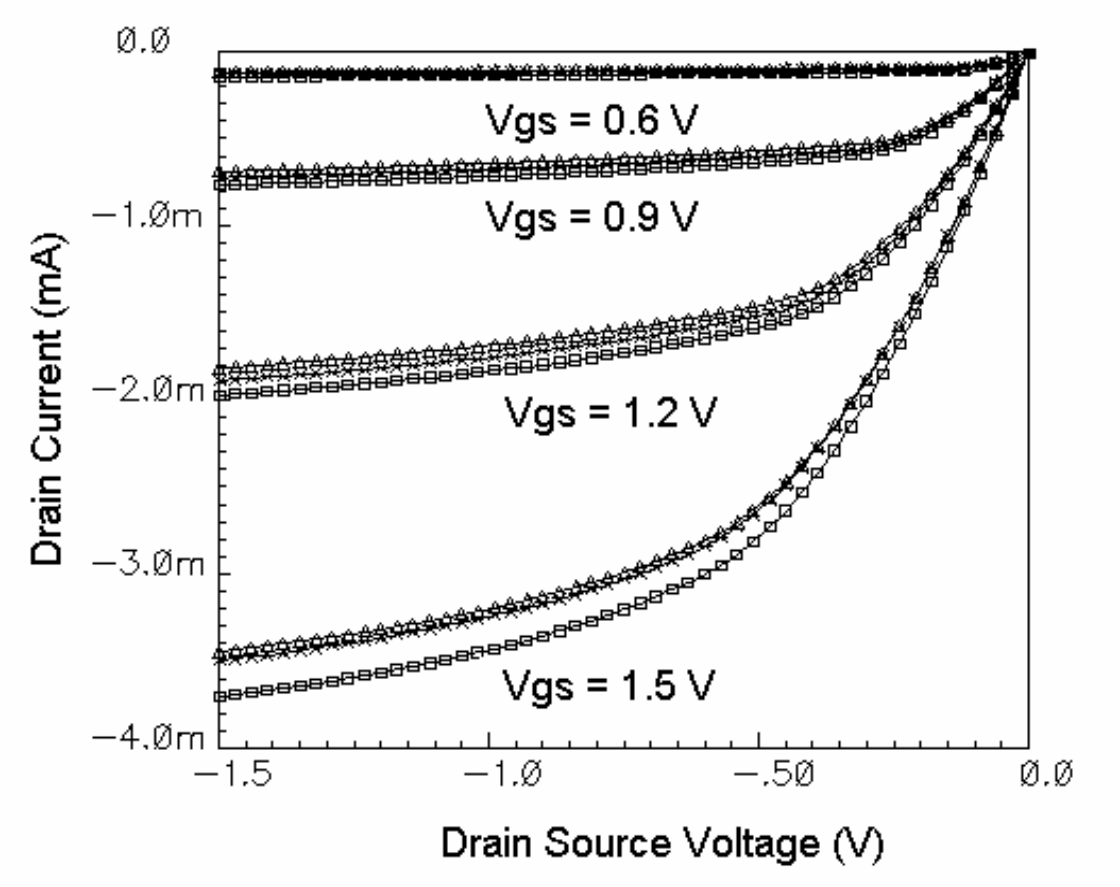


Fig.6.6 (a) I-V characteristics for fresh (□), NS stress (x), and NSH stress (Δ). All stress were performed at 400 K. Stress time is 7200 seconds.

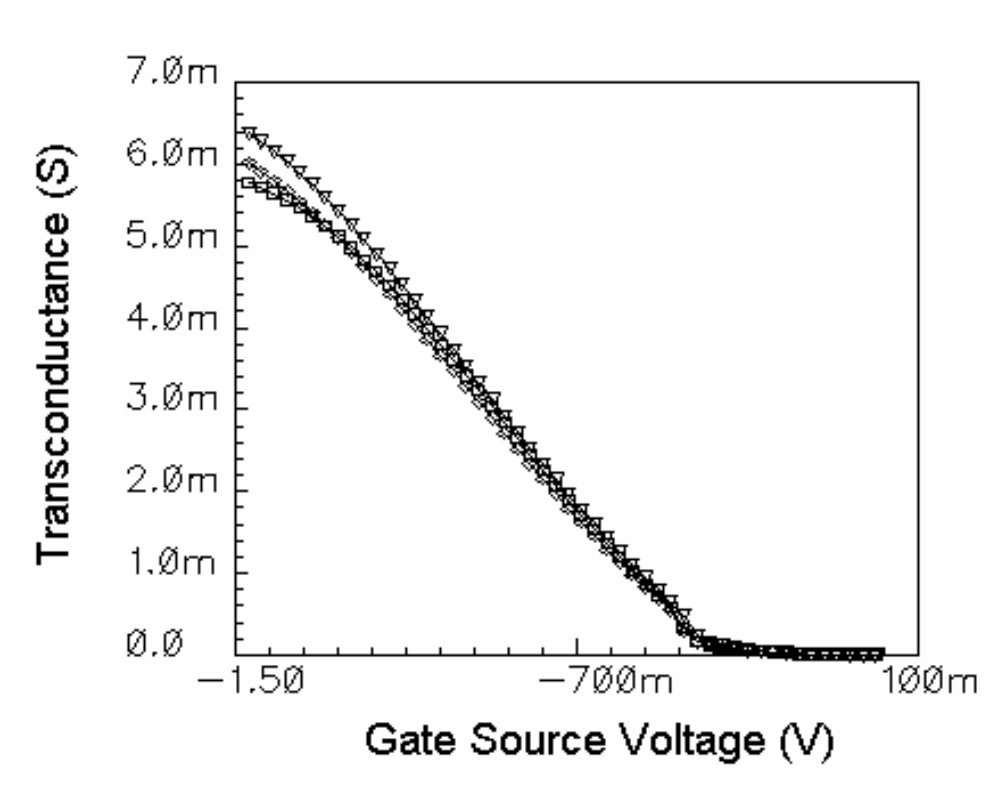


Fig.6.7 (b) Transconductance versus gate source voltage for fresh (□), NS stress (◊), and NSH stress (Δ). All stress were performed at 400 K. Stress time is 7200 seconds.

The drain current degradation is clearly visible in the device after NSH stress at 400 K for 2 hours, as shown in Fig. 6.7(a). All the curves shifted upward after stress. The transconductance degradation is shown in Fig. 6.7(b). From Figs. 6.6 and 6.7, we can see that the degradation due to NS stress is smaller than NSH stress at high temperature (400 K). The NSH degradation became more severe under higher temperature. The shift of S-parameters before and after NSH stress at 400 K for 2 hours is given in Fig. 6.8. The gate-source dc bias voltage for S-parameters measurement is -0.9 V and the drain-source voltage is set at -1.5 V. The devices are operated in the saturation region. It can see that all S-parameters changed.

The Y-parameters before and after stress are extracted from S-parameters. There is a

significant degradation for Y-parameters, and change in the RF model parameters is expected. The statistic average value for R_{gs} is 800 KΩ and R_{gd} is 66.5 MΩ. Before stress, R_{gs} and R_{gd} are suggested to be infinite. According to [49], the valid extraction region is up to 10 GHz. The mean values from 1 GHz to 10 GHz are selected as the extracted parameters. The extracted C_{gs} showes a significant change after stress, but C_{gd} changes slightly. R_g, R_s, and R_d do not change significantly. R_g is about 27 Ω, R_s and R_d are 6 Ω and 1.38 Ω, respectively. R_{bd} is approximately equal to R_{sb}; they are 100 Ω for the fresh device and 80 Ω after stress. Extracted C_{bd} changes from 163 fF to 187 fF after stress. For the fresh device, R_{bsd} and C_{sb} are 10 Ω and 380 fF. They are 8 Ω and 420 fF for the stressed device. By inspecting the extracted BSIM3v3 model files, it can be seen that many model parameters are adjusted to represent the stressed device behavior, including *Vth0, K1, K2, K3, U0, Ua, Ub, Uc, Voff, NFactor*, etc.

The extracted 'fresh' models, as well as 'stressed' models, are used in the simulation to evaluate the temperature accelerated stress induced degradation. Fig. 5 (a) gives the output power versus input power at V_{gs} = -0.9 V and V_{ds} = -1.5 V. A two-tone input (ω_1 = 5.0 GHz, ω_2 = 5.02 GHz) is used in simulation. Third-order input inter-modulation (IIP3) changes from 16.1594 dBm to 13.3857 dBm after NS stress under 400 K for 2 hours, and to 11.0938 dBm after NSH stress under 400 K for 2 hours. Figure 5(b) shows the noise figure (NF) for the source impedance of 50 Ω before and after stress. Drain voltage is set at -1.5 V and gate voltage is –0.9 V. The NF relates to the transconductance, overlap capacitances, and polysilicon sheet resistance (R_g, R_s) [50]. All the parameters changed after stress. Therefore, the NF is increased with stress.

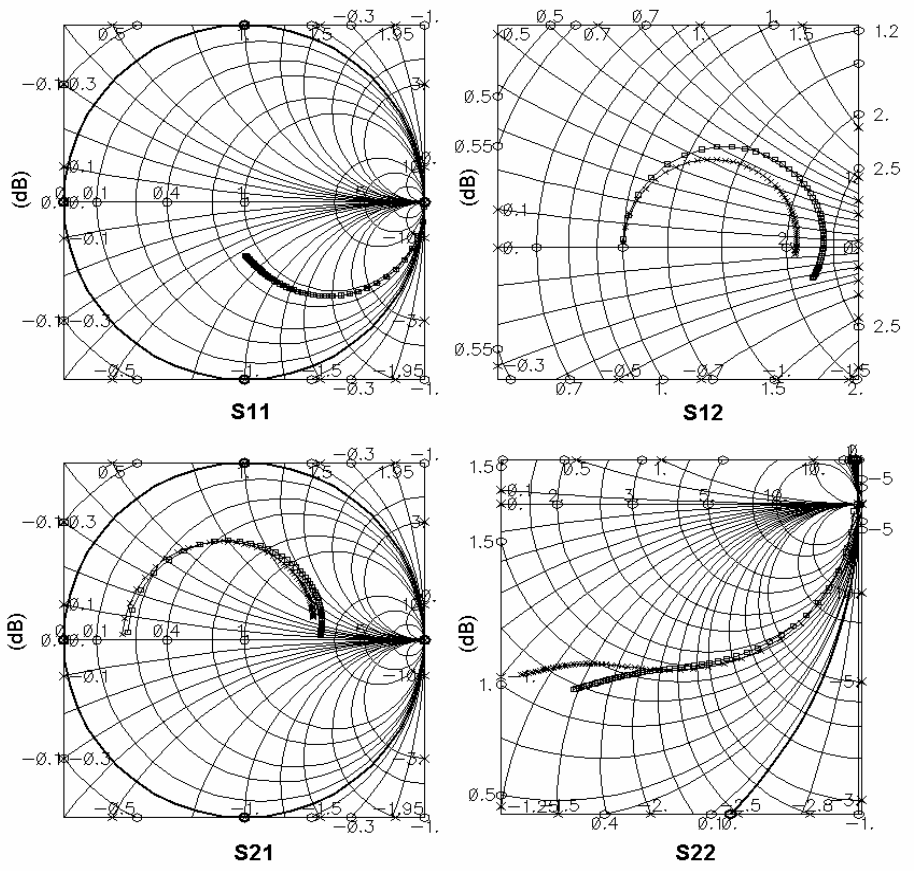


Fig. 6.8 S-parameters for fresh (□) and NSH stress (x). The stress was performed at 400 K. Stress time is 7200 seconds. Measurements were taken with *Vgs* = -0.9 V and *Vds* = -1.5 V.

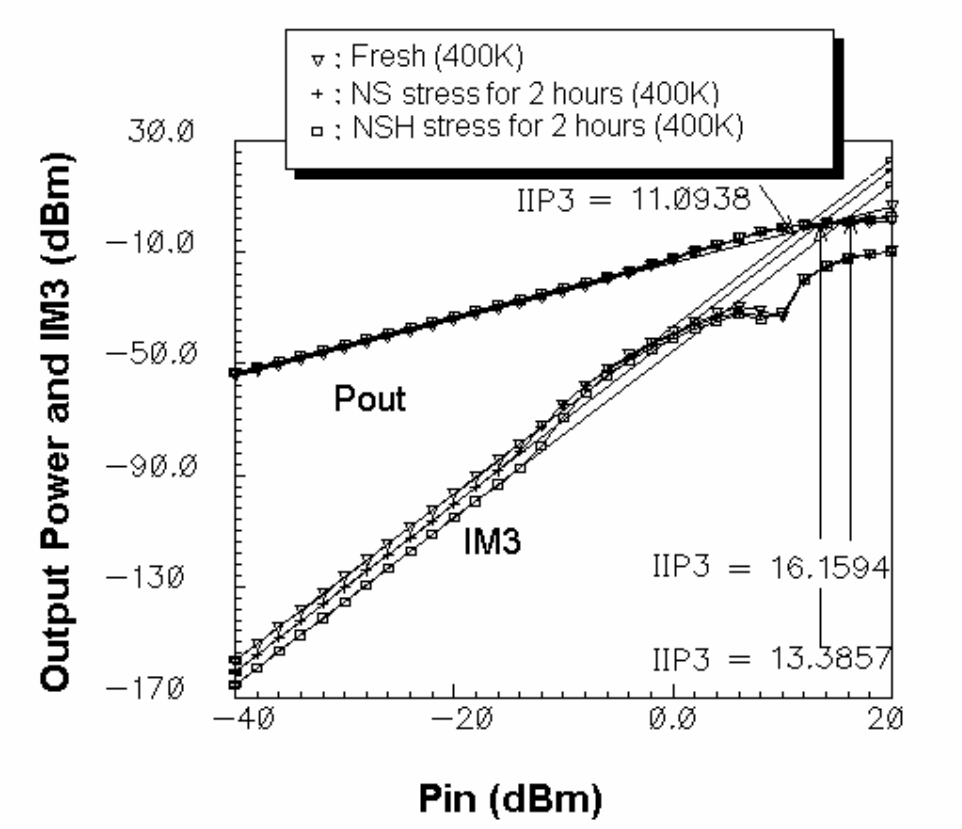


Fig. 6.9 (a) Simulated Output power and IM3 versus input power for fresh, NS stress, and NSH stress. Stress temperature is 400 K, and stress time is 2 hours.

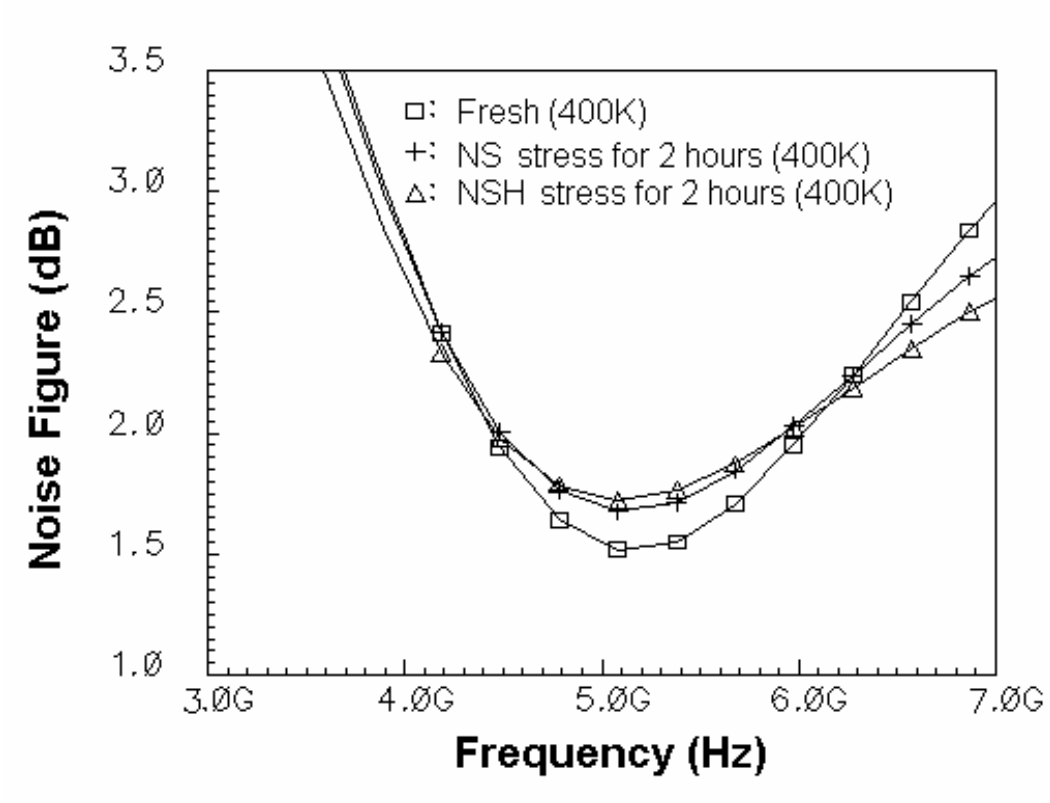


Fig. 6.9 (b) Simulated noise figure versus frequency for fresh, NS stress, and NSH stress. Stress temperature is 400 K, and stress time is 2 hours.

6.4 NSH and NS effects on Circuit Performance

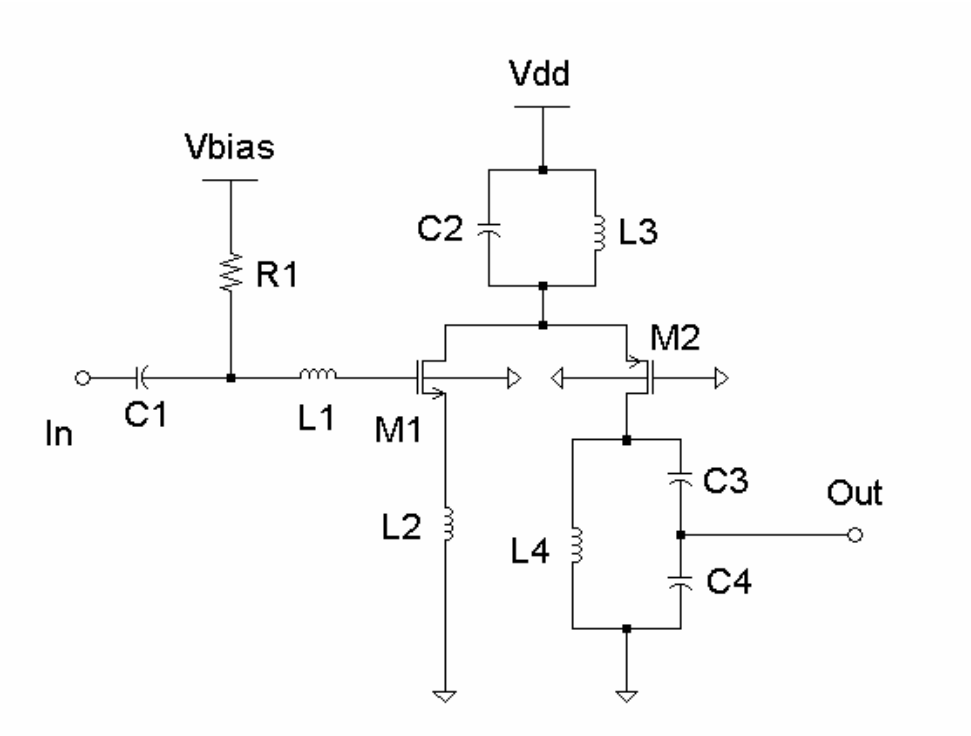


Fig. 6.10 Simplified folded low noise amplifier. *R1* is 1 KΩ, *L1, L2,* and *L3* are 0.5 nH, 2.8 nH, and 2.8 nH, respectively. *C1* is DC block. *C2, C3*, and *C4* are 300 fF, 600 fF, and 600 fF, respectively. The sizes of M1 and M2 are 0.16×50 μm^2 and 0.16×50 μm^2, respectively. *Vdd* is 1.5 V. The operation frequency is 5 GHz.

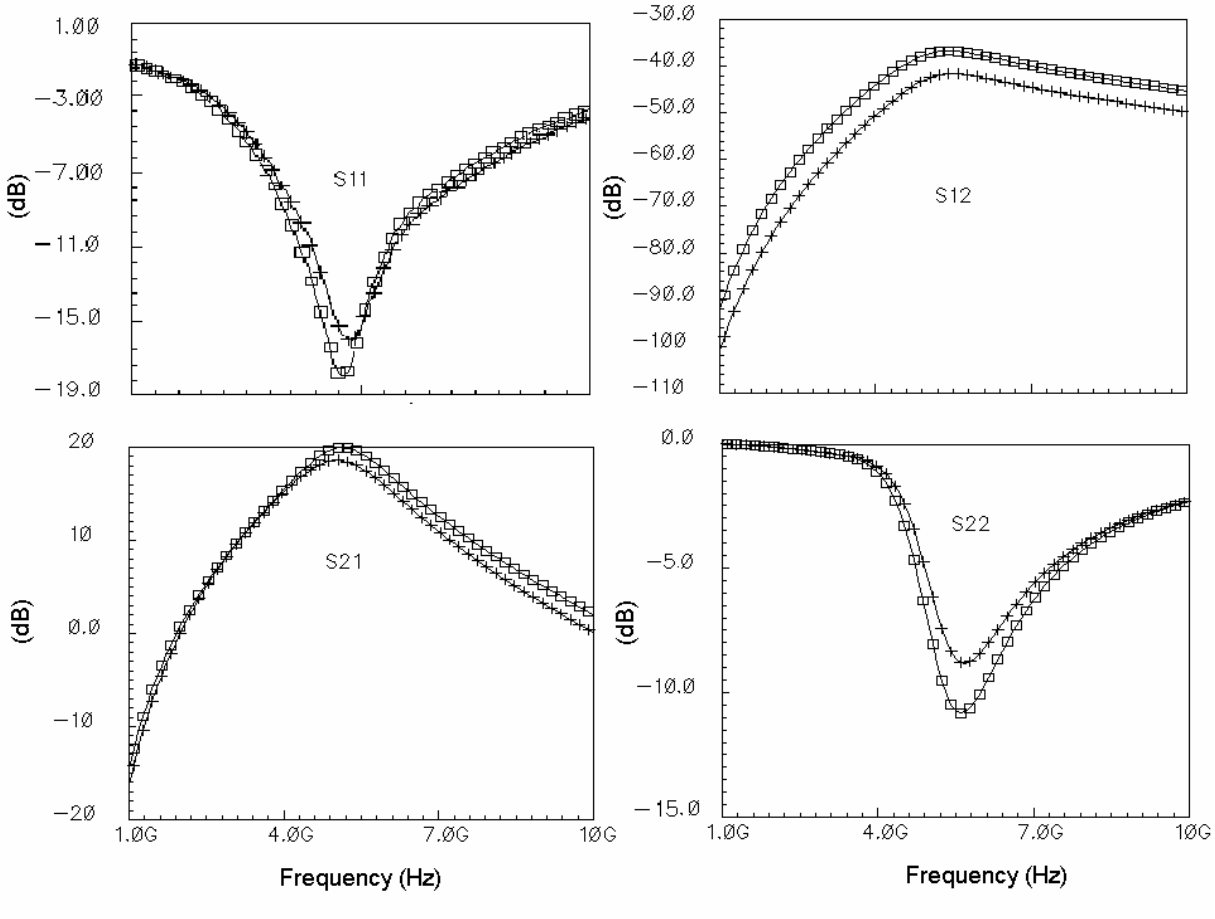


Fig. 6.11 S-parameters before (□) and after (+) NSH stress on pMOS. Stress temperature is 400K, and stress time is 2 hours.

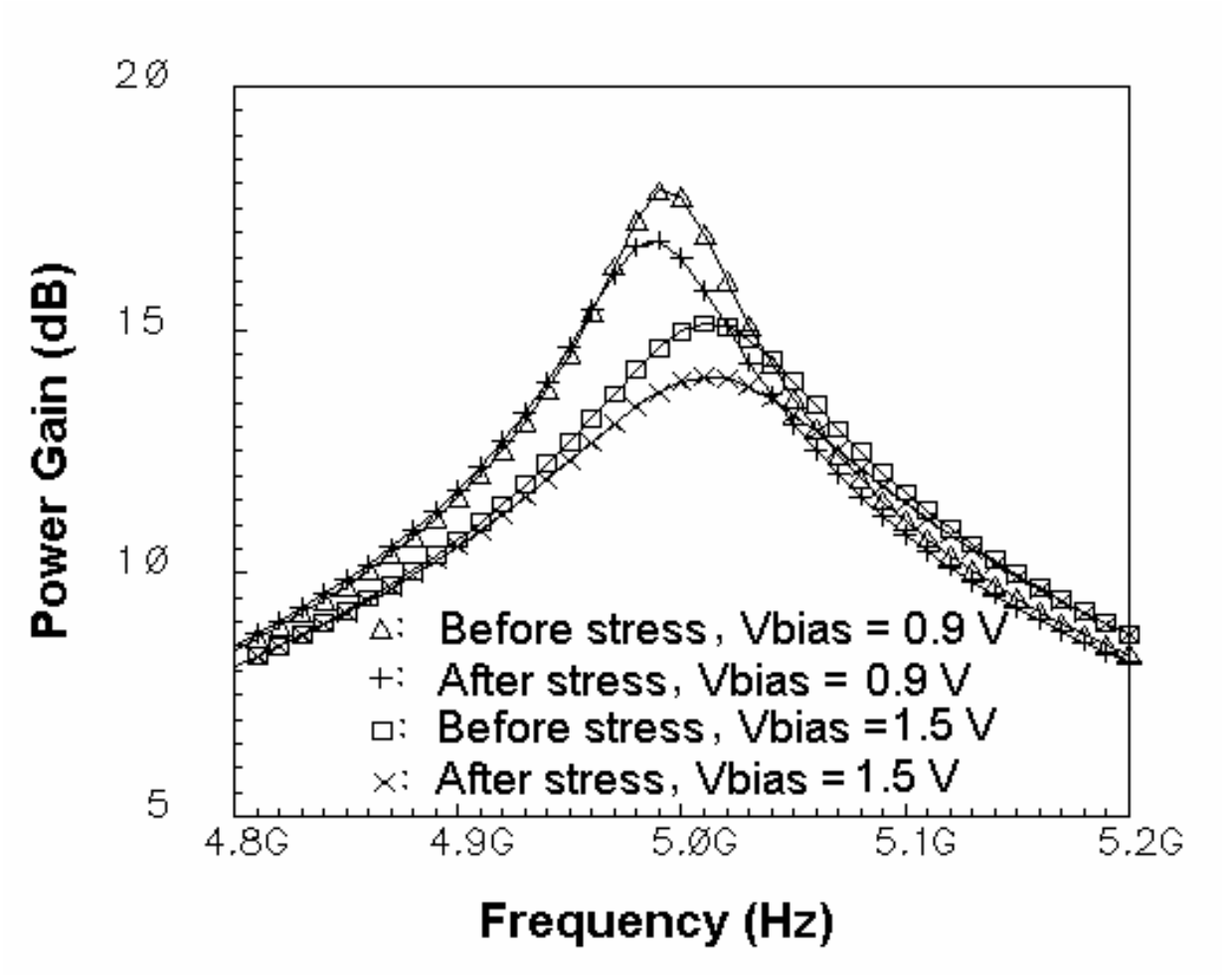


Fig. 6.12 Power gain before and after NSH stress on pMOS. Stress temperature is 400K, and stress time is 2 hours.

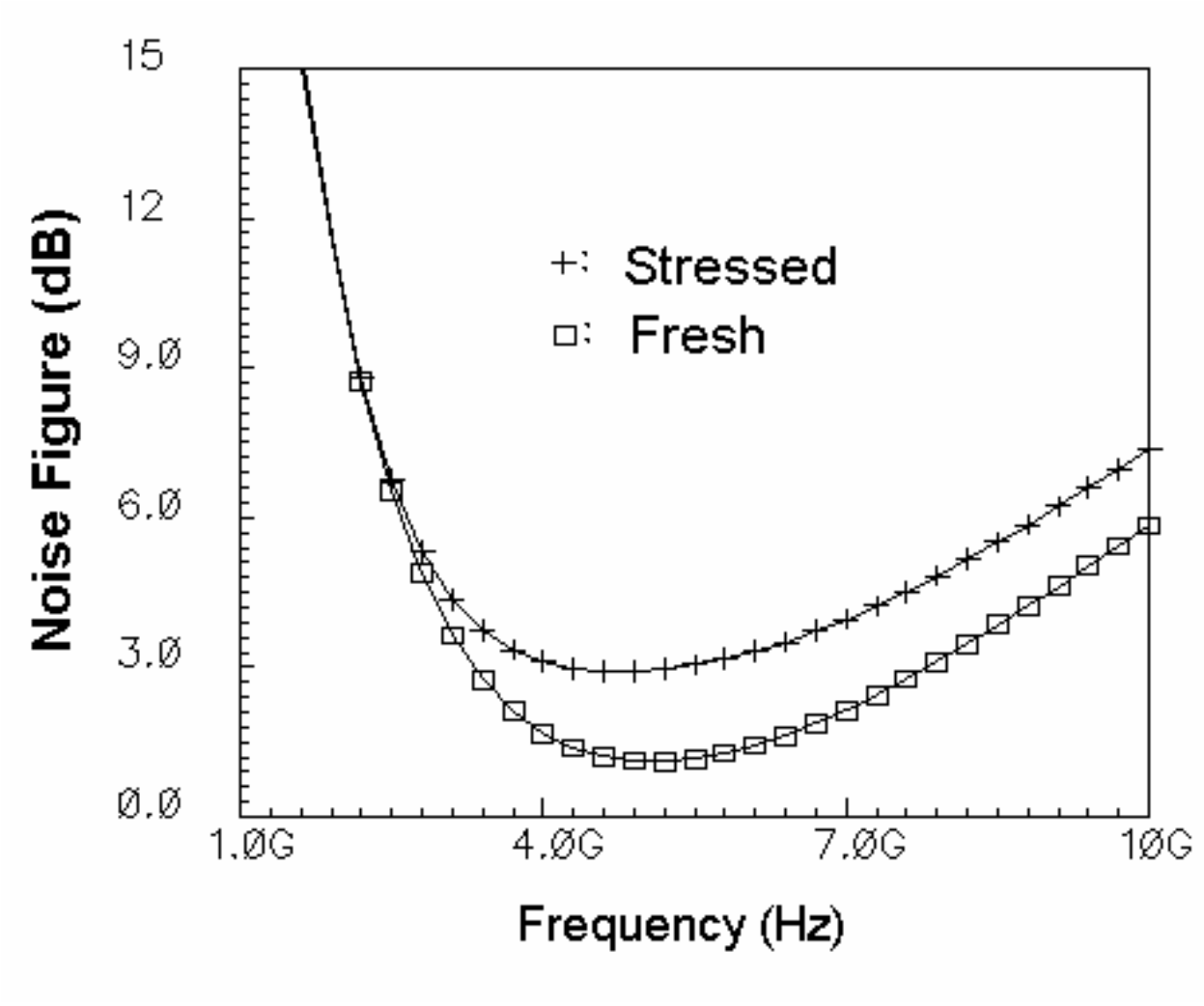


Fig. 6.13 Noise figure (@ 50 Ω) before and after NSH stress on pMOS. Stress temperature is 400K, and stress time is 2 hours.

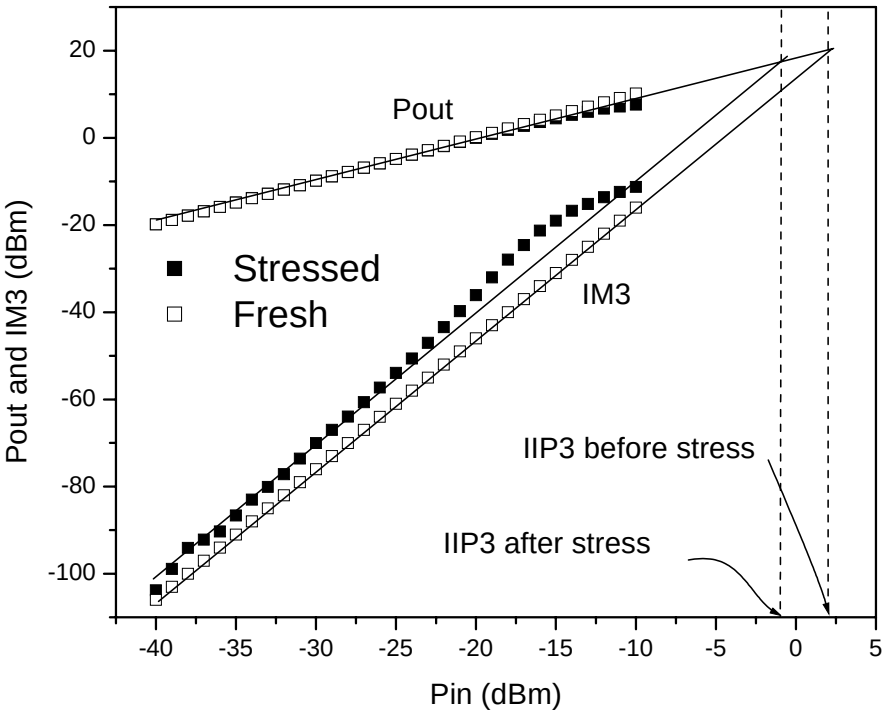


Fig. 6.14 Output power and IM3 versus input power before and after NSH stress on pMOS. Stress temperature is 400K, and stress time is 2 hours.

It is expected that the RF circuit performance degradation follows the device degradation. A folded low noise amplifier (LNA), as shown in Fig. 6, is used as an example to demonstrate the RF performance degradation subject to NSH stress effects. The folded structure is for low-voltage operation purposes [51]. The cascade transistor M2 reduces the input capacitance and enables a good reverse isolation, hereby enhancing the stability. The supply voltage is 1.5 V and the gate bias is 0.86 V. The biasing of the device is consistent with the measurement condition for the model extraction. Here, it assumed that only M2 suffers from the NSH stress effects. The stress time is 2 hours. The devices used in the LNA simulation have 0.16 μm of

channel length. nMOS transistor has 10 fingers 20 μm each and pMOS transistor has 3 fingers 50μm each. A transistor finger is modeled by an extracted transistor model.

The S-parameters as a function of the frequency are shown in Fig. 6.11. At 5.0 GHz, S11 and S21 change slightly. S12 changes from -46 dB to -50 dB at 5 GHz, an 8.6% reduction; S22 diminishes from -9 dB to -8 dB at 5 GHz. Power gain is degraded significantly after stress, as shown in Fig. 6.12. This is mainly due to the decrease of the transconductance of the transistor. Noise figure versus frequency is plotted in Fig. 6.13. After soft breakdown, a leakage path exists across the gate oxide, which adds another noise source to the transistor, thus degrading the noise figure. Also, the drastic increase in gate current due to NSH stress effects increases the real part of the complex input impedance. The immediate impact of such a change affects the impedance matching condition, which is critical for LNA noise performance. Two-tone simulations were performed on the LNA at 5 GHz, with separation of 20 MHz in frequency. The power levels in Fig. 6.14 are given for the fundamental and the third-order inter-modulation product (IM3). IM3 after stress increases, which results linearity degradation. The IIP3 before and after stress are 4.2 and -1.1 dBm, respectively.

6.5 Conclusion

The thermal electrochemical analysis and modeling of MOS devices are given. The temperature accelerated voltage stress shows that degradation increased with temperature and time. The degradation due to NSH stress is more severe than NS stress at high temperature (400 K). A model aiming to evaluate the stress-induced degradation via simulation is developed. The

RF performance degradation of a folded LNA due to temperature accelerated voltage stress is investigated.

CHAPTER SEVEN: SUMMARY

7.1 Achievements

(1) RF performance degradation in nMOSFET and pMOSFET due to hot carrier and soft breakdown effects are examined experimentally

(2) A modeling method to analyze the soft breakdown effects on RF nMOSFET.

(3) The VCO degradation due to gate oxide breakdown is examined.

(4)NSH and NS effects on RF performance are investigated.

7.2 Future Work

(1)It is desirable to examine the RF circuits performance degradation due to HC and SBD stress in the future, such as Power Amplifier (PA). Because when the transistor is operated at the zero drain voltage region, the device suffers significant gate oxide stress. On the other hand, when the transistor is operated at the zero current region, the device suffers significant channel HC stress due to a very large drain voltage. The peak drain-source voltage for a class-E PA can be as high as 3.6 V_{DD}. This gives considerable HC and gate oxide stress to degrade PA performance due to the drain-gate overlap region stress.

(2) In addition, it is expected to investigate some other RF circuits performance degradation due to HC and SBD stress, such as phase lock loop (PLL) and RF filters, because there is few work about it done.

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