MODELING AND OPTIMIZATION OF BODY DIODE REVERSE RECOVERY CHARACTERISTICS OF LDMOS TRANSISTORS

by

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ABSTRACT

As switching speeds for DC-DC converter applications keep becoming faster and faster and voltage requirements become smaller and smaller, the need for new device structures becomes more prevalent. Designers of these new structures will need to make sure they take into consideration the different power losses associated with the different structures and make modifications to reduce or if possible eliminate them. A new 30V LDMOS device has been created and is being implemented into a synchronous buck converter for future DC-DC conversions. This new lateral device has a Figure of Merit of 80mΩ*nC, representing a 50% reduction from the conventional trench MOSFET. The only draw back with this new device is that the body diode power loss has increased significantly.

There are two principal goals of this research. The first is to reduce the body diode reverse recovery characteristics of a 30V LDMOS transistor without employing an additional Schottky diode, increasing the Figure of Merit, or decreasing the breakdown voltage past 30 volts. The second is to achieve 75% reduction in reverse recovery charge (Qrr) through each solution. Four solutions will be presented in this study and have been verified through extensive ISE-TCAD device and circuit simulation.

To my beautiful and loving wife Angela.

ACKNOWLEDGMENTS

I would like to take this opportunity to give praise and thanksgiving to the Lord Jesus Christ for granting me the power to accomplish this research project and write this paper. I would also like to thank my family for all of their loving support and patience, especially my wife Angela.

I would like to express my gratitude to my advisor Dr. Shen for his guidance, support and encouragement throughout the course of my study at the University of Central Florida. It has been a great privilege and honor to work under his supervision. I am also grateful to Dr. Cheng for providing guidance as to the use of ISE-TCAD and in the area of device fabrication processes.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF EQUATIONS

LIST OF ACRONYMS/ABBREVIATIONS

°	Degree
T	Temperature
BV	Breakdown Voltage
V	Voltage
A	Ampere
W	Watt
K	Kelvin
D_n	Electron diffusion coefficient
D_p	Hole diffusion coefficient
E (x)	Local Electric Field
J_n (x)	Electron Current Density
J_p (x)	Hole Current Density
Q_{rr}	Reverse Recovery Charge
T_{rr}	Reverse Recovery Time
n_i	Thermal equilibrium density of electrons and holes

I INTRODUCTION

A Problem Description

i Synchronous Rectifier DC-DC Converter

Microprocessors are used everywhere in today's society. From places that we might not think a microprocessor is used, like imbedded in your automobile's seats. To places that we are all accustom to seeing them in, like computers. As technologies in IC fabrication keep improving and a demand for faster switching speed keeps growing, we continue to see microprocessors being able to use smaller and smaller voltages. On the other side the power consumption continues to increase as more and more transistors are integrated onto a single chip [4]. According to the Semiconductor Industry Association (SIA) technology roadmap, microprocessors will be operating at less than 1V, drawing up to 170A in the near future [6]. This trend tells us that new or better ways of delivering low voltage and high current are needed for the future. Buck converters with synchronous rectifiers are able to provide this low-voltage and high-current that the future will demand.

The buck converter takes a high DC voltage usually with a low current, from a power supply, and steps it down to a lower DC voltage with a higher current. Ideally the power into the converter will equal the power out. This is why if the voltage is stepped down the current will increase. A buck converter operates by applying a pulse width modulated (PWM) waveform to an L-C filter. The filter then averages the PWM

waveform, resulting in a DC output voltage. A variation on a simple buck replaces the diode with a controlled switch, or Synchronous Rectifier (SR), see Figure 1 and Figure 2 below. Figure 1 shows a basic Buck converter with one MOSFET and one diode as the two switches for the topology. Figure 2 shows a typical buck converter that uses two MOSFETs for both the control FET (Q1) and synchronous FET (Q2). Both MOSFETs, Q1 and Q2, are shown with their body diode.

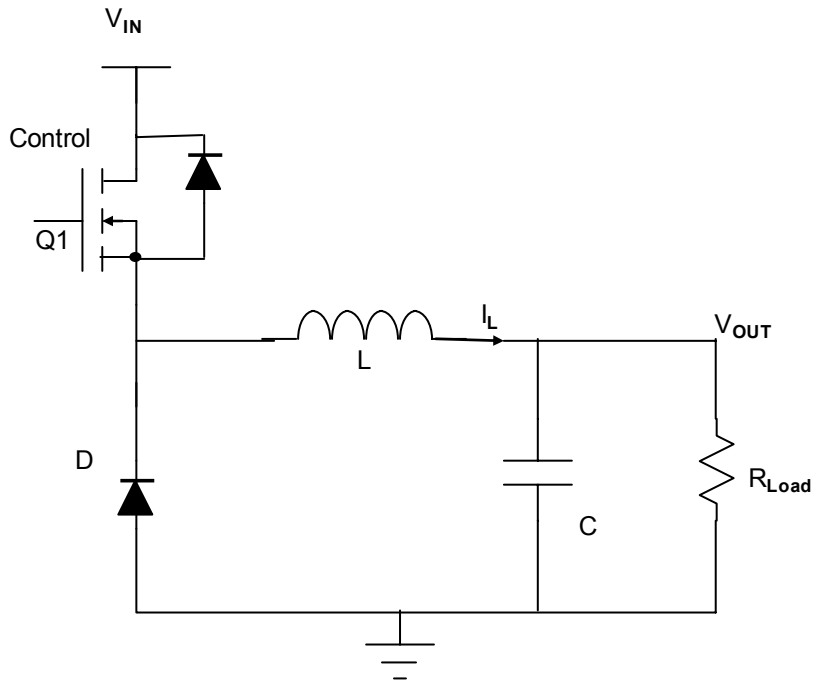

Figure 1: Basic Buck converter with control FET (Q1) and Diode (D)

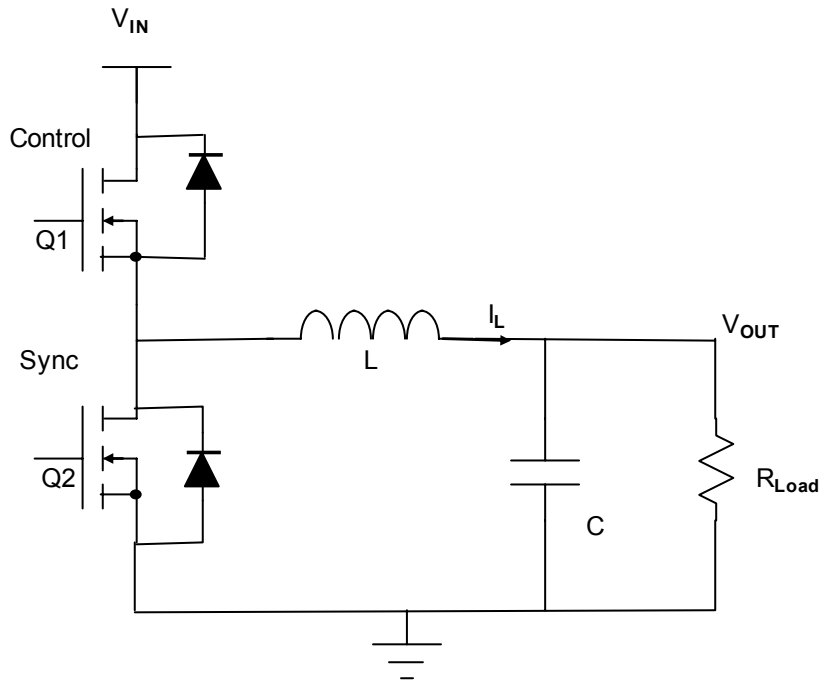

Figure 2: Synchronous Buck converter with control FET (Q1) and synchronous FET (Q2)

A synchronous MOSFET or rectifier has a lower voltage drop than a conventional or Schottky diode, and so its use is quite popular in low voltage DC-DC converters. A table of the three different types of switching devices and their advantages and disadvantages is shown below in Table 1.

Table 1: Different Switching Devices Used in Buck Converters [4]

Device Technology	Advantages	Disadvantages
PN Diode	• Simple two-terminal device • Autonomous self-synchronized rectification (does not need a control signal) • Low cost	• High voltage drop (0.7 – 1.0 V) • High conduction loss • Large reverse recovery loss.
Schottky Diode	• Simple two-terminal device • Autonomous self-synchronized rectification (does not need a control signal) • Medium voltage drop (0.4 – 0.7	• Medium voltage drop (0.4 – 0.7 V) • Additional cost (either discrete or integrated Schottky diodes.

	V) • No reverse recovery loss	• Additional parasitic inductance
Synchronous MOSFET	• Very low voltage drop (0.1 V) • Free body diode in parallel for current freewheeling	• Three-terminal device requiring complicated external control (dead time control) • Large body diode loss due to reverse recovery and diode conduction

As is shown in Table 1 the synchronous MOSFET is a three-terminal device that requires precise external control. A brief explanation of how the synchronous buck converter operates will show why precise control of the synchronous rectifier is needed. A steady-state analysis of the buck converter in Figure 2 shows that the step down ratio V_{out}/V_{in} in the buck converter is controlled by changing the duty cycle of the control FET (Q1). To improve efficiency it is desirable to have the sync FET (Q2) turned on when Q1 is turned off. However, due to finite FET turn-on and turn-off time the state of the two FETs cannot be switched instantaneously. Under normal operation of the synchronous buck converter circuit, the switching sequence goes like the following:

Step 1: Q1 is closed, Q2 is open

Step 2: Q1 is open, Q2 is open

Step 3: Q1 is open, Q2 is closed

Step 4: Q1 is open, Q2 is open

Step 5: Q1 is closed, Q2 is open

To increase the efficiency of the converter the time (dead time) that both of the FETs are open should be reduced to the minimal duration. There is a limit to this reduction. If the

dead time is reduced below the turn-on or turn-off time of the FETs, the switches may go to a state that both of the FETs are closed. This state is often referred to as shoot-through when both transistors are on at the same time shorting the input supply. This state should be avoided as it can result in significant loss of efficiency and could damage the FETs. The switches drive an inductive load as shown in Figure 2. When the circuit transitions from step 1 to 2, the current through the inductor cannot instantly drop to zero and will continue to flow through the PN body diode of sync FET Q2. The diode will conduct the current through the inductor until the bottom FET can be turned on in step 3. Generally, during step 2, current flows through the diode. This current leads to high power losses which have vast impacts on the efficiency of the converter. The body diode power losses will be a major barrier in meeting efficiency requirements for future buck converters as the frequencies keep increasing.

ii Adaptation of LDMOS in DC-DC Converters

Since next generation microprocessors and ultimately computers, will demand 1 V 170 A, DC-DC converters and higher power conversion efficiency at higher operating frequency will also be required. Usually synchronous rectification is used to meet such requirements. But as efficiencies and operating frequencies go up the power losses from the MOSFETs used in the synchronous buck converter will also go up, so new technology is needed to reduce these power losses. Particularly, control FETs will be required to reduce both their conduction losses and switching losses. Conduction losses are due to the resistance in the channel of the MOSFET, referred to as $R_{DS(ON)}$. Switching losses are due to parasitic capacitances such as C_{GD} and C_{GS}. To estimate the total loss of the control FET, the product of $R_{DS(ON)}$ and Q_G (the switching charge) is commonly used. This product is referred to as the figure of merit (FOM). Published research has shown that various techniques have been used to reduce the conduction and switching losses by reducing the FOM [4]. Reducing the gate resistance (R_G) is also an effective method to reduce switching loss because modem drivers for MOSFETs have low output resistance. The Power Semiconductor Device Research Group at the University of Central Florida has developed a new LDMOS structure with improved FOM for the control FET of DC-DC converter applications. This device achieves not only low $R_{DS(ON)} * Q_G$ but also low gate resistance.

This adaptation of LDMOS for use in DC-DC converters has been relatively a new and recent development. LDMOS have been around for many years, but historically it has been used in RF switching. Vertical DMOSFETs have been commonly used in DC-

DC converters as the switching devices. In recent years people have found that using Lateral DMOSFETs will give you better performance characteristics. Table 2 lists some of the performance characteristics that you get when using either VDMOS of LDMOS.

Table 2: Vertical DMOS vs. Lateral DMOS

Vertical DMOS	**Lateral DMOS**
• Bottom Side Drain	• Bottom Side Source
• Source bond wire reducing gain	• No source bond wire
• Higher C_{RSS}	• 3dB higher gain
• BEO isolation	• Lower C_{RSS}
• High Package Cost	• Higher Power
	• Higher Efficiency
	• Lower Package Cost
	• No BEO required
	• Improve theta jc

iii Poor Reverse Recovery Characteristics of LDMOS Devices

As the conduction and switching losses in synchronous MOSFETs used in buck converters are reduced through use of new devices, such as LDMOS, body diode conduction losses or reverse recovery losses will start to contribute to a substantial portion of the total power losses. In the device that has been created by the Power Semiconductor Device Research Group at the University of Central Florida the reverse recovery characteristics actually became worst than in the commonly used Vertical MOSFET. This poor reverse recovery characteristic of LDMOS will need to be solved before this type of device can be used in future DC-DC applications.

B General Goal of Research

The goal of this research project is to investigate solutions to the poor reverse recovery characteristics of the LDMOS synchronous MOSFET. To verify that the solutions will work, extensive mixed-mode device and circuit simulations will be run and analyzed. Any modifications or changes done to the original device should be done without altering any of the other characteristics such as the Figure of Merit or breakdown voltage.

II LITERATURE REVIEW

A PN Diodes, Power Diodes, and Schottky Diodes

There are three basic types of diodes, the basic *pn* diode, the power diode, and the Schottky diode. The *pn* junction is the most basic device of all semiconductor devices, it serves a building block for all other devices and a good understanding of its structure and how it works is needed as a foundation. A *pn* junction is formed when an *n*-type region in a silicon crystal is adjacent to a *p*-type region in the same crystal, as illustrated in Figure 3. Such a junction can be formed by diffusing either acceptor impurities into an *n*-type silicon crystal or donor impurities into a *p*-type silicon. The *pn* junction is characterized by a few ways. The junction is often characterized by how the doping change from p-type to n-type as the junction is crossed. The junction is also characterized by the relative doping densities on each side of the junction. If the acceptor density on the *p*-type side is very large compared to the donor density on the *n*-type side, the junction is referred to as a p^+n junction. The difference needs to be on an order of magnitude greater. If the donor density is not much larger than n_i in the previous example, the junction might be termed a p^+n^-. Other variations are also used but are usually found in power semiconductor devices. The *pn* junction is also referred to as a *pn* diode. The diode is only different in structure from just two pieces of silicon next to each other in that it has metal contacts on each end of silicon. These contacts are usually referred to as the anode and cathode, see Figure 3. When an external voltage is applied between the *p* and *n* regions it appears entirely across the space charge region (SCR) because of the large resistance of the

depletion layer compared to the rest of the material. If the applied potential is positive on the *p* side, or anode side, it opposes the contact potential and reduces the height of the potential barrier, and the junction is said to be forward biased. If the applied voltage is positive on the *n* side, or cathode side, the junction is said to be reverse biased and the barrier height is increased. Figure 4 shows the *I-V* characteristic of a *pn* diode in both forward and reverse bias. When the *pn* diode is reversed bias it actually does conduct a small leakage current. The *pn* diode's *I-V* characteristics are very close to an ideal switch. When the diode is forward bias it cunducts current or is on and when the diode is reverse bias it is off and only conducts a very small reverse current. The diode actually has a limit on the reverse voltage it can take before the current starts to increase dramatically. This rapid increase in current at the reverse bias voltage is termed reverse breakdown or avalanche breakdown. Operation of the diode in breakdown must be avoided because the product of the very large voltage and current can lead to excessive power dissipation and can damage the device.

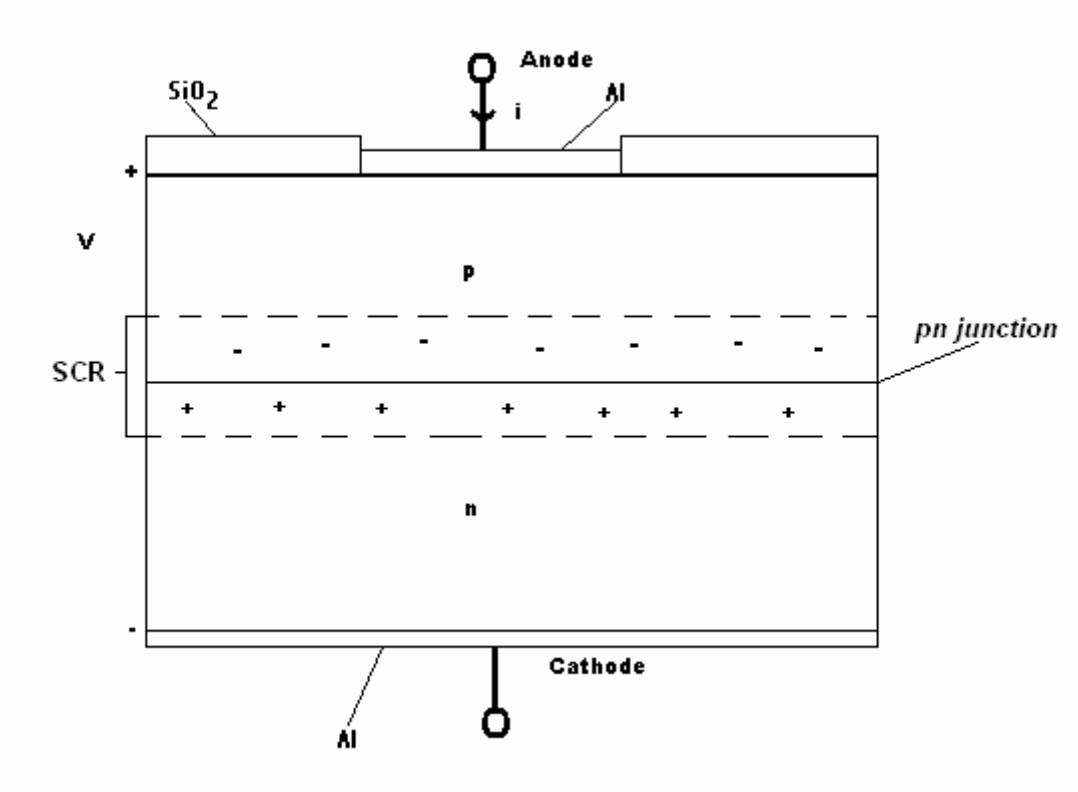

Figure 3: Basic Diode with Space Charge Region shown

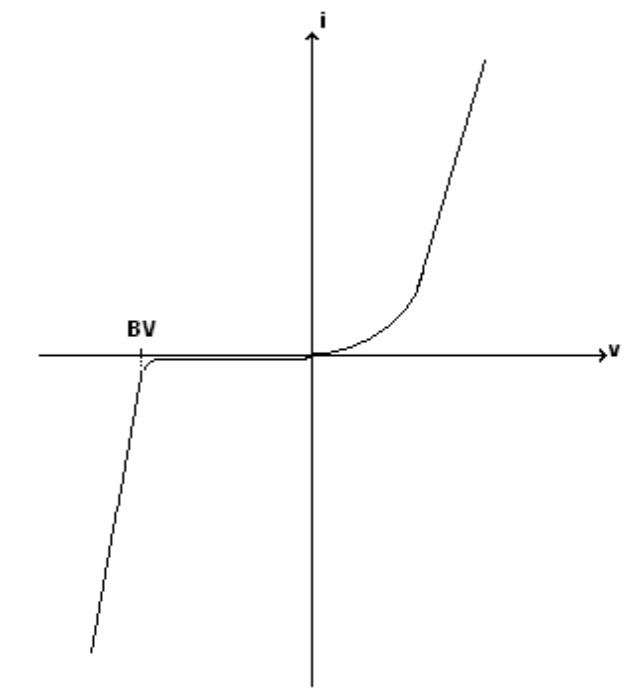

Figure 4: *I-V* characteristic of a *pn* diode

The typical power diode consists of a heavily doped n-type substrate on top of which is grown a lightly doped n- epitaxial layer of a specified thickness. Finally the *pn* junction is formed by diffusing in a heavily doped *p*-type region that forms the anode of the diode. The n- epitaxial layer, which is often termed the drift region, is the prime structural feature not found in low-power *pn* diodes. Its function is to absorb the depletion layer of the reverse-biased *p*+*n*- junction. This layer can be quite wide at large reverse voltages. The drift region establishes what the reverse breakdown voltage will be. This relatively long lightly doped region would appear to add significant ohmic resistance to the diode when it is forward biased, a situation that would apparently lead to unacceptably large power dissipation in the diode when it is conducting current. The *I*-*V* characteristic curve for the power diode is basically the same as the low power *pn* diode, except for the slope of the curve for the forward biased region increases linearly and not exponentially like on the low power diode. The power diode does have a particular issue that needs to be addressed when designing a diode for a particular breakdown voltage rating that the basic *pn* diode doesn't have. This issue has to do with the length of W_d. If the length W_d of the lightly doped drift region is longer than the depletion layer width at breakdown, then the structure is termed a non-punch through diode, that is, the depletion layer has not reached through (or punched through) the lightly doped drift region and reached the highly doped *n*+ substrate.

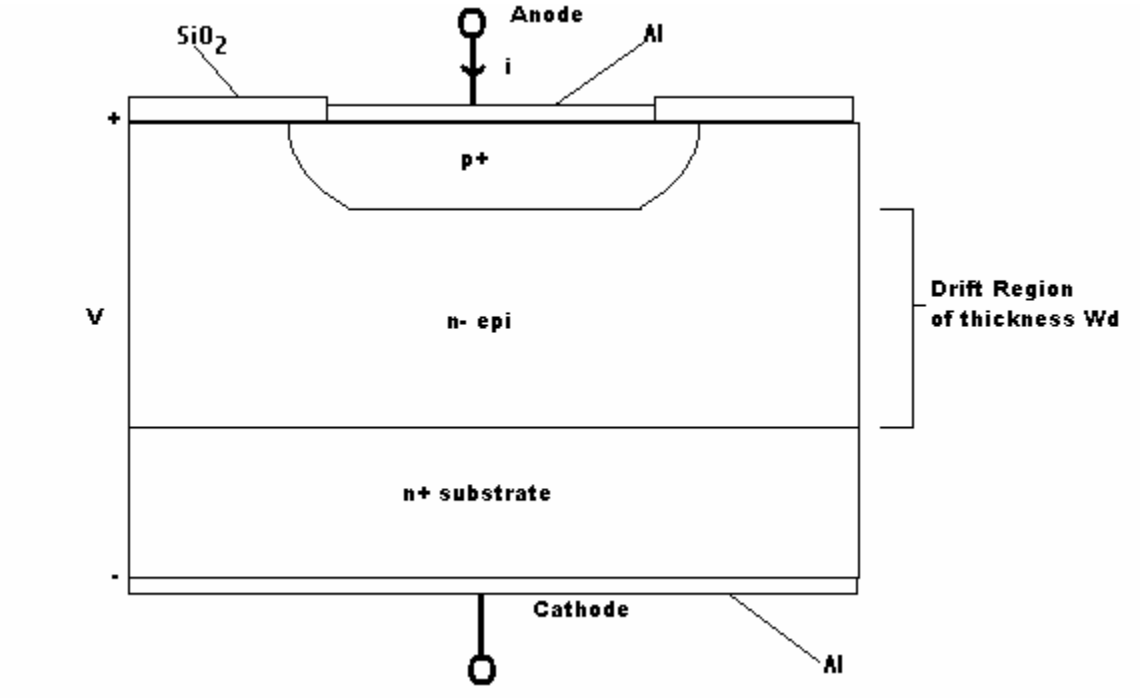

Figure 5: Cross-sectional view of a pn-junction diode intended for power applications

A Schottky diode is formed by placing a thin film of metal in direct contact with a semiconductor. The thin metal film serves as the positive electrode and the semiconductor is the cathode. The *I-V* characteristic curves of the Schottky diode are very similar to that of the basic *pn* diode and the power diode. The fundamental physics are different though between the Schottky diode and the other two. The Schottky diode has some advantages over the *pn* diodes, but it also has some disadvantages. Table 1 lists the advantages and disadvantages for both the *pn* diode and the Schottky diode. The Schottky diode has been used extensively to reduce the reverse recovery time in DC-DC converters, but for my particular research solutions it would cost to much as far as fabrication costs and parasitic losses are concerned. This topic will be discussed more in the proceeding sections.

B Reverse Recovery Characteristics and Device Solutions

The transition from the conduction to the blocking state in a diode that is in a switching circuit takes a finite amount of time. This finite amount of time is known as the reverse recovery time (t_{rr}) of the diode. This can further be divided into the time, t_a, taken to remove the carriers (current through the diode reverses for a short period of time) before it can block the voltage, and the time, t_b, during which the diode voltage goes negative with a rate of change dV_R/dt. Increased injection, to reduce the forward voltage drop, implies more charge that needs to be removed from the intrinsic region before the diode will be able to block voltage. This will, therefore, adversely affect the reverse recovery time. Figure 6 below gives the waveforms and the definitions of the recovery characteristics of a diode. The removal of stored charge in the intrinsic region occurs by means of the flow of a large reverse current during time t_a. At the end of this time the junction becomes reverse biased. The reverse current at this point is defined as the peak reverse recovery current, I_{RR}. The value of I_{RR} is proportional to the rate of change of forward current through zero crossing dI_F/dt.

$$I_{RR} = \left(\frac{dI_F}{dt}\right) \times t_a$$

Equation 1

The reverse current then decreases by recombination at a rate of dI_R/dt in time t_b. The amount of reverse recovery charge is given by

$$Q_{RR} = \frac{(I_{RR} \times t_{rr})}{2}$$

Equation 2

Where $t_{rr} = t_a + t_b$

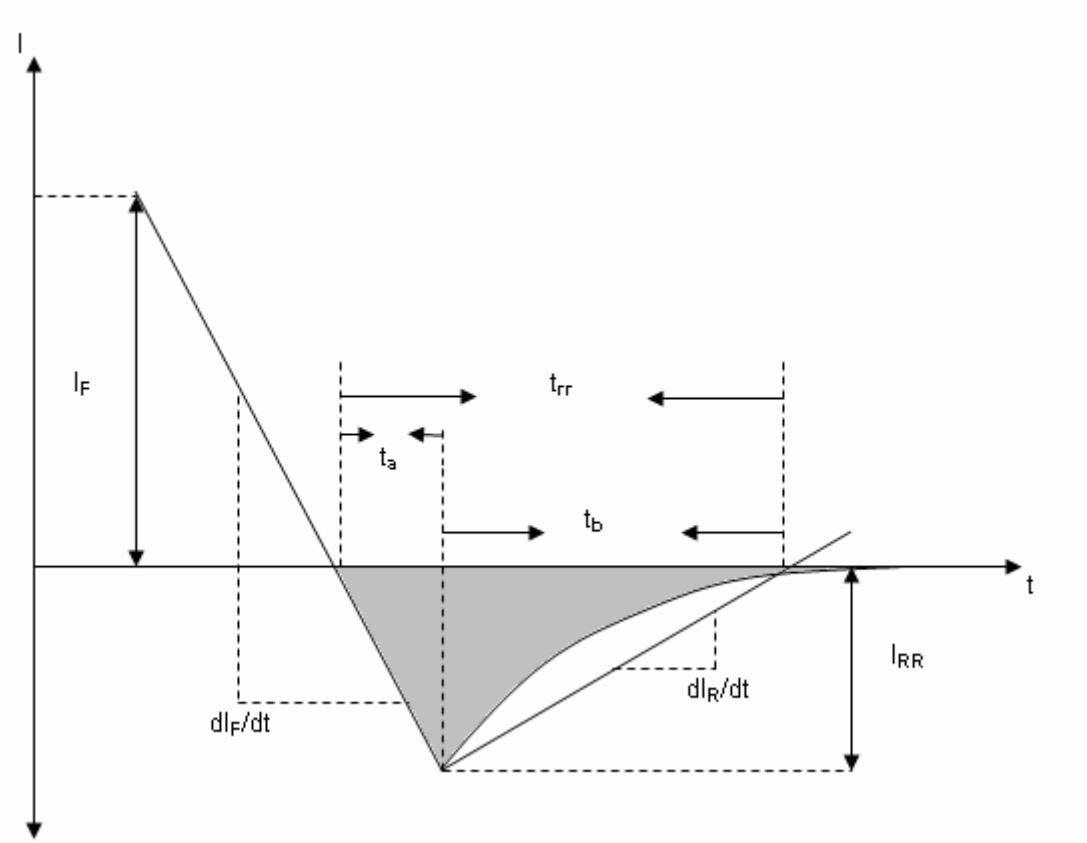

Figure 6: Reverse recovery waveform and definitions

Several prior-art approaches have been proposed to address the body diode power loss issue, but unfortunately all are at the expense of increased size, cost, and control complexity of the synchronous MOSFET [3]. The main solution that has been used previously surrounds the idea of a Schottky diode in parallel with the body diode, either

integrated or as a discrete. This solution has been shown to have actually more losses than gains mainly due to the added parasitic inductances from the connections of the Schottky to the MOSFET. Integration of a Schottky diode onto the same die as the MOSFET will significantly reduce the parasitic inductances but will add extra costs into the fabrication process. Another solution to reducing the reverse recovery effect that is being used is ion irradiation. Ion irradiation will not work in this application because it can have an adverse effect on the other characteristics of the LDMOS device. The purpose of this project is to give the device designer some solutions to the body diode power loss issue without increasing size, cost, or control complexity of the synchronous MOSFET.

III RESEARCH OBJECTIVES

As was stated previously the goal of this research project is to investigate solutions to the poor reverse recovery characteristics of the LDMOS synchronous MOSFET. The solutions will be verified through extensive ISE-TCAD device and circuit simulation. A proposal of four different solutions has been identified in this paper. These solutions will reduce the body diode reverse recovery characteristics of original LDMOS transistor without employing an additional Schottky diode or increasing the Figure of Merit. These solutions will also stay above 30V for a breakdown voltage. My target is to achieve 75% reduction in reverse recovery (Qrr) through each solution.

IV TECHNICAL APPROACH

A New Device Structures

i Baseline LDMOS Transistor

The device shown in Figure 7 is a new 30V LDMOSFET with a ($R_{DS(ON)}$*Q_G) FOM of 80mΩ*nC. Unfortunately, this particular MOSFET has large reverse recovery losses. Table 3 lists the electrical characteristics that go with the 30V LDMOS device. This particular device structure was created in FLOOPS and then the electrical characteristics were obtained by running the FLOOPS structure through DESSIS. For more on FLOOPS, DESSIS, and the entire ISE-TCAD software package please refer to section B Numerical Modeling Approach. The same DESSIS files are used to derive the electrical characteristics of the solutions, thus we baseline all of the results against this information. The breakdown voltage in Table 3 is higher than 30V which is the required breakdown voltage. This is ok and actually is an added increase in performance. All of the solutions that will be developed and modeled will also have this 30V minimal breakdown voltage. This will be the first electrical characteristic that we will look at in the results to verify that the device meets the 30V requirement

Table 3: Reverse Recovery Characteristics of 30V LDMOS Device

Qrr (C)	1.79605E-07
Trr (sec)	4.00000E-08
Irr (A)	3.91073E+00
BV (V)	39.8

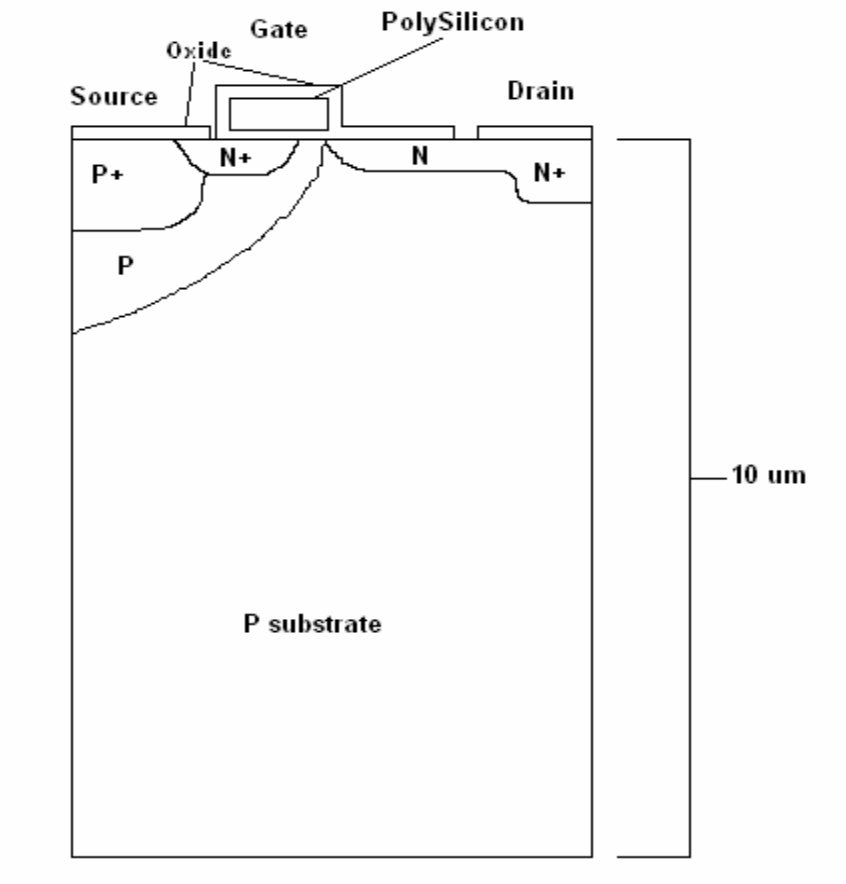

Figure 7: Baseline LDMOS Transistor

ii LDMOS Transistor with P+ Substrate and P Epi Layer

This solution was derived from the idea that people used to create the *p-i-n* diode for power applications. The difference between this structure and the baseline is in the beginning stages of fabrication. First, a highly doped substrate is laid down and then a lightly doped epitaxial layer is deposited on top of it. The rest of the sequences in the fabrication process are the same. The boundary between the epitaxial layer and the highly doped substrate serves as a barrier for depletion layer that is formed by the reverse-biased *n+p-* junction. The length of this epi region will establish what the reverse breakdown voltage will be. The shorter the length of the epi region the smaller the breakdown voltage will be. Figure 8 shows cross-sections of the three variations of this solution that simulations were run on. Each variation has a different epi layer thickness.

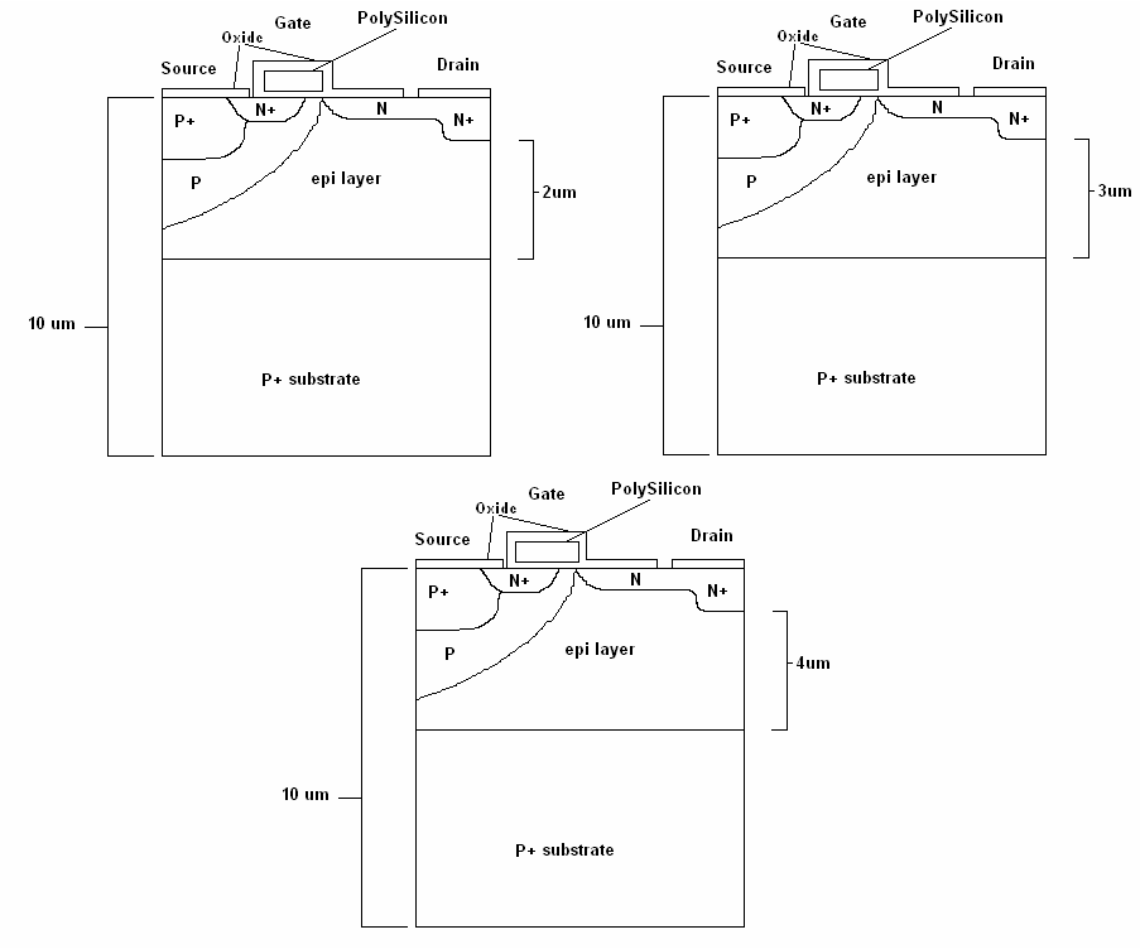

Figure 8: LDMOS Transistor with P+ Substrate and P epi layer

iii LDMOS Transistor with P Substrate and SOI layer

This solution is a variation of the previous idea behind the last solution. Instead of creating a depletion region barrier with a P+ and P- region we insert a SOI layer at a specified depth on to the p substrate. The SOI layer serves as the boundary or stopping point for the depletion region. Figure 9 shows cross-sections of the three variations of this solution that simulations were run on. All three variations have a SOI layer of 2µm in thickness. Each variation has the SOI layer a different distance away from the N+ region.

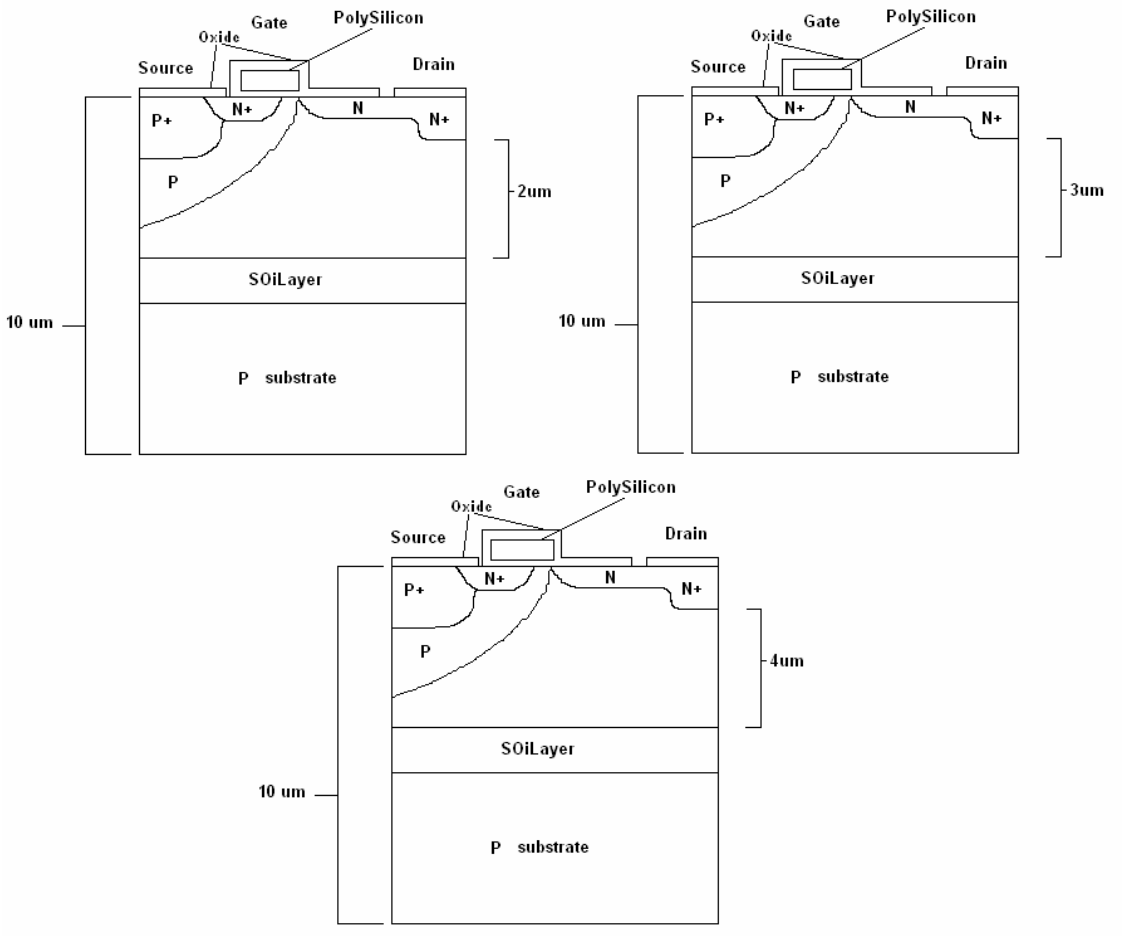

Figure 9: LDMOS Transistor with P substrate and a SOI layer implanted at different distances from N+ region

iv LDMOS Transistor with P Substrate, SOI layer, and P Epi Layer

This solution is a combination of the last two solutions. This device has a P substrate initially then a SOI layer of 2μm thickness is deposited and then an epitaxial layer is also deposited. The epitaxial layer varies in thickness for each different device shown in Figure 10. This combination is being tried to see if an optimal solution can be found by combining some of the previous solutions together.

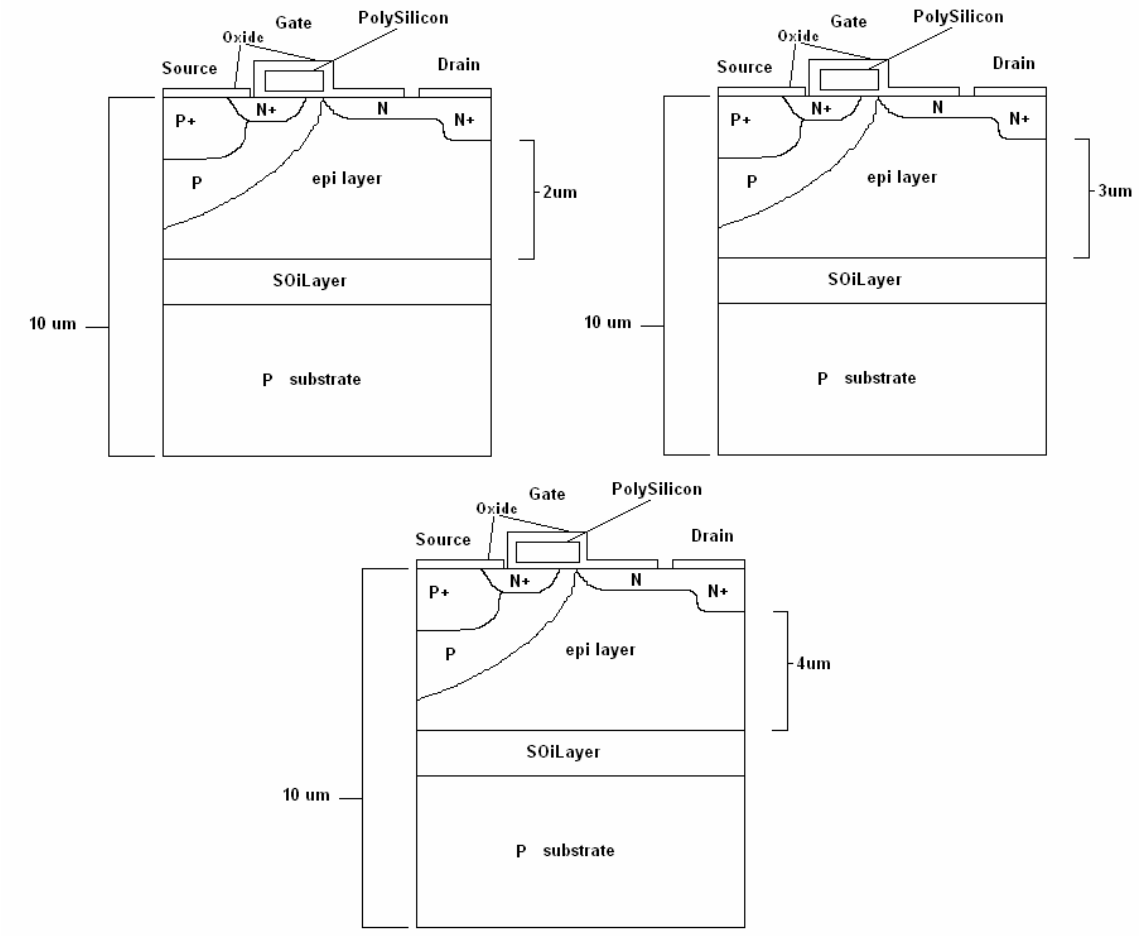

Figure 10: LDMOS Transistor with P substrate, SOI layer, and P epi layer of different thickness and different doping concentrations

v LDMOS Transistor with P+ Substrate, SOI layer, and P Epi Layer

This solution is a second combination of the first two solutions. This device has a P+ substrate initially then a SOI layer of 2µm thickness is deposited and then an epitaxial layer is also deposited. The epitaxial layer varies in thickness for each different device shown in Figure 11. This combination is being tried to see if a P+ substrate will have any effect on the reverse recovery characteristics or the breakdown characteristics.

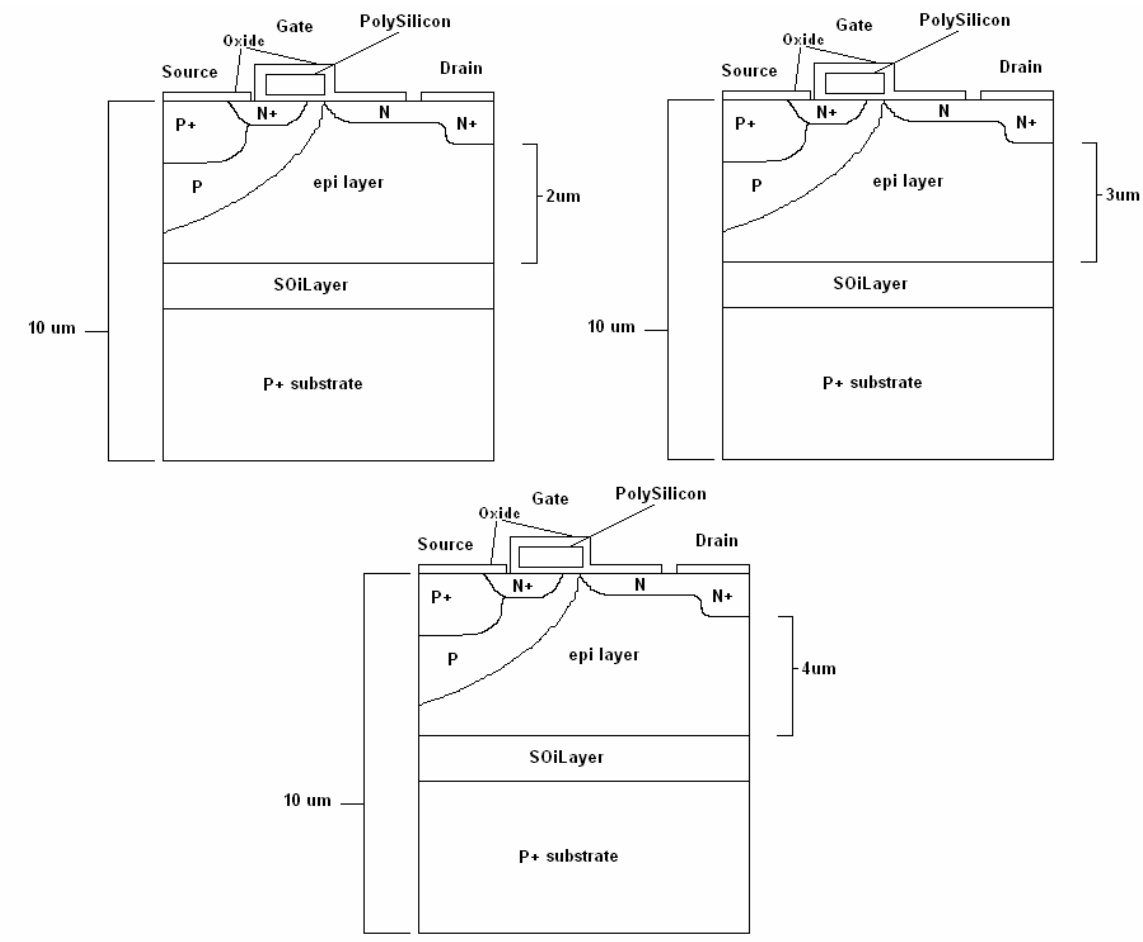

Figure 11: LDMOS Transistor with P+ substrate, SOI layer, and P epi layer of different thickness and different doping concentrations

B Numerical Modeling Approach

ISE-TCAD is the modeling and simulation package that was used for this project. ISE-TCAD is a powerful software package that is used throughout the semiconductor industry from development of new sub-micron devices to large-scale, high-voltage power devices. Designers can, and have used TCAD to more efficiently explore new device architectures and optimize process flows. TCAD has also been used in manufacturing for advance process control and parametric yield improvement [1]. The four main functions of ISE-TCAD that were used during this project were the device simulator – DESSIS, the process simulator – FLOOPS, the interfacing tool – MDRAW, and the graphing tool - Tecplot.

FLOOPS is used first to help us foresee and visualize what the device structure looks like. FLOOPS reads a command file that was created in Windows Notepad and runs it through a DOS command window. The command file contains all of the steps that the designer would like the device to go through during its build. For example, if you were going to create a basic *pn*-diode, the first thing that would be in your command file would be code that specifies what size substrate and doping concentration you would like to start with. Then you would insert a layer of epitaxial and bake it for 15 minutes at 1100° C. Then you would lay an oxidation layer down and bake it again for 30 minutes at 1100° C. An implant window opening would be created and you would diffuse some Boron into the device for 10 minutes at 1150° C. Finally, a contact window opening and metallization would be added. A sample of the code used is shown in the APPENDIX: ISE CODE. After the command file is run through FLOOPS the designer can check what the device looks like by using Tecplot the graphing tool within the package. FLOOPS

writes the final structure of the device into an interface format to be used by another program called MDRAW.

MDRAW is the program that is used to convert the FLOOPS final structure file into the format that DESSIS can use to simulate the electrical characteristics of the device. MDRAW can also be used to draw a device structure from "scratch" and pass it to DESSIS. This approach is simpler and faster, but less precise. It is often used when a designer wants to verify that the basic idea of the structure will make sense and work and not have to go through all of the trouble of coding the FLOOPS file. In MDRAW you actually re-draw the entire device and specify the mesh to be used by DESSIS. The mesh takes the data points from the FLOOPS file and loads them into the device structure that you have created. DESSIS then takes another command file, file that the designer has specified what characteristics that they would like to test for, and the MDRAW file and runs the specific test. The results are in the form of a data file and can be viewed by any graphing tool, such as Tecplot.

V MODELING RESULTS AND DISCUSSION

A LDMOS Transistor with P+ Substrate and P Epi Layer

This solution provided results that were expected, as the epitaxial layer thickness decreased in size the breakdown voltage also decreased in size. If the breakdown voltage was the only thing that was being investigated then the "sweet spot" or the device with the highest BV would be the device with an epi layer that has a doping concentration of 9E15 cm^{-3} and a thickness of 4µm. See Figure 12 for a comparison of all of the doping concentration variations with the epi thickness assigned. Figure 25 thru Figure 27 also show the breakdown voltages for each device in this category of solution. Figure 13 shows the electric field potential when breakdown occurs. As the electric field goes up the region becomes "hotter". The variation with an epitaxial thickness of 2µm actually reduced the breakdown voltage past the minimum value required.

The opposite effect happened with the reverse recovery characteristics and the epi thickness. As the epi layer thickness became smaller the reverse recovery characteristics also became smaller. This makes sense because as the epi thickness becomes less so does the amount of charge that can be stored in that region. The more charge that is in the region the longer the reverse recovery time will be and the larger the reverse recovery charge (Qrr) will be. The best performing device as far as Qrr is concerned is the device with an epi layer that has a doping concentration of 7E15 cm^{-3} and a thickness of 2µm. This device compared to the baseline device showed a 79% improvement in reverse recovery charge. Figure 14 thru Figure 16 show different comparisons between Qrr and

doping concentrations, Trr and doping concentrations, and Irr and doping concentrations. Figure 17 thru Figure 21 shows the reverse recovery waveforms decreasing in size as the epitaxial layer decreases in size. These figures also compare the reverse recovery waveform of the baseline device with that of the solutions with different epi thicknesses. A dramatic improvement in the reverse recovery characteristics can be seen. Figure 22 thru Figure 24 show the reverse recovery waveforms for each epi layer thickness but with varied doping concentrations. The doping concentration in this solution doesn't play a large role in reducing the reverse recovery characteristics.

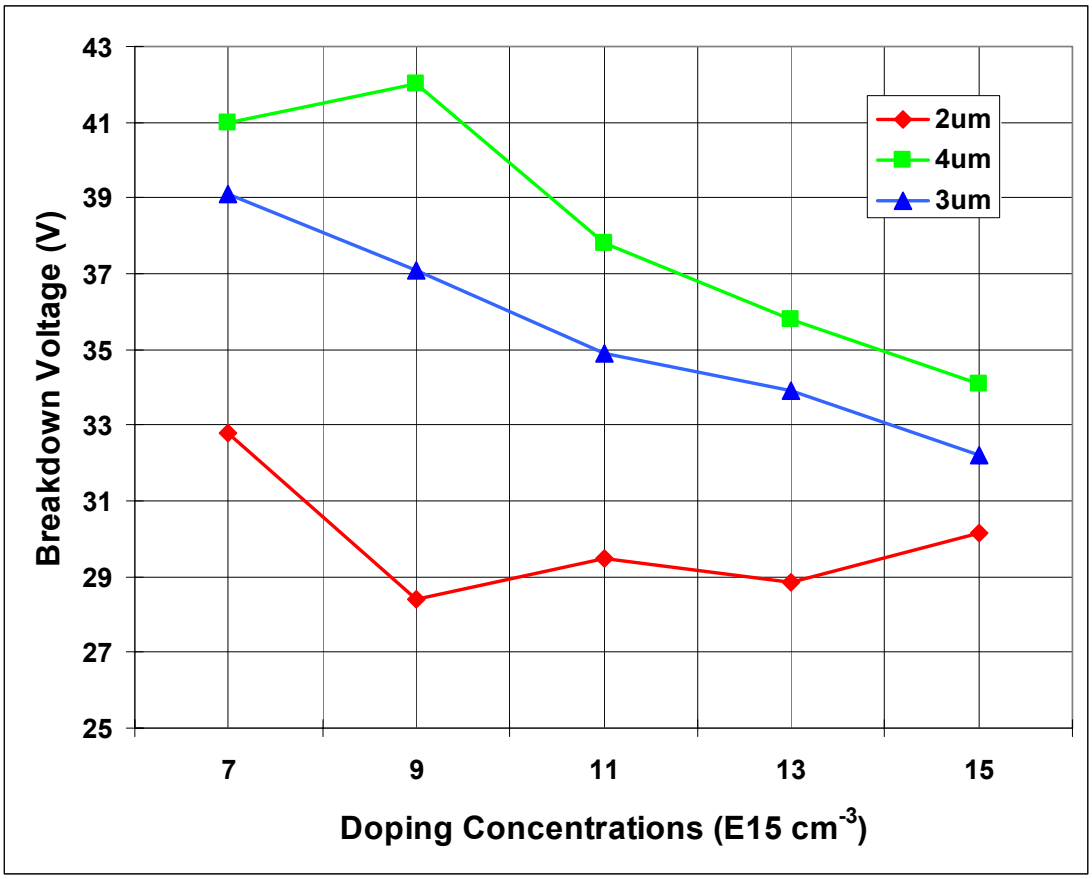

Figure 12: Breakdown Voltage vs. Doping Concentrations for devices with epi on P+ substrates

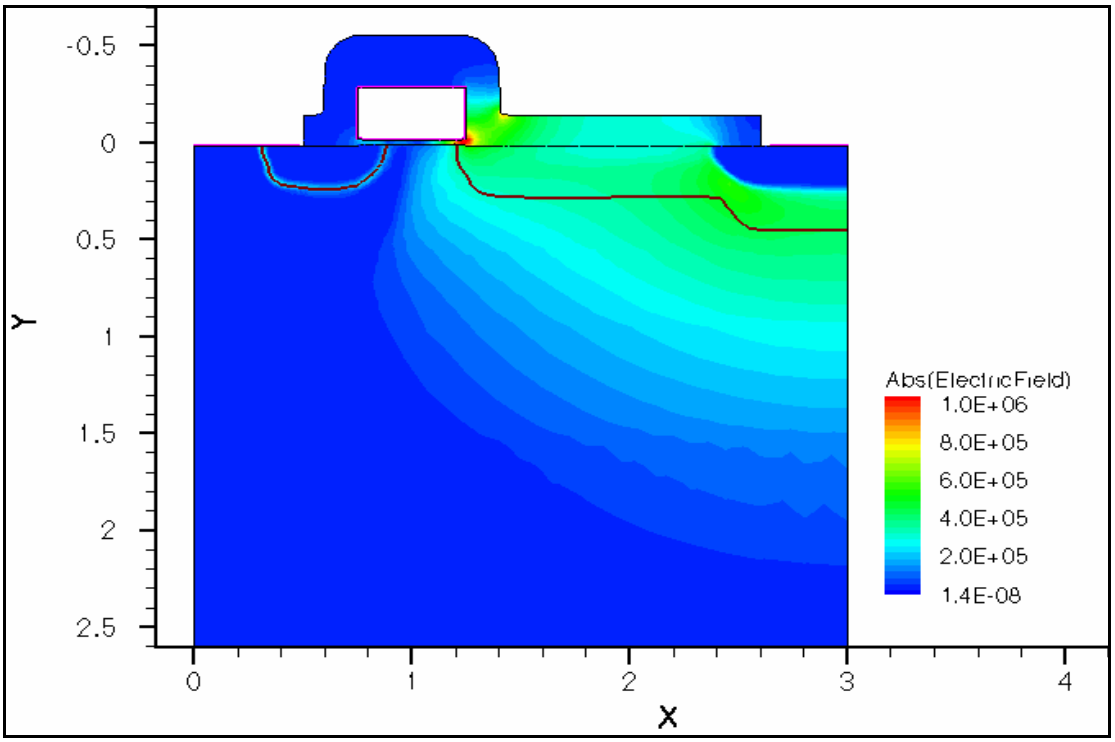

Figure 13: Electric Field Potential where breakdown occurs

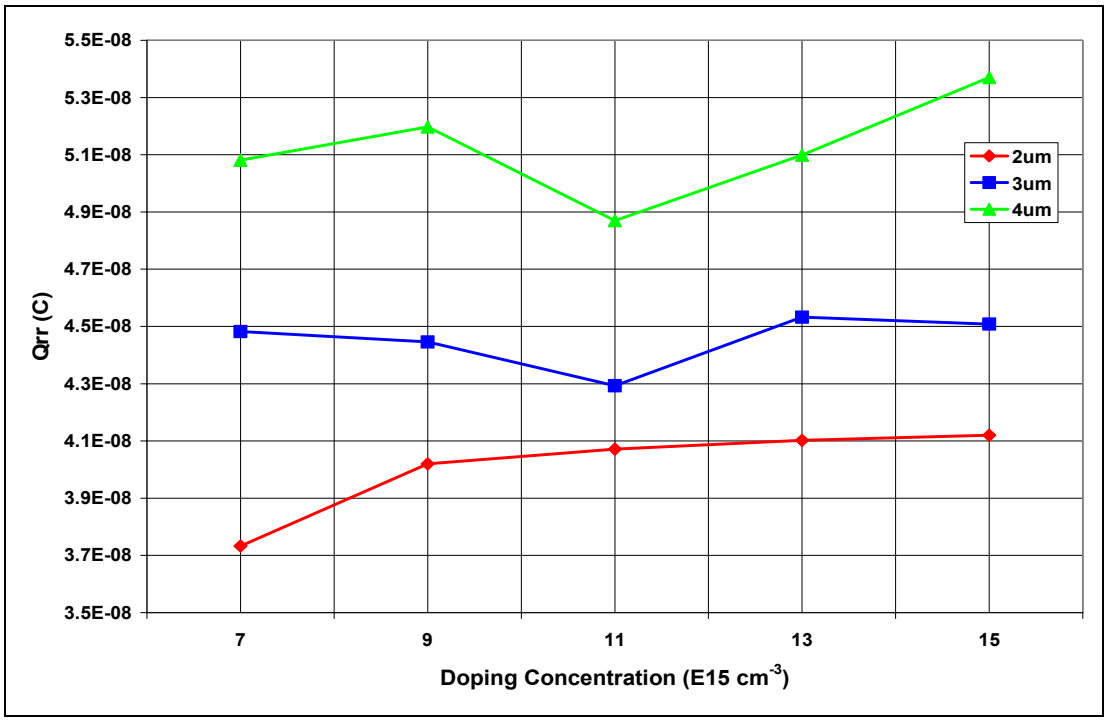

Figure 14: Qrr vs. Doping Concentrations for devices with epi on P+ substrates

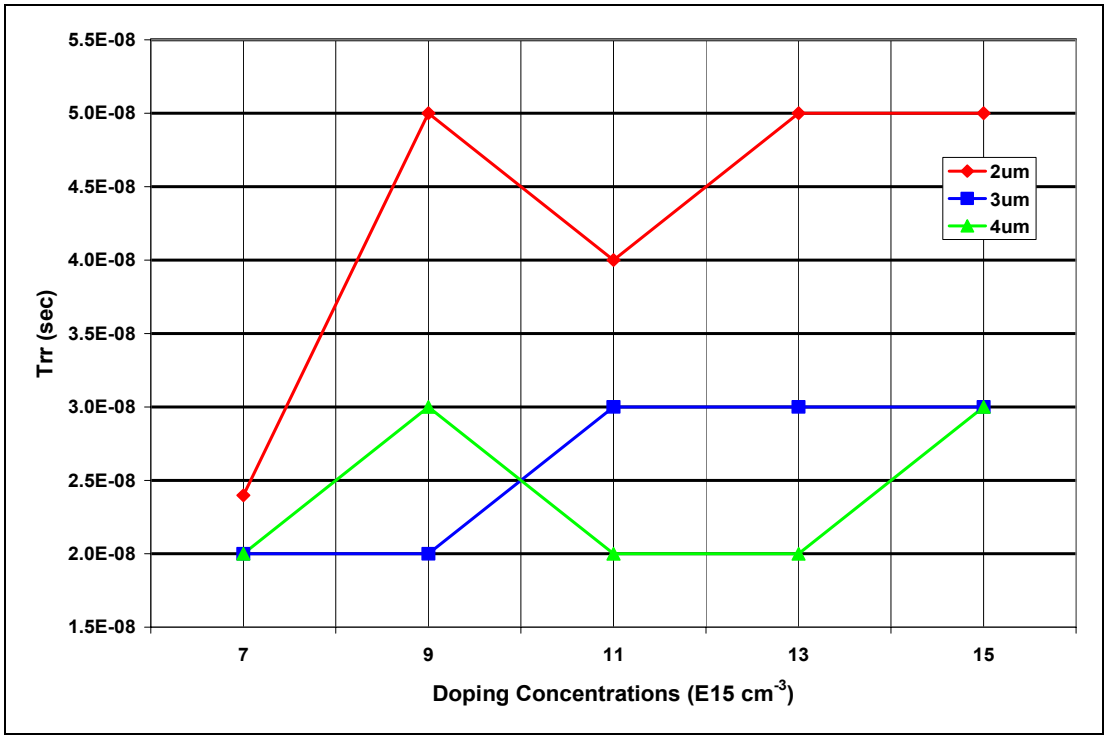

Figure 15: Trr vs. Doping Concentrations for devices with epi on P+ substrates

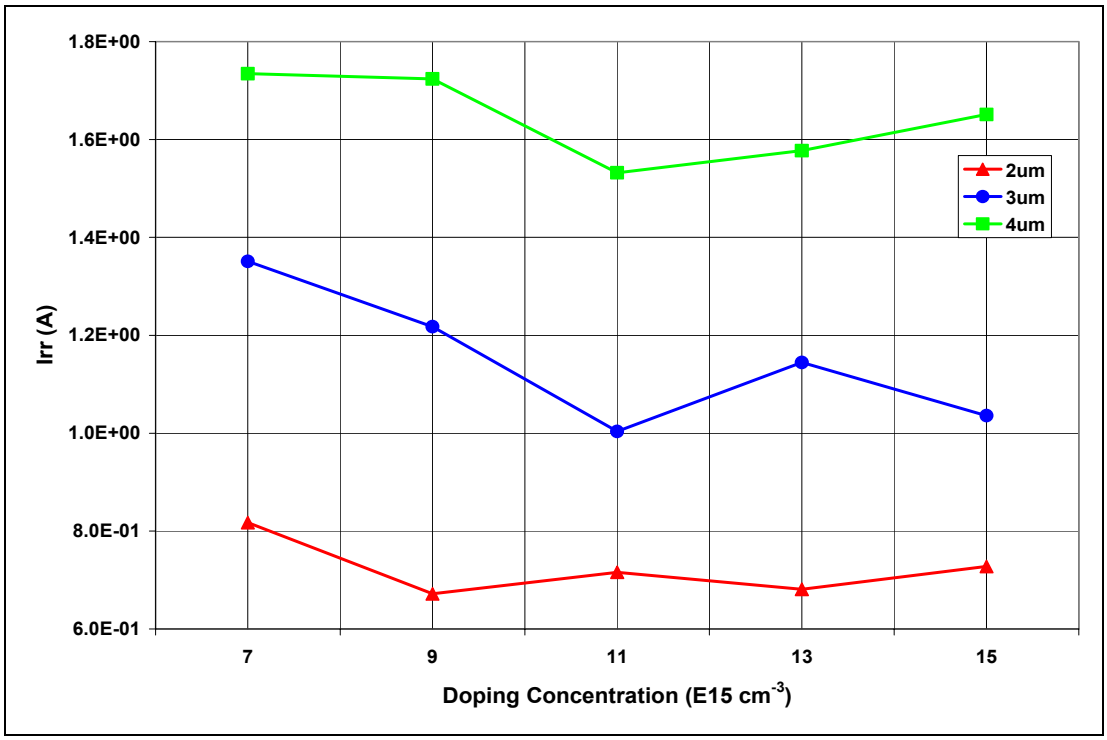

Figure 16: Irr vs. Doping Concentrations for devices with epi on P+ substrates

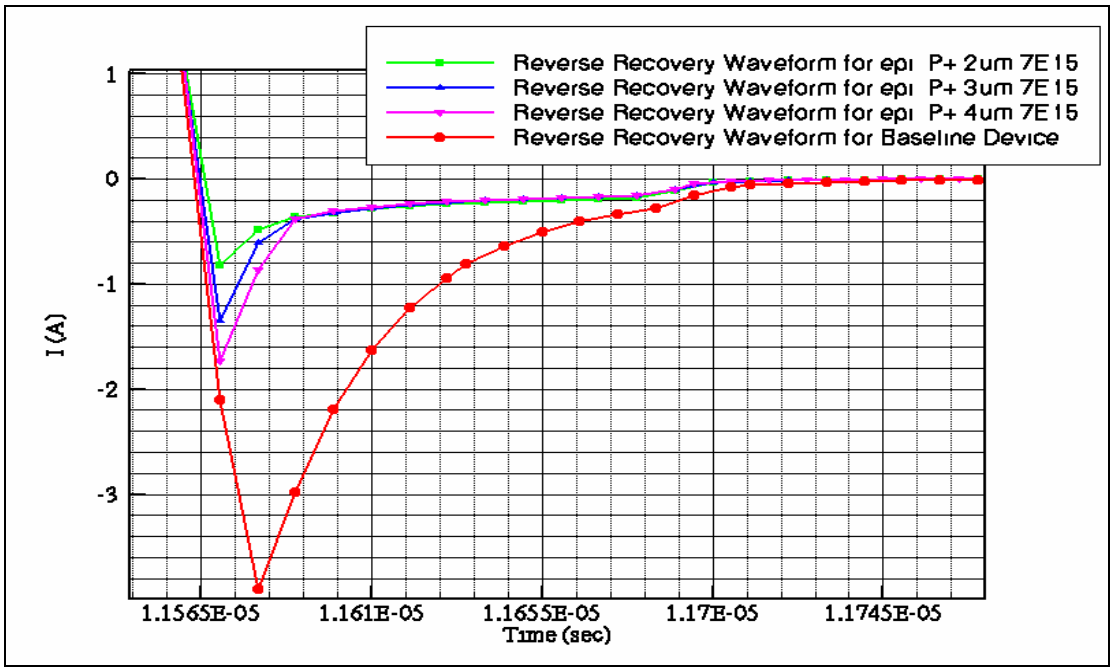

Figure 17: Reverse Recovery waveforms for LDMOS transistors with P epi layers with a doping concentration of 7E15 cm^{-3} of different thickness on P+ substrates

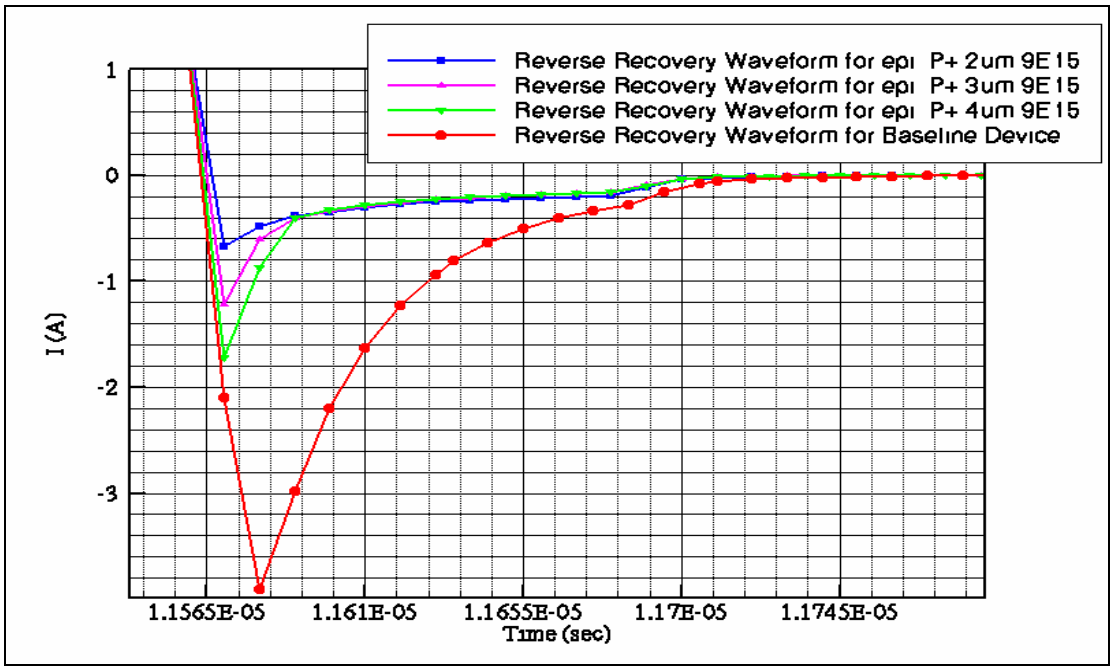

Figure 18: Reverse Recovery waveforms for LDMOS transistors with P epi layers with a doping concentration of 9E15 cm^{-3} of different thickness on P+ substrates

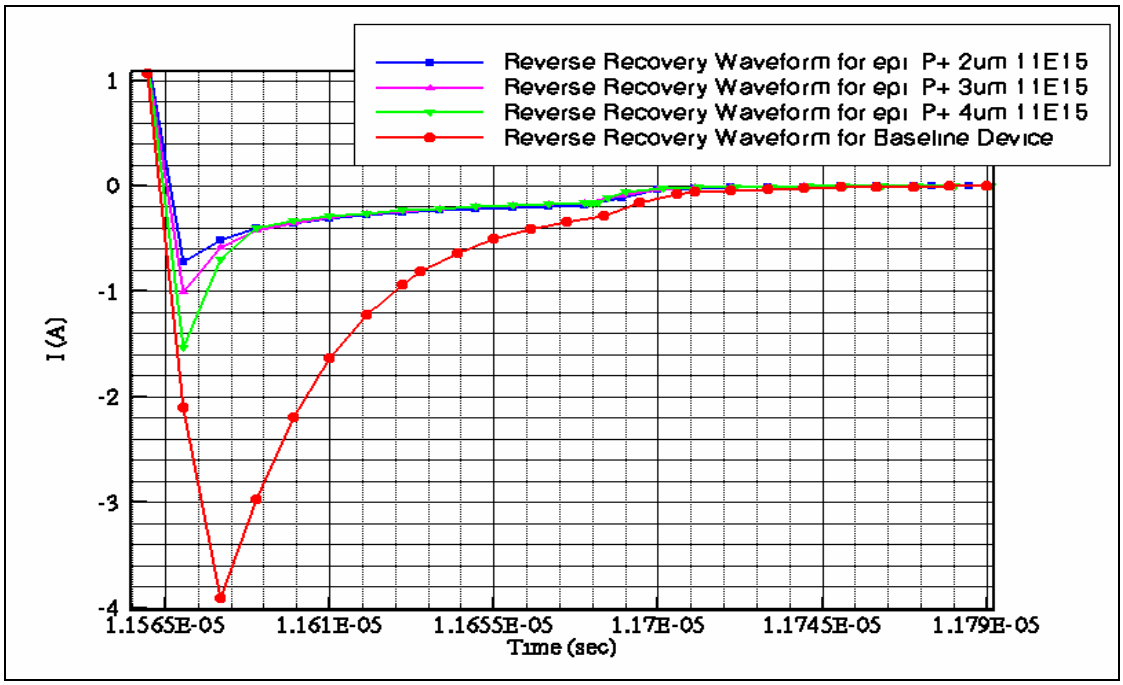

Figure 19: Reverse Recovery waveforms for LDMOS transistors with P epi layers with a doping concentration of 11E15 cm^{-3} of different thickness on P+ substrates

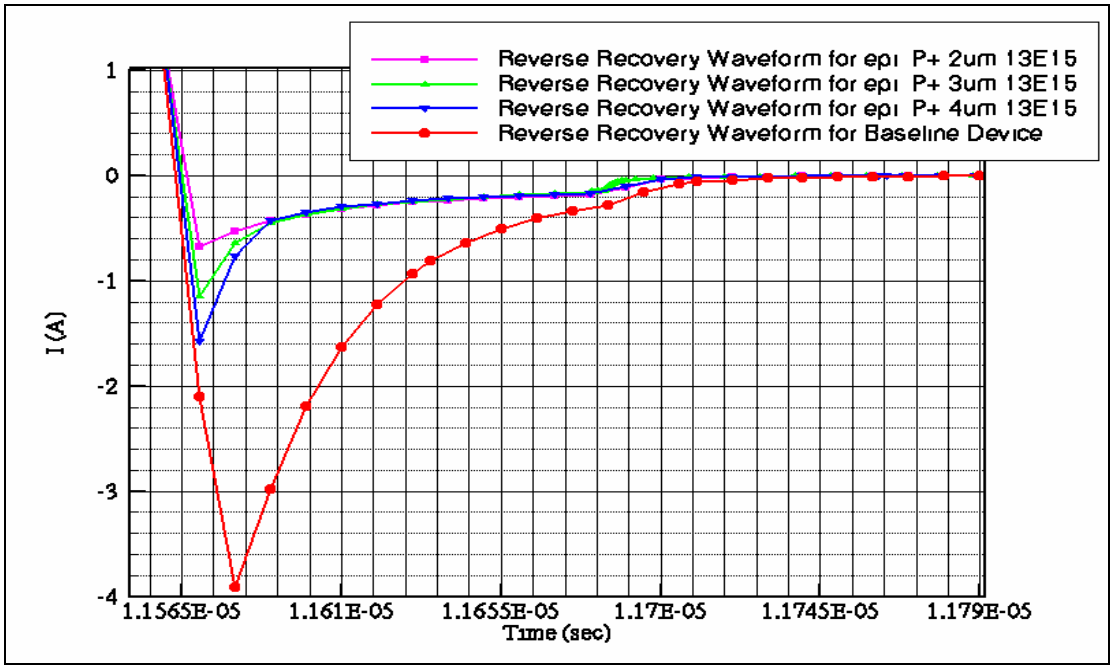

Figure 20: Reverse Recovery waveforms for LDMOS transistors with P epi layers with a doping concentration of 13E15 cm^{-3} of different thickness on P+ substrates

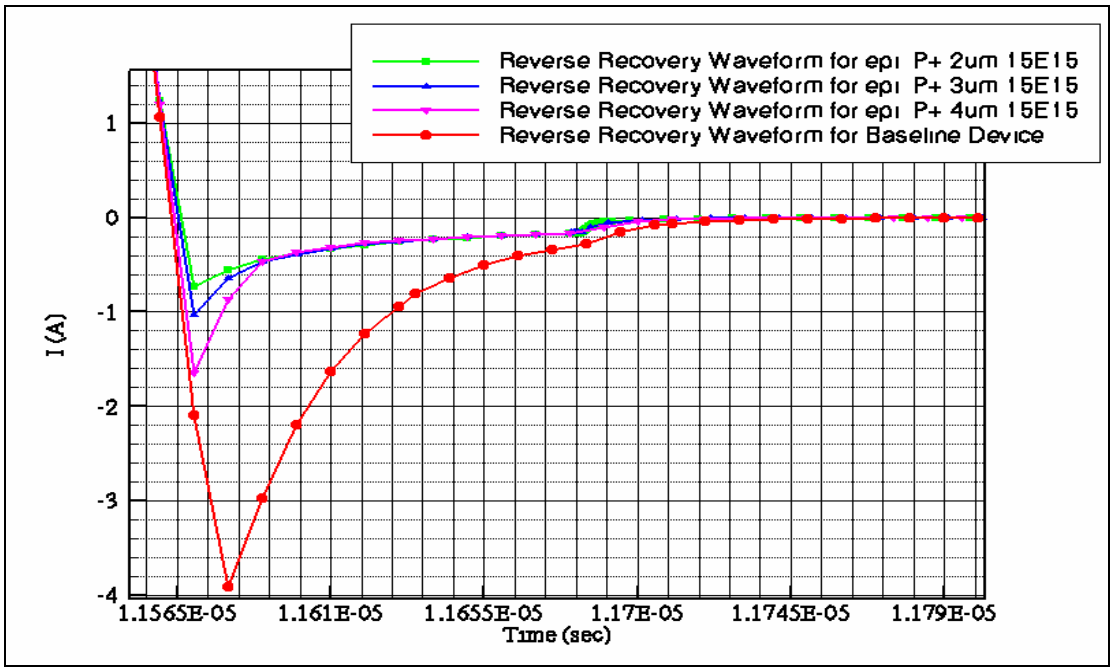

Figure 21: Reverse Recovery waveforms for LDMOS transistors with P epi layers with a doping concentration of 15E15 cm^{-3} of different thickness on P+ substrates

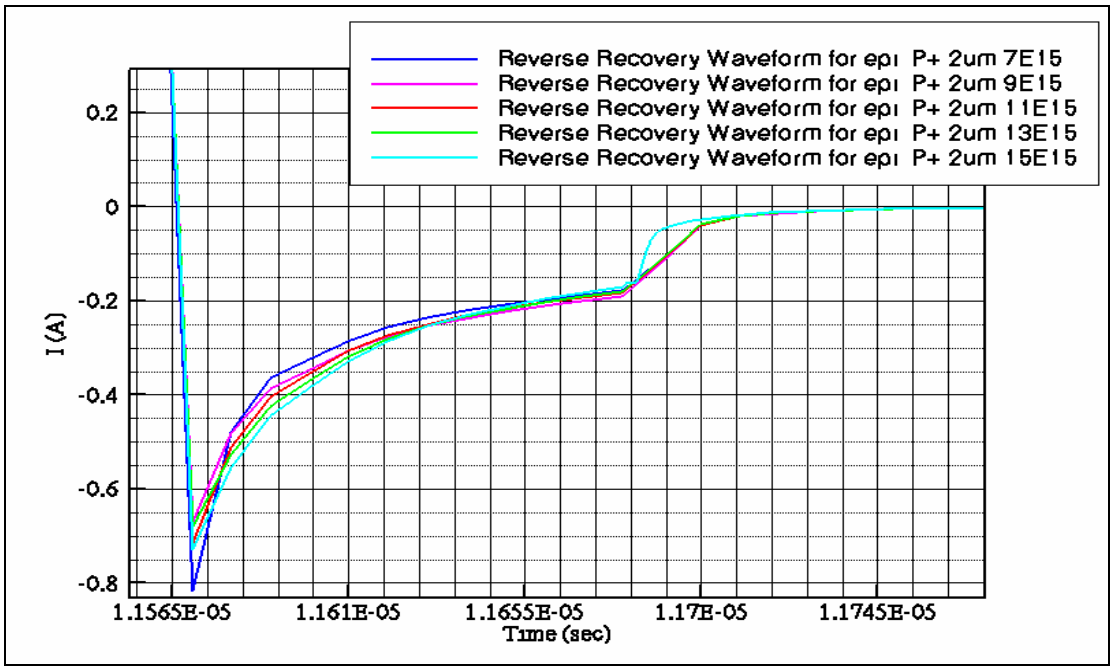

Figure 22: Reverse Recovery waveforms for LDMOS transistors with P epi layers with an epi thickness of 2µm for different doping concentrations on P+ substrates

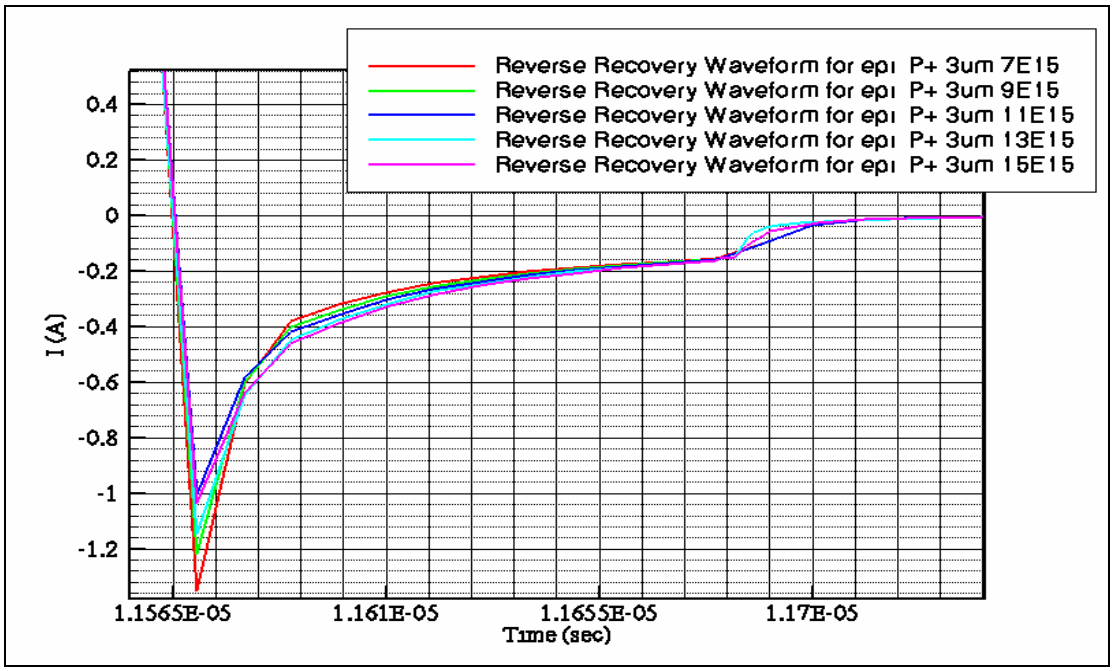

Figure 23: Reverse Recovery waveforms for LDMOS transistors with P epi layers with an epi thickness of 3µm for different doping concentrations on P+ substrates

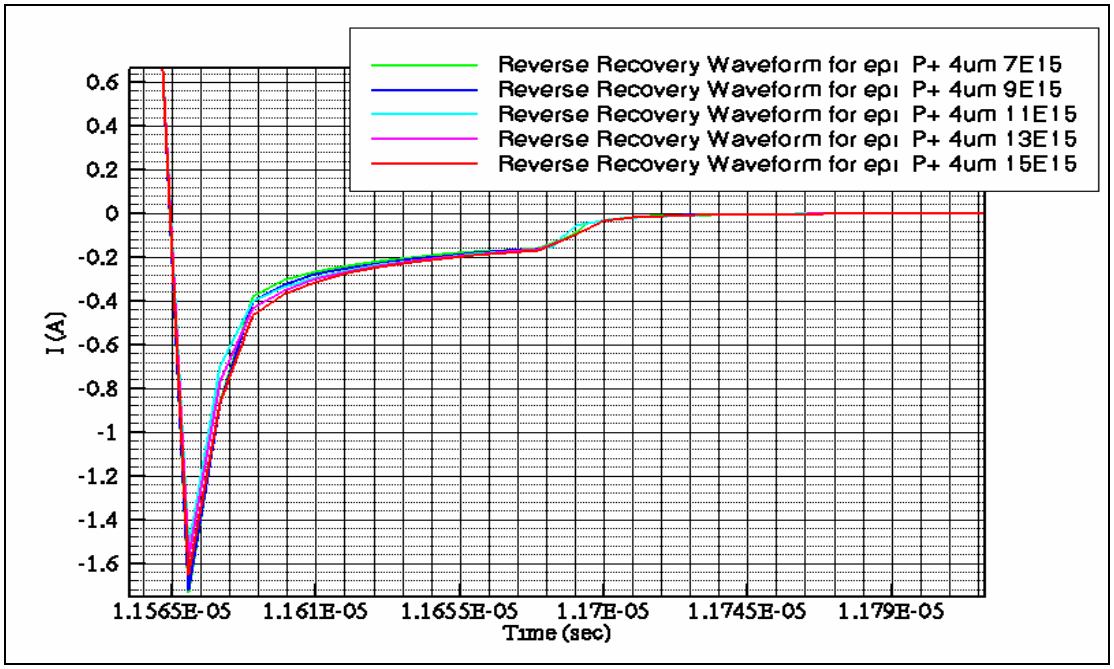

Figure 24: Reverse Recovery waveforms for LDMOS transistors with P epi layers with an epi thickness of 4µm for different doping concentrations on P+ substrates

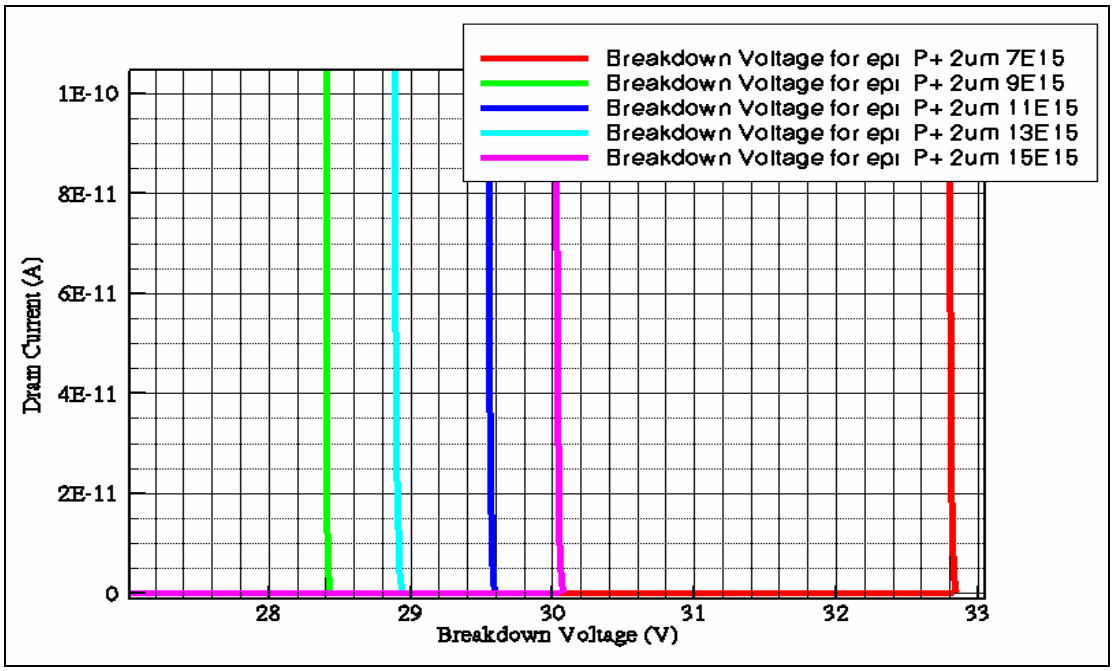

Figure 25: Breakdown Voltages for LDMOS transistors with P epi layers with an epi thickness of 2µm for different doping concentrations on P+ substrates

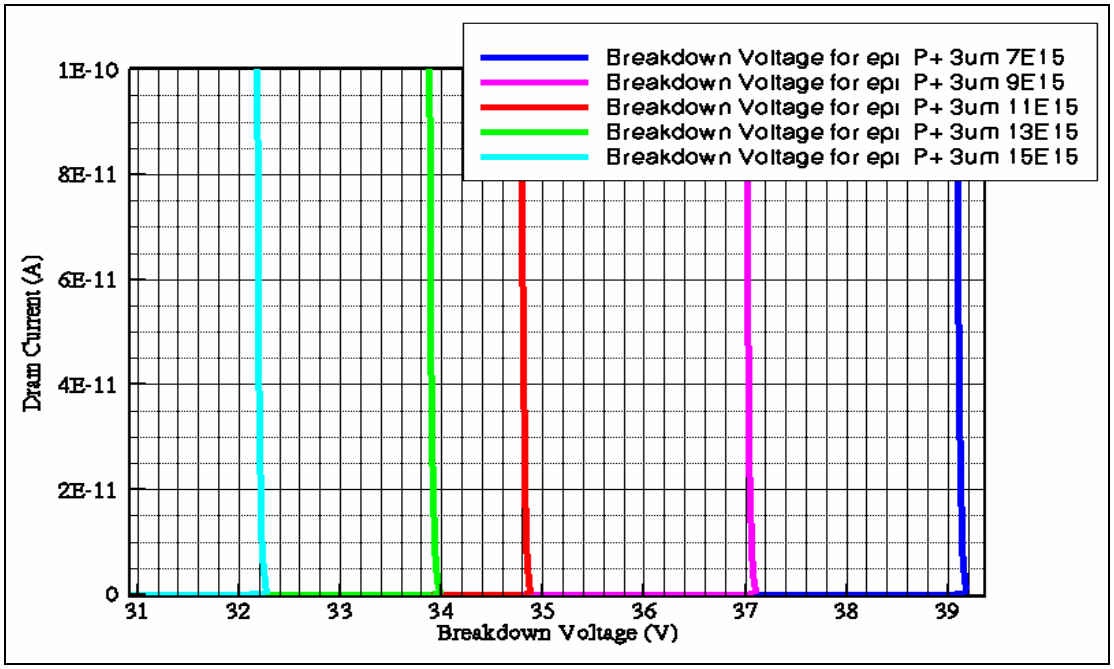

Figure 26: Breakdown Voltages for LDMOS transistors with P epi layers with an epi thickness of 3µm for different doping concentrations on P+ substrates

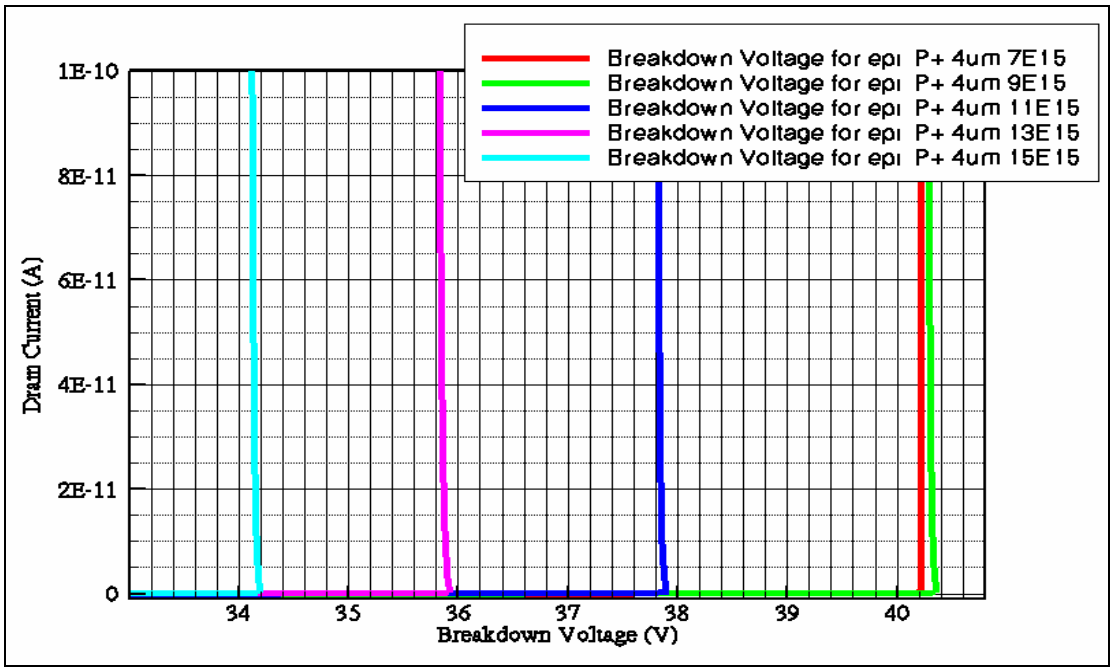

Figure 27: Breakdown Voltages for LDMOS transistors with P epi layers with an epi thickness of 4µm for different doping concentrations on P+ substrates

B LDMOS Transistor with P Substrate and SOI layer

The results from this solution were a little different than expected but did show some promising results which will lead to other variations of this solutions. The SOI layer was expected to also serve as a barrier for the depletion region, which it did. The result that was different from before was as the distance from the N+ region and the top of the SOI layer increased the breakdown voltage did not also increase. This is probably due to the fact that the region between the N+ and SOI layer is only doped with 1E15 P substance. This smaller doping concentration also caused the breakdown voltage of all three variations of the solution to be below the 30V minimum breakdown voltage requirement. See Figure 28 and Figure 34 for a graphical comparison of the breakdown voltages for each variation of this solution and the baseline device. Figure 29 shows the electric field potential when breakdown occurs. As the electric field goes up the region becomes “hotter”.

This device did show promising results as far as the reverse recovery characteristics are concerned. As the region between the N+ layer and SOI layer became smaller the reverse recovery characteristics also became smaller. This follows the same logic that was talked about previously, as the region between the N+ layer and the SOI layer becomes less so does the amount of charge that can be stored in that region. The more charge that is in the region the longer the reverse recovery time will be and the larger the reverse recovery charge (Qrr) will be. The best performing device as far as Qrr is concerned is the device with an SOI layer a distance of 2μm from the N+ region. This device compared to the baseline device showed a 79.7% improvement in reverse recovery charge. Figure 30 thru Figure 32 show different comparisons between Qrr and

SOI layer distances, Trr and SOI layer distances, and Irr and SOI layer distances. Figure 33 shows the reverse recovery waveforms decreasing in size as the distance between the SOI layer and N+ region decreases in size. This figure also compares the reverse recovery waveform of the baseline device with that of the solutions with different SOI distances from the N+ region. Huge improvement in the reverse recovery characteristics can be seen.

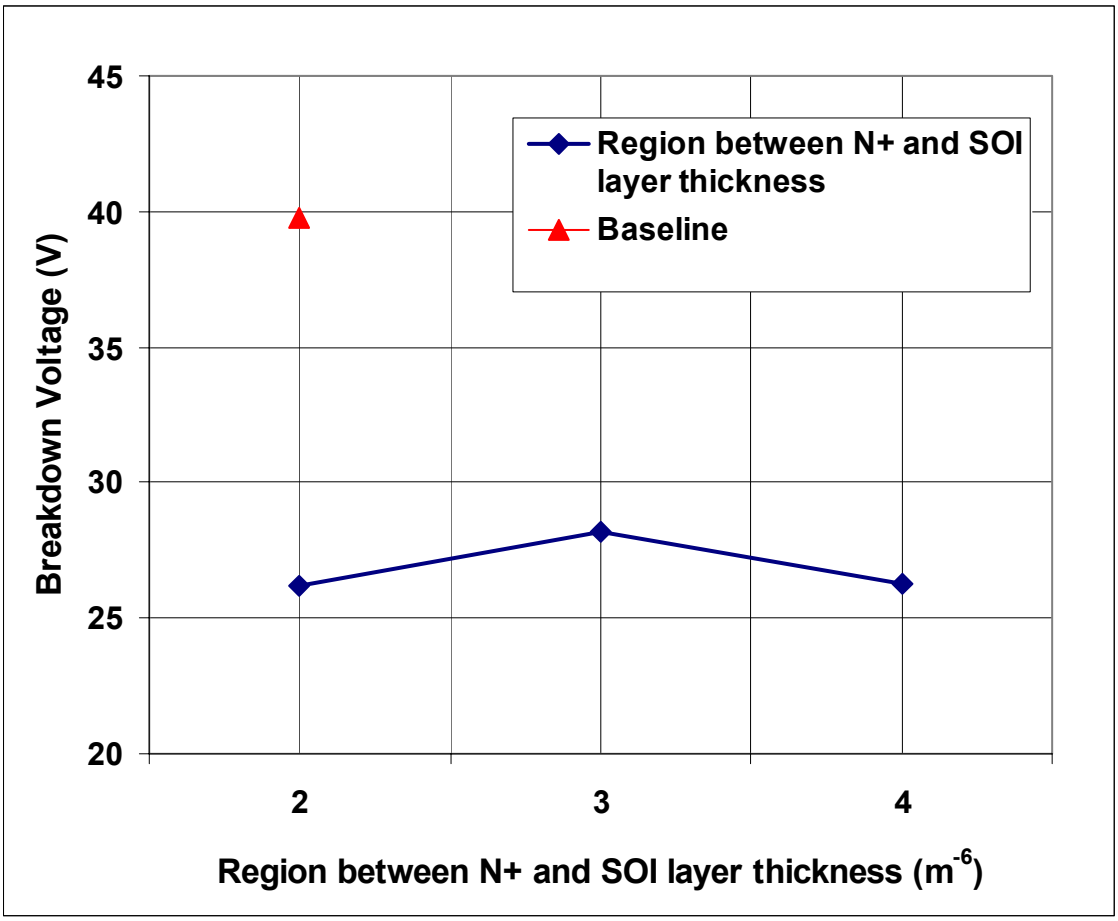

Figure 28: Breakdown Voltage vs. Region between N+ and SOI layer for SOI layer Device

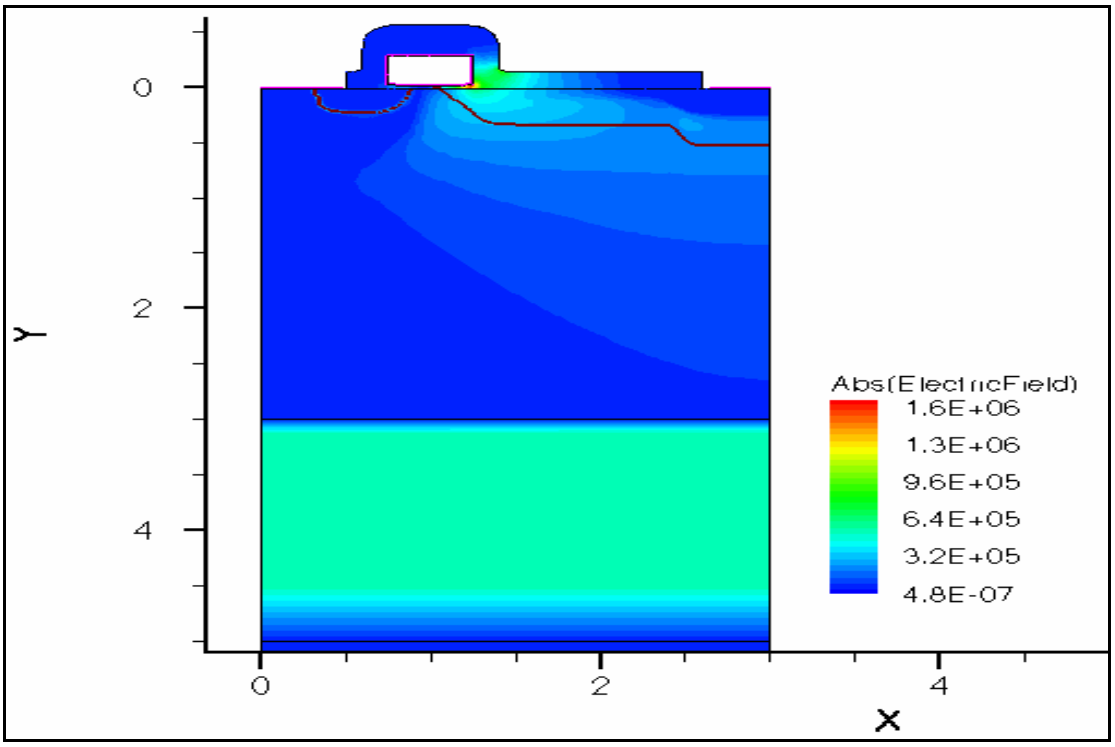

Figure 29: Electric Field Potential where breakdown occurs

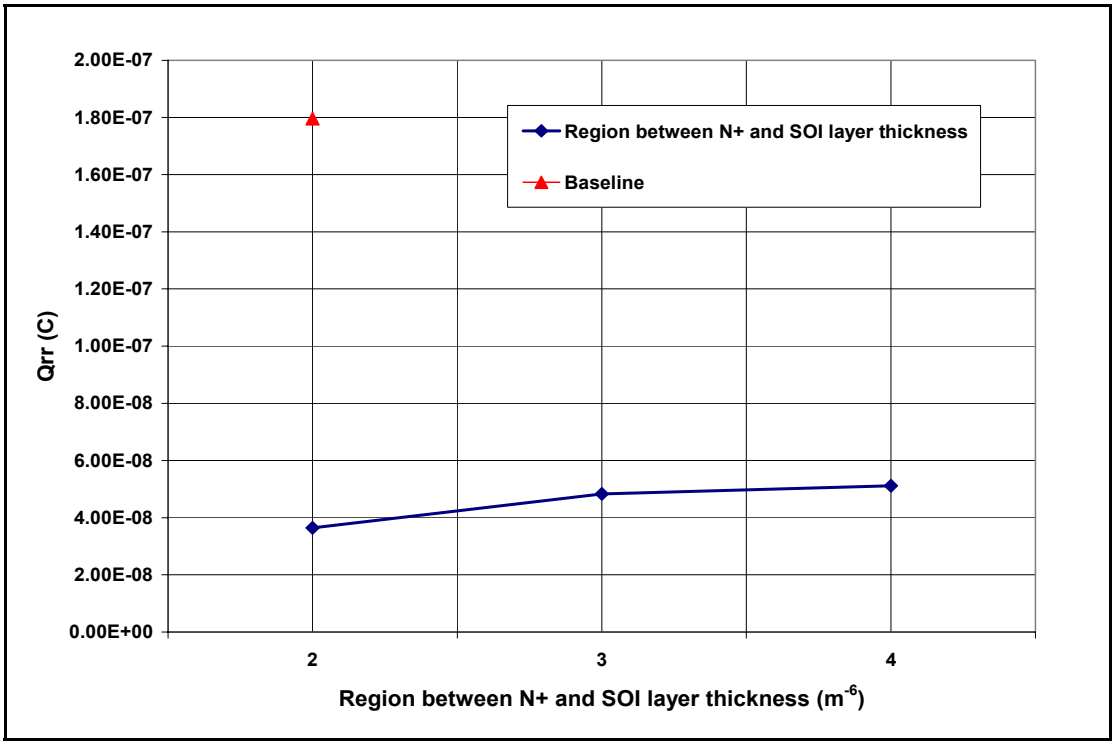

Figure 30: Qrr vs. Region between N+ and SOI layer for SOI layer Device

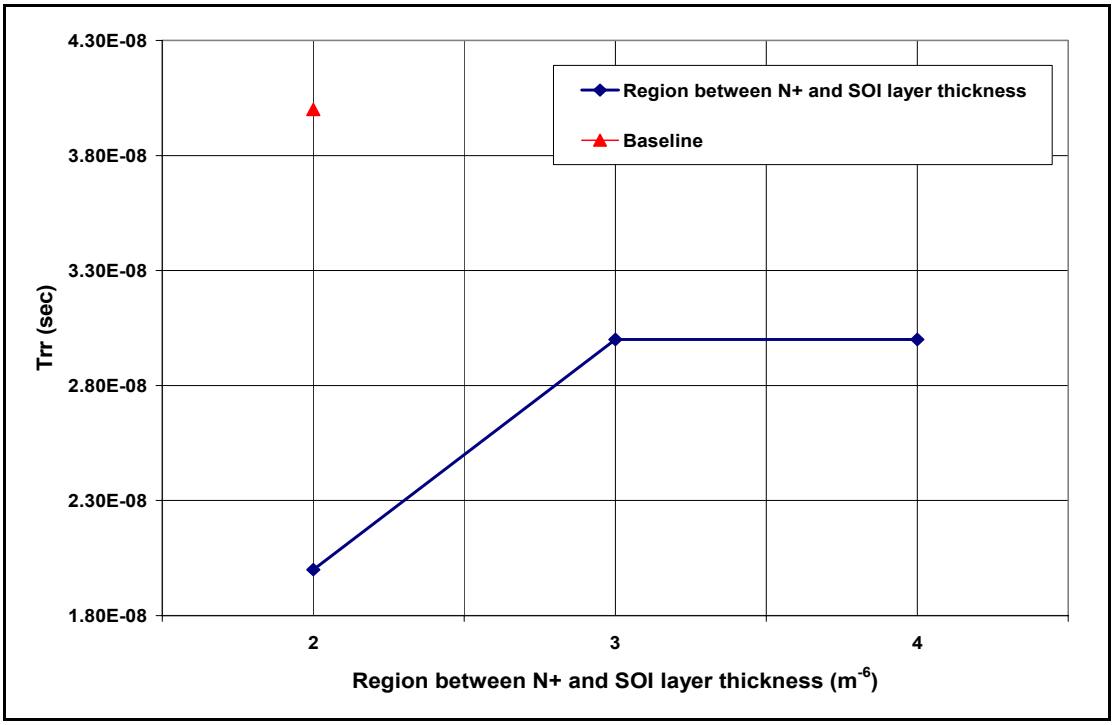

Figure 31: Trr vs. Region between N+ and SOI layer for SOI layer Device

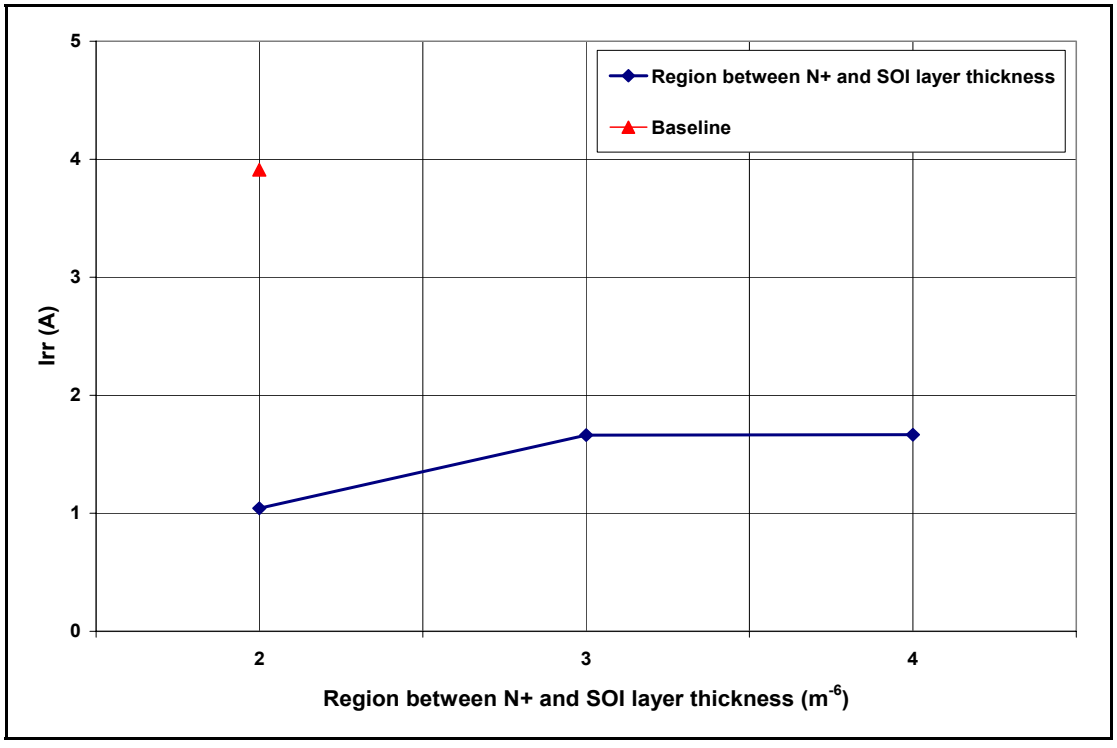

Figure 32: Irr vs. Region between N+ and SOI layer for SOI layer Device

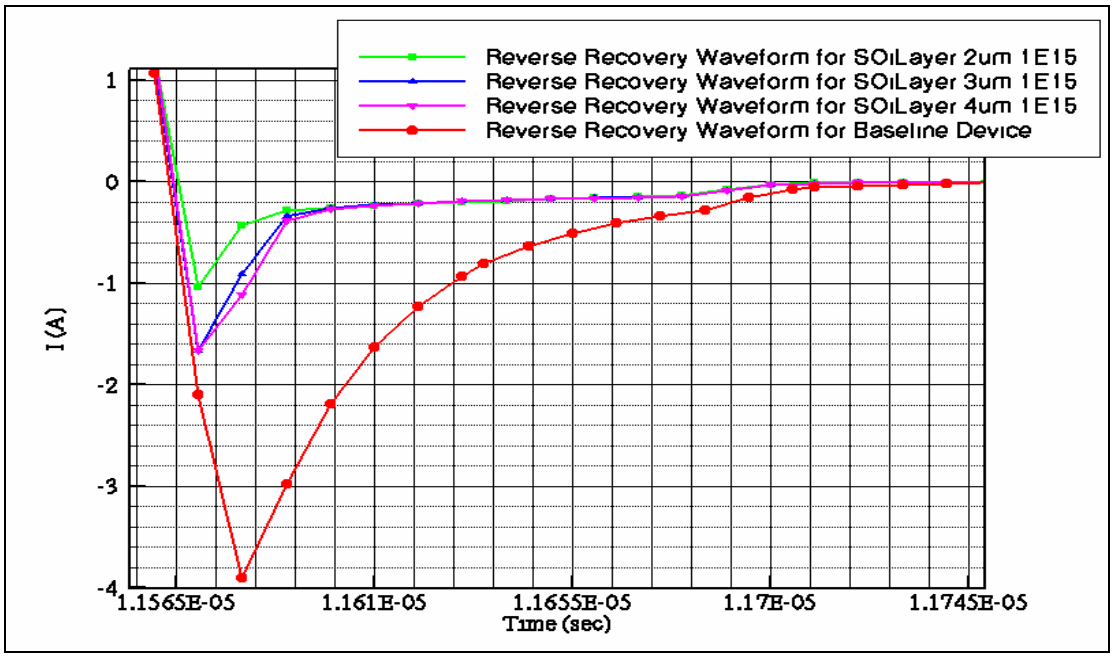

Figure 33: Reverse Recovery waveforms for LDMOS transistors with SOI layers of different distances from the N+ region on P substrates

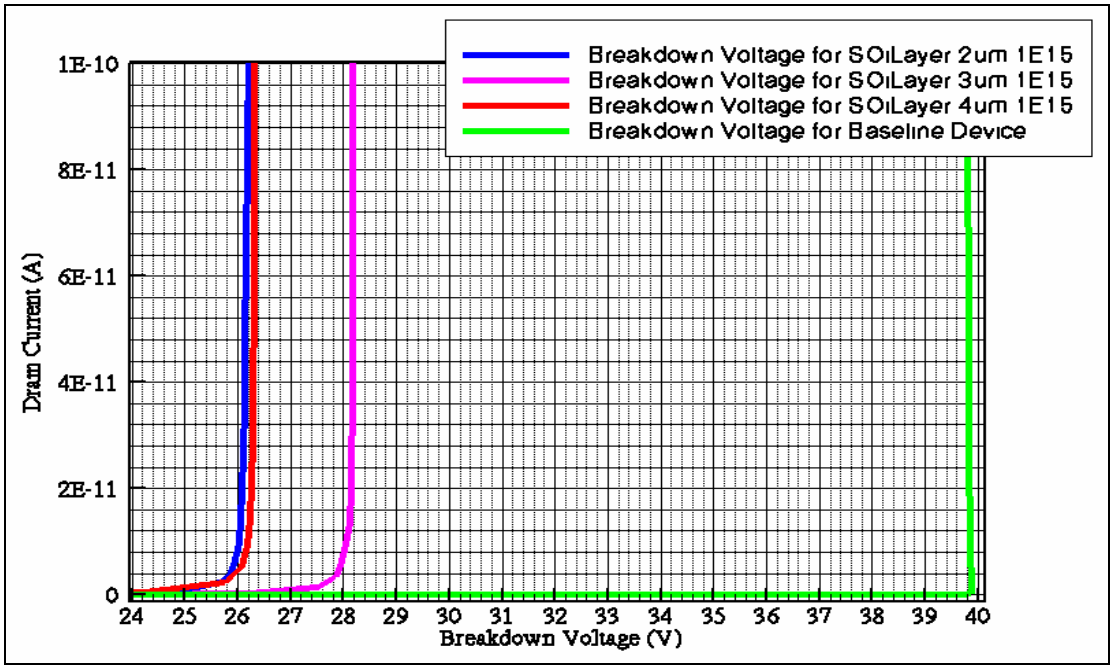

Figure 34: Breakdown Voltages for LDMOS transistors with SOI layers of different distances from the N+ region on P substrates

C LDMOS Transistor with P Substrate, SOI layer, and P Epi Layer

This solution combined the first two solutions together but made the substrate with a P doping instead of a P+. This combination provided unique results of its own. As the epitaxial layer thickness decreased in size from 4µm to 2µm the breakdown voltages started to increase and then decreased. This solution seems to have a "sweet spot" for the epi layer thickness if breakdown voltage is only considered. Another difference that should be pointed out is in the first solution the breakdown voltages were spread out across a larger range than this solution provides. Also all of the variations provide at least the 30V minimum requirement. The best performing device as far as the one with the highest breakdown voltage goes is the one with an epi layer that has a doping concentration of 9E15 cm^{-3} and a thickness of 3µm. See Figure 35 for a comparison of all of the doping concentration variations with the epi thickness assigned. Figure 48 thru Figure 50 also show the breakdown voltages for each device in this category of solution. Figure 36 shows the electric field potential when breakdown occurs. As the electric field goes up the region becomes "hotter".

This combination showed the same results for decreasing the reverse recovery characteristics as the previous two solutions. As the epi layer thickness became smaller the reverse recovery characteristics also became smaller. The best performing device as far as reverse recovery charge (Qrr) is concerned is the device with an epi layer that has a doping concentration of 9E15 cm^{-3} and a thickness of 2µm. This device compared to the baseline device showed a 77% improvement in reverse recovery charge. This percentage was a little less than the previous two solutions but is still above the goal of 75% reduction in reverse recovery characteristics. Figure 37 thru Figure 39 show different

comparisons between Qrr and doping concentrations, Trr and doping concentrations, and Irr and doping concentrations. Figure 40 thru Figure 44 shows the reverse recovery waveforms decreasing in size as the epitaxial layer decreases in size. These figures also compare the reverse recovery waveform of the baseline device with that of the solutions with different epi thicknesses. A dramatic improvement in the reverse recovery characteristics can be seen. Figure 45 thru Figure 47 show the reverse recovery waveforms for each epi layer thickness but with varied doping concentrations. The doping concentration in this solution doesn't play a large role in reducing the reverse recovery characteristics.

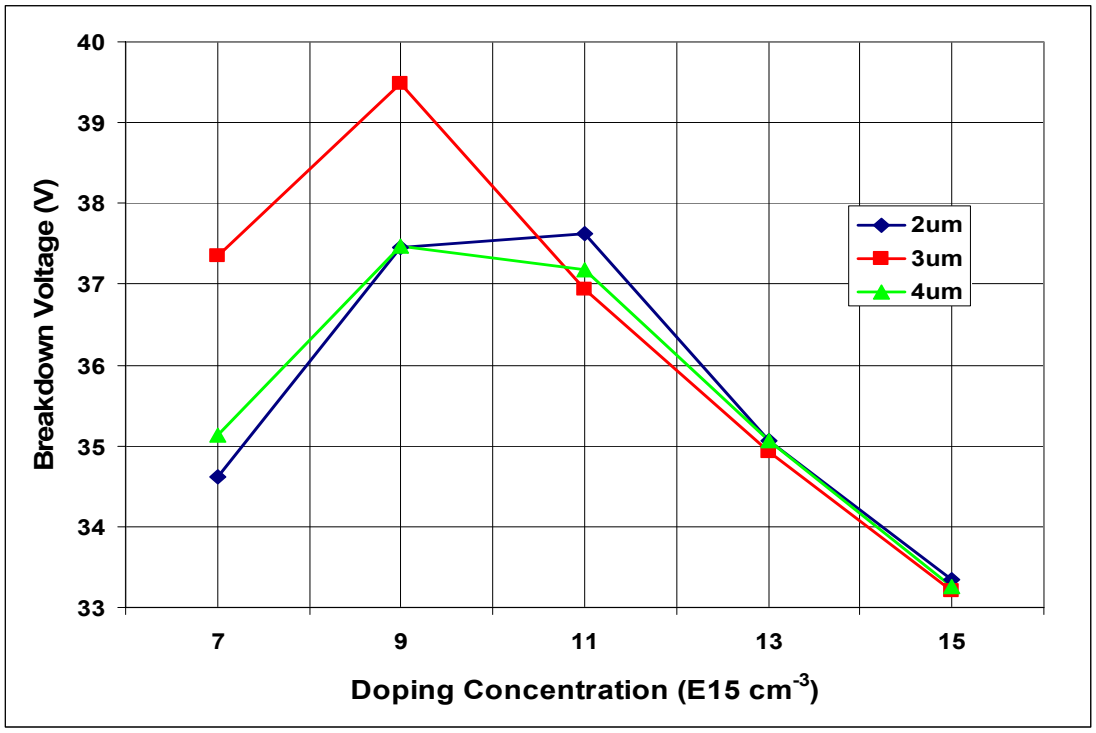

Figure 35: Breakdown Voltage vs. Doping for SOI layer Device with P epi on 1E15 Substrate

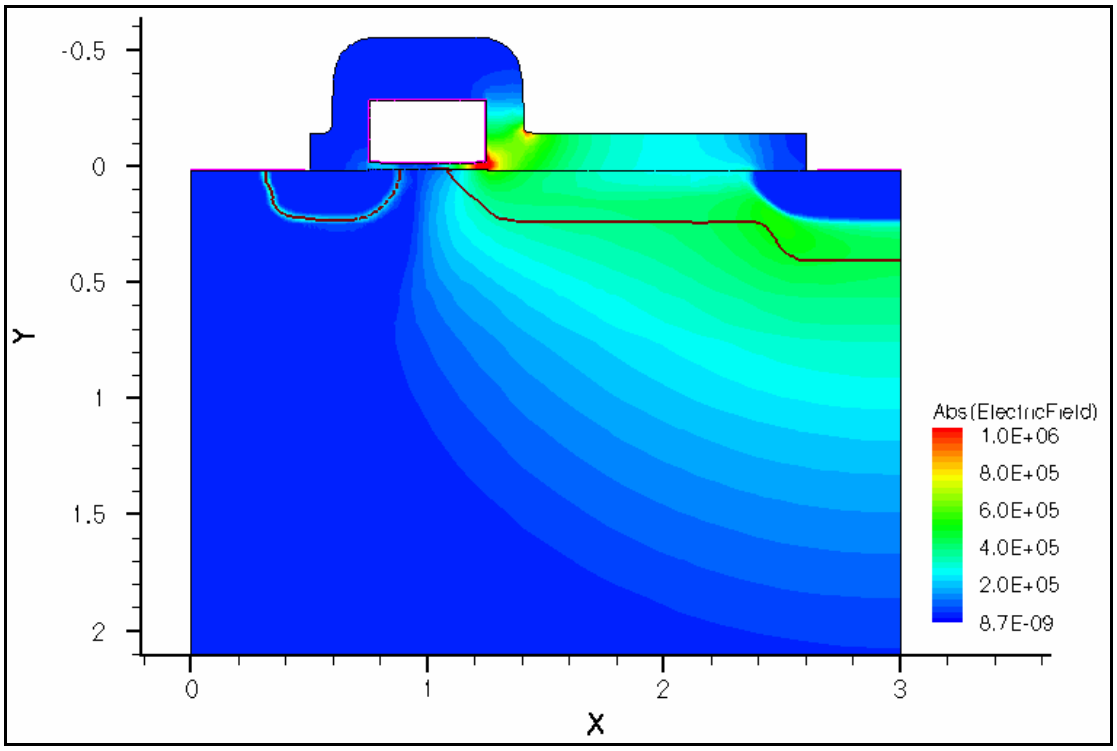

Figure 36: Electric Field Potential where breakdown occurs

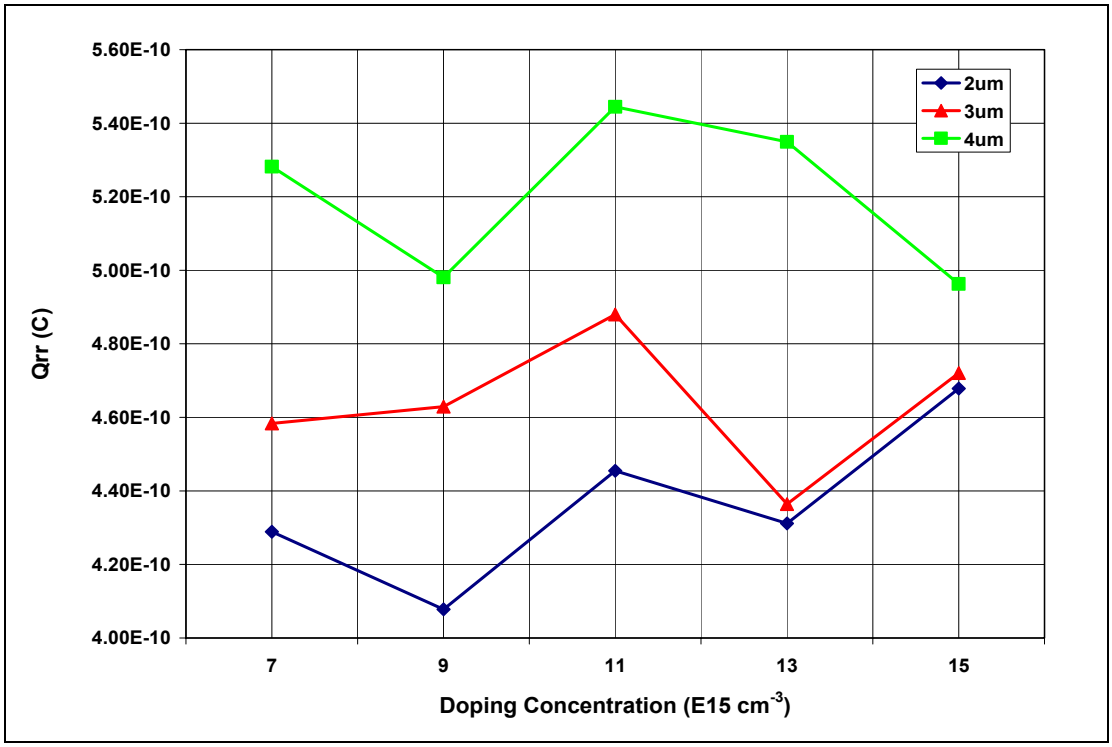

Figure 37: Qrr vs. Doping Concentrations for SOI layer Device with P epi on 1E15 Substrate

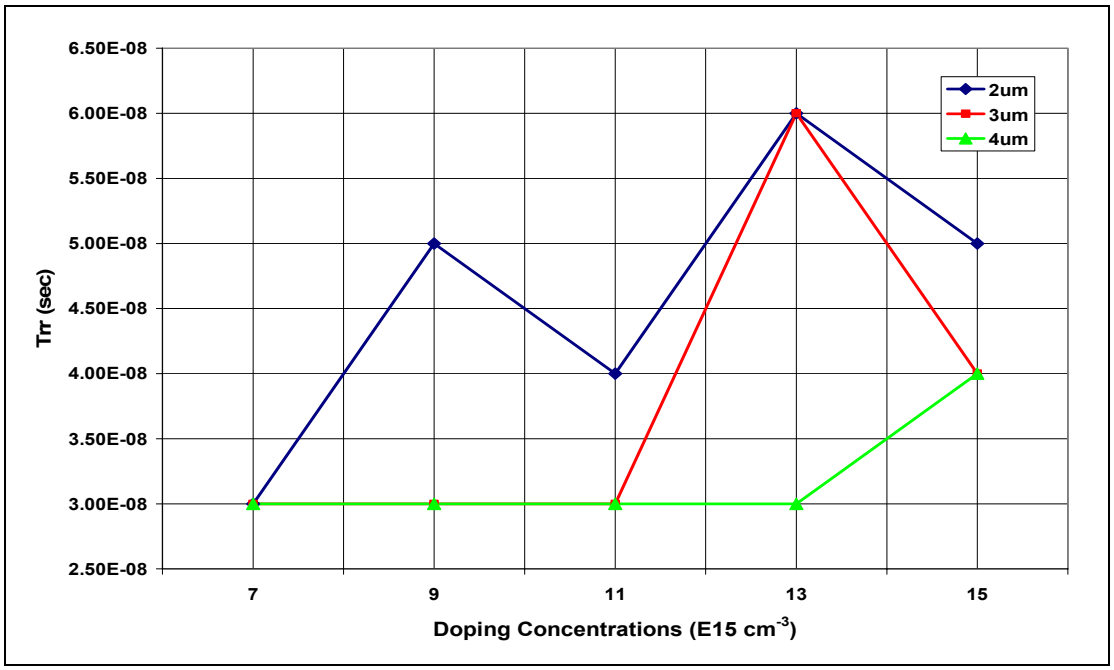

Figure 38: Trr vs. Doping Concentrations for SOI layer Device with P epi on 1E15 Substrate

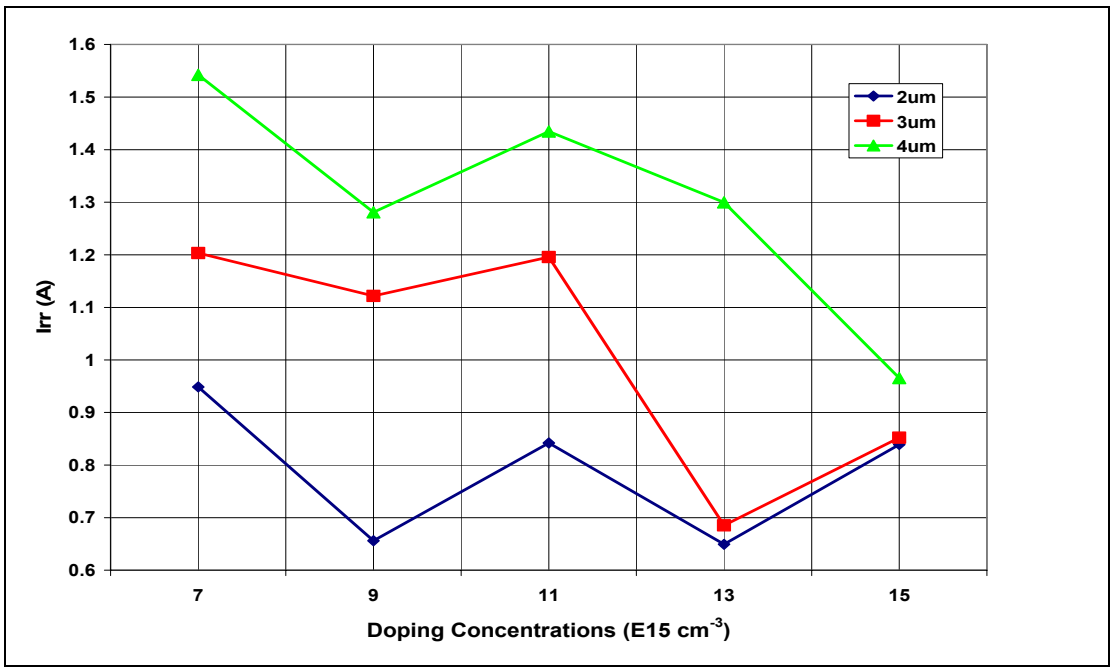

Figure 39: Irr vs. Doping Concentrations for SOI layer Device with P epi on 1E15 Substrate

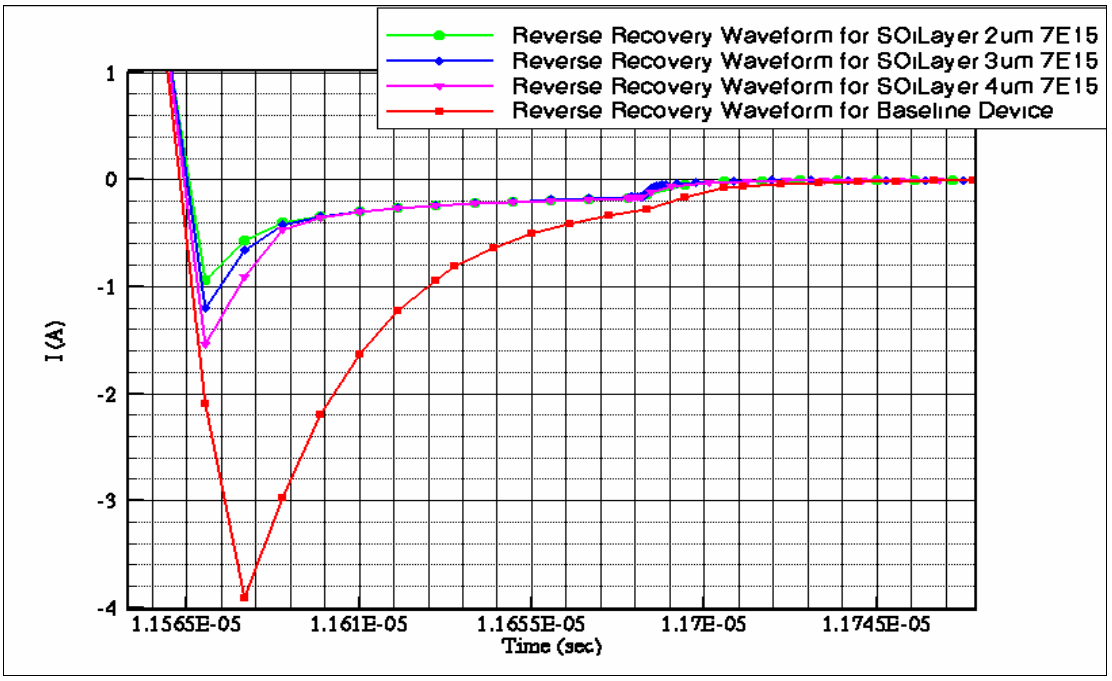

Figure 40: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 7E15 cm^{-3} of different thickness on P substrates

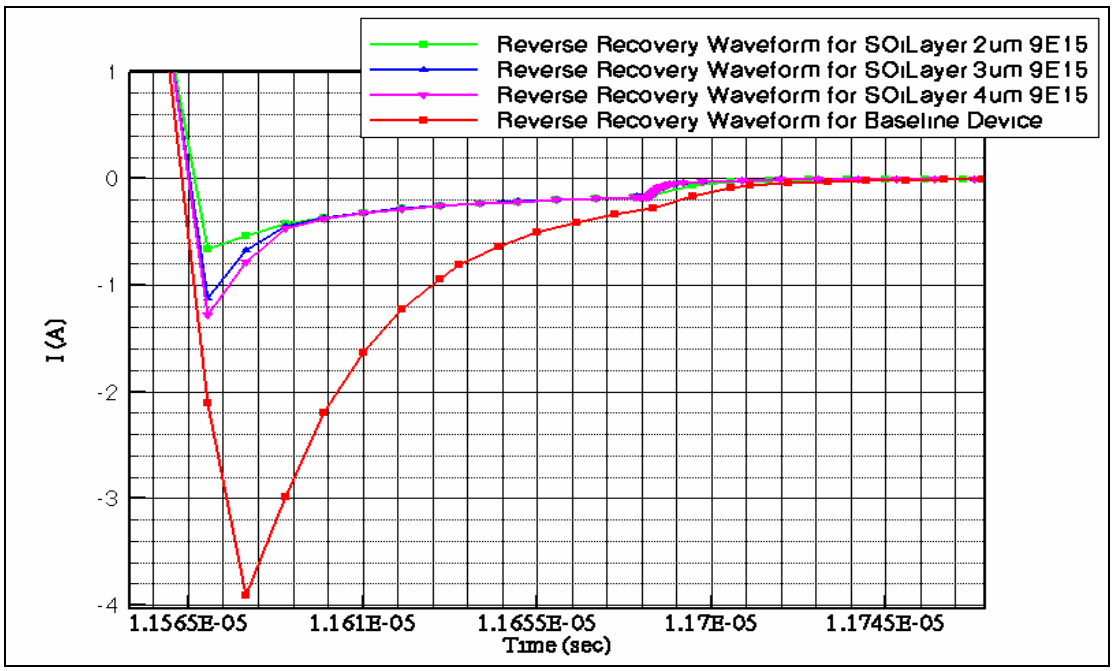

Figure 41: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 9E15 cm^{-3} of different thickness on P substrates

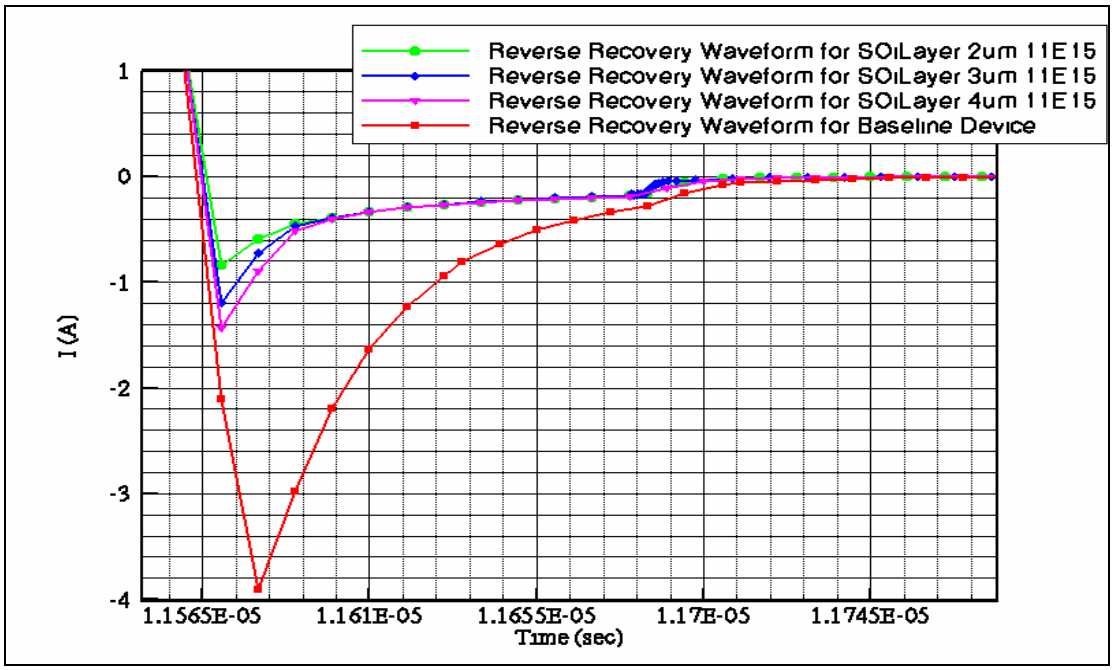

Figure 42: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 11E15 cm^{-3} of different thickness on P substrates

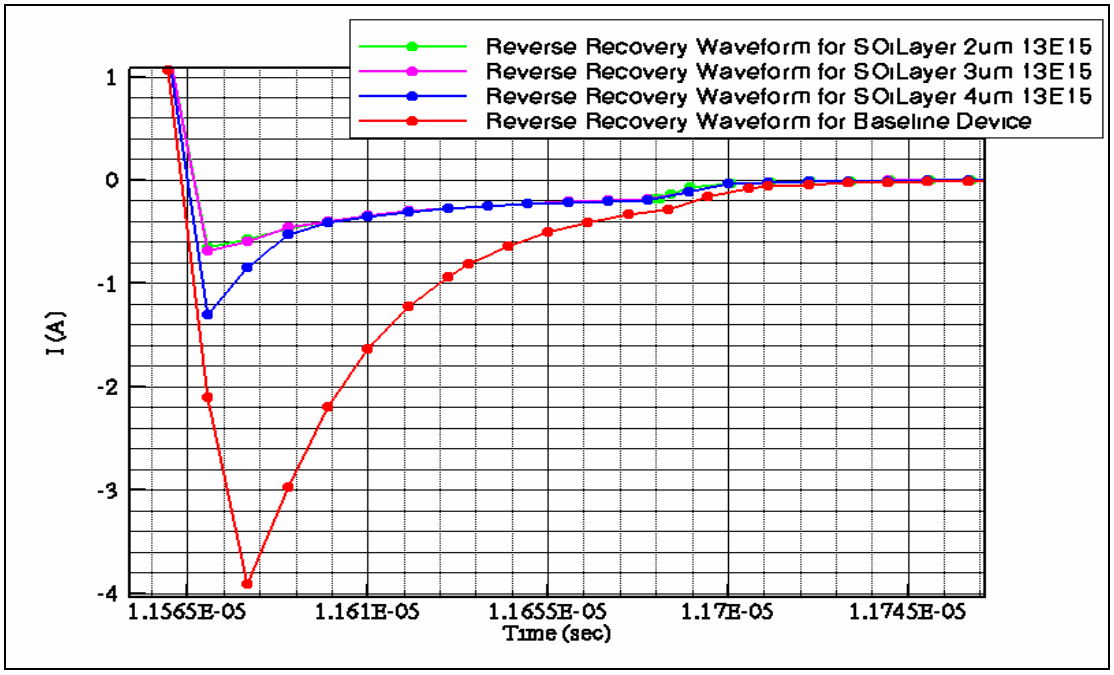

Figure 43: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 13E15 cm^{-3} of different thickness on P substrates

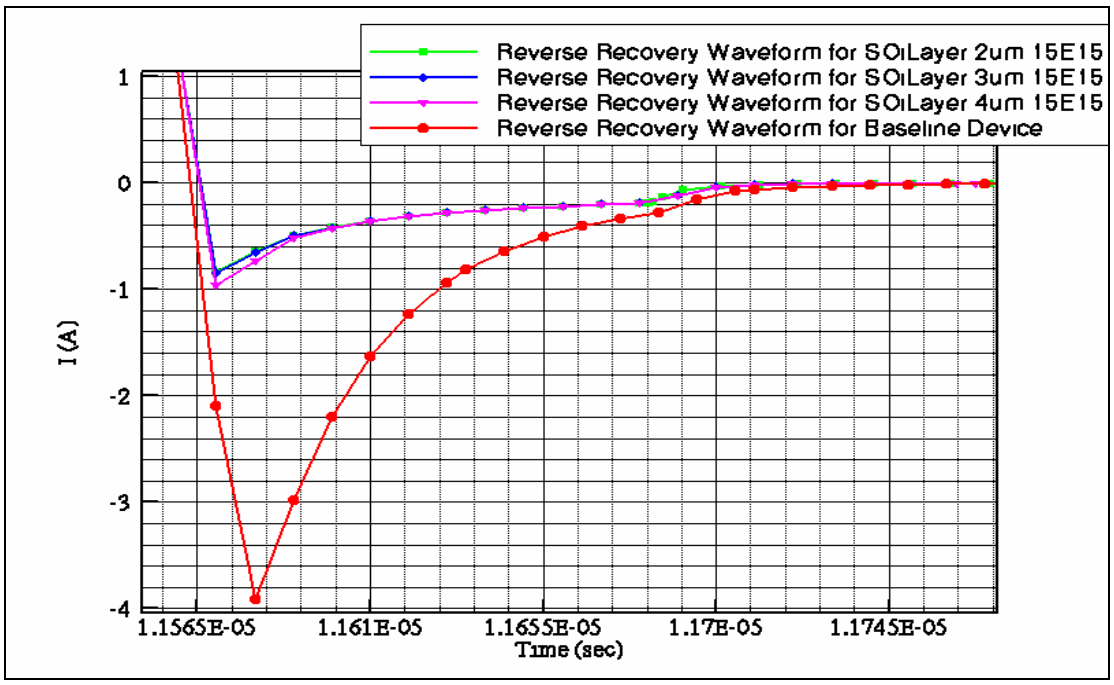

Figure 44: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 15E15 cm^{-3} of different thickness on P substrates

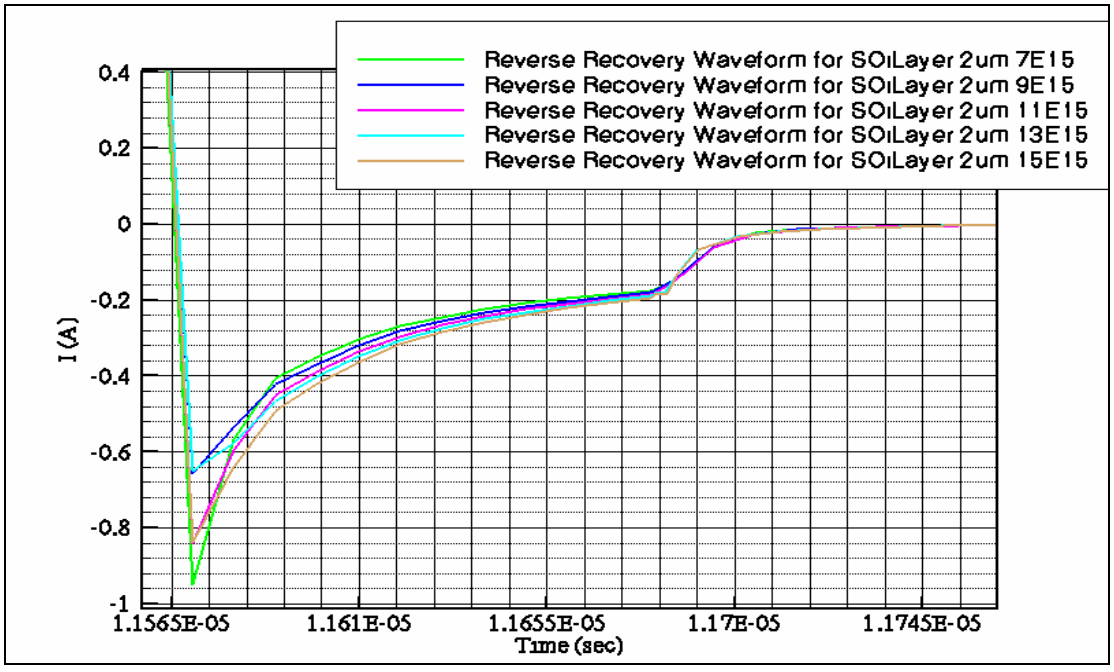

Figure 45: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 2µm and different doping concentrations on P substrates

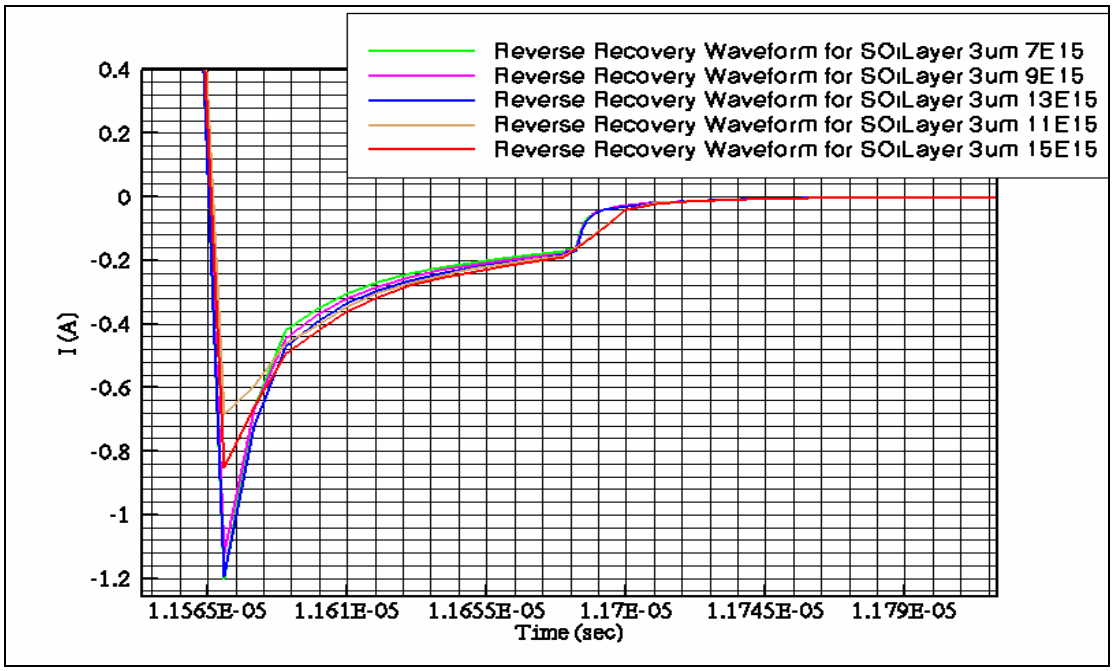

Figure 46: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 3µm and different doping concentrations on P substrates

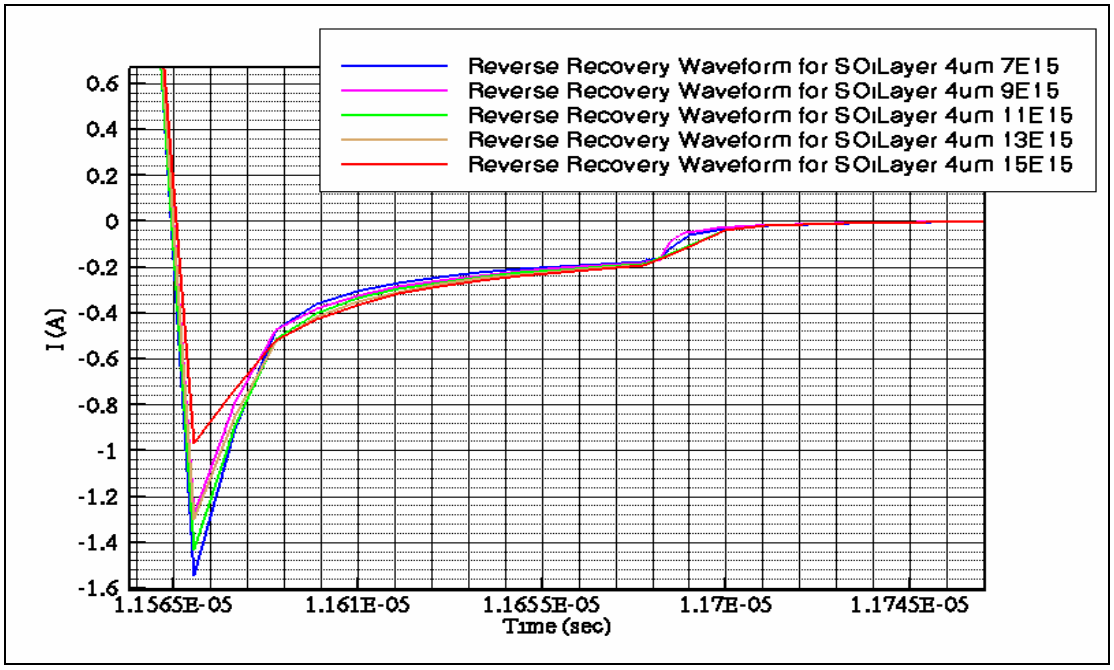

Figure 47: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 4µm and different doping concentrations on P substrates

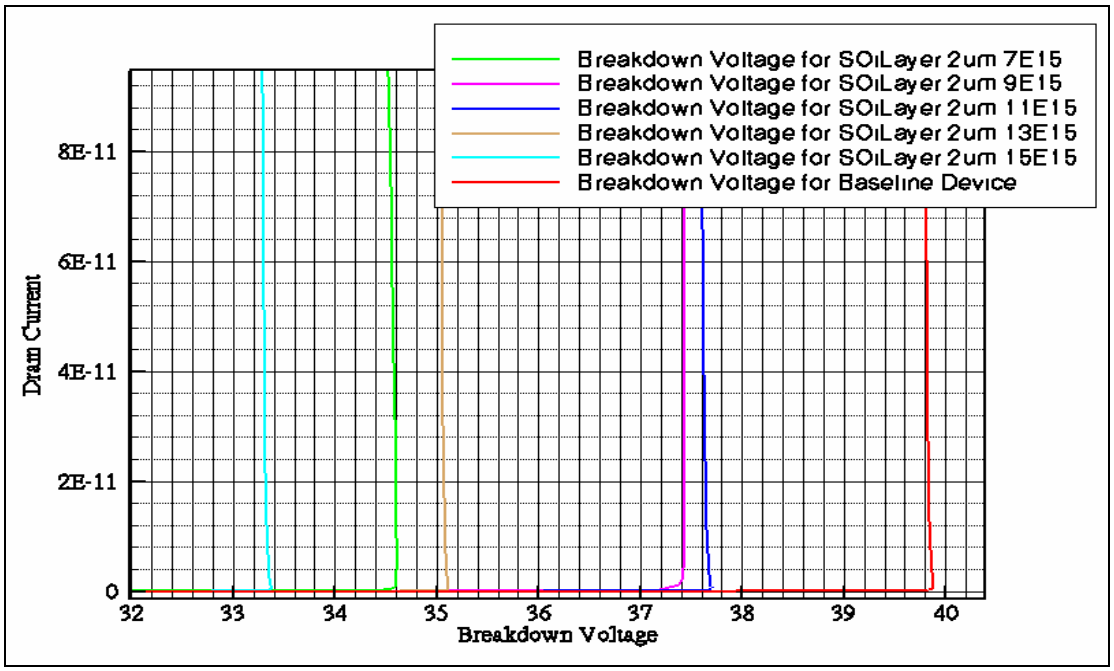

Figure 48: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 2µm and different doping concentrations on P substrates

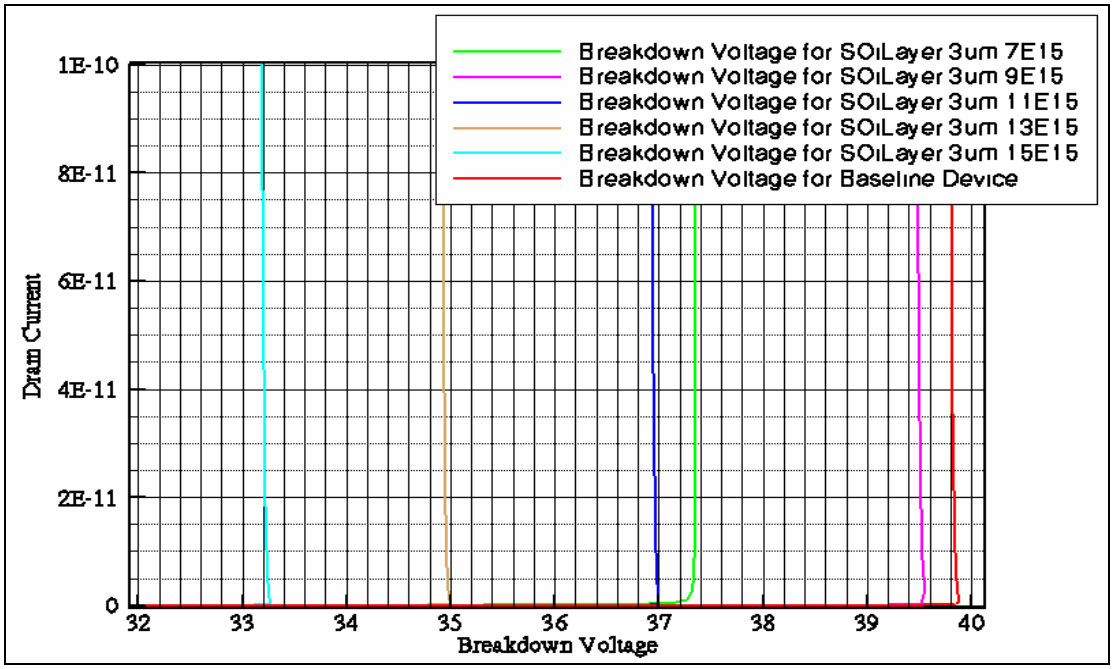

Figure 49: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 3µm and different doping concentrations on P substrates

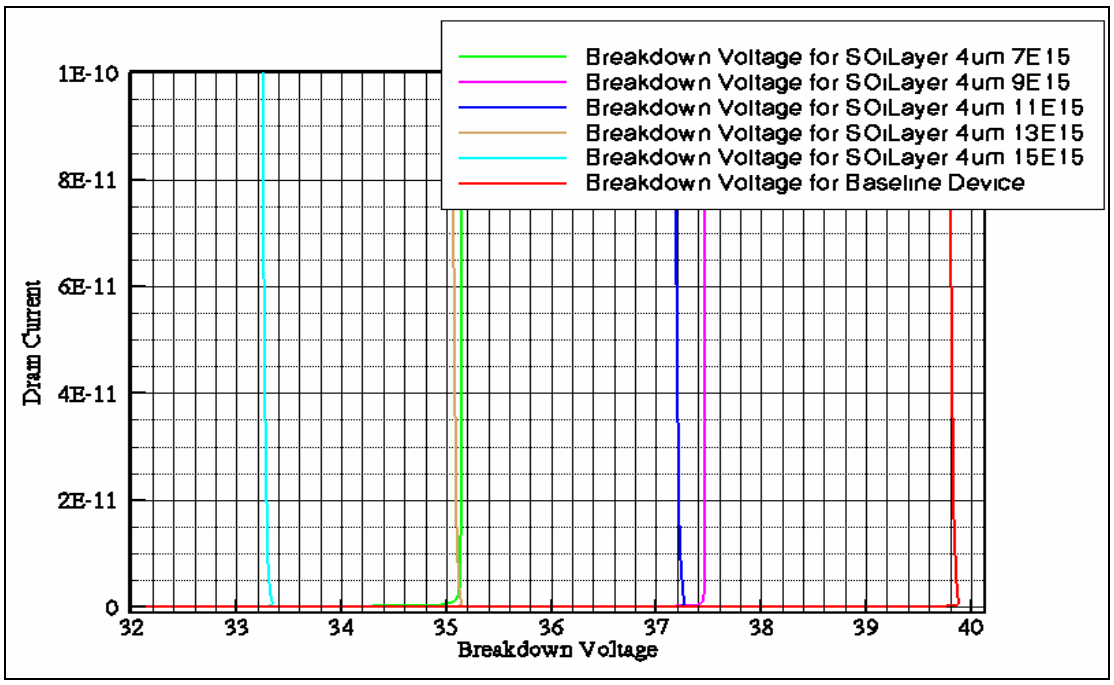

Figure 50: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 4µm and different doping concentrations on P substrates

D LDMOS Transistor with P+ Substrate, SOI layer, and P Epi Layer

This solution is the same as the previous one, but this device has a P+ substrate instead of the P substrate. The results from this solution are very similar to the previous solution. As the epitaxial layer thickness decreased in size from 4μm to 2μm the breakdown voltages started to increase and then decreased. This solution seems to have a "sweet spot" for the epi layer thickness if breakdown voltage is only considered. Another difference that should be pointed out is in the first solution and second is the breakdown voltages were spread out across a larger range than this solution provides. Also all of the variations provide at least the 30V minimum requirement. The best performing device as far as the one with the highest breakdown voltage goes is the one with an epi layer that has a doping concentration of 9E15 cm^{-3} and a thickness of 3μm. See Figure 51 for a comparison of all of the doping concentration variations with the epi thickness assigned. Figure 64 thru Figure 66 also show the breakdown voltages for each device in this category of solution. Figure 52 shows the electric field potential when breakdown occurs. As the electric field goes up the region becomes "hotter".

This combination showed the same results for decreasing the reverse recovery characteristics as all of the other solutions. As the epi layer thickness became smaller the reverse recovery characteristics also became smaller. The best performing device as far as reverse recovery charge (Qrr) is concerned is the device with an epi layer that has a doping concentration of 7E15 cm^{-3} and a thickness of 2μm. This device compared to the baseline device showed a 77.5% improvement in reverse recovery charge. This percentage was a little less than the first two solutions but is still above the goal of 75% reduction in reverse recovery characteristics. Figure 53 thru Figure 55 show different

comparisons between Qrr and doping concentrations, Trr and doping concentrations, and Irr and doping concentrations. Figure 56 thru Figure 60 shows the reverse recovery waveforms decreasing in size as the epitaxial layer decreases in size. These figures also compare the reverse recovery waveform of the baseline device with that of the solutions with different epi thicknesses. A dramatic improvement in the reverse recovery characteristics can be seen. Figure 61 thru Figure 63 show the reverse recovery waveforms for each epi layer thickness but with varied doping concentrations. The doping concentration in this solution doesn't play a large role in reducing the reverse recovery characteristics.

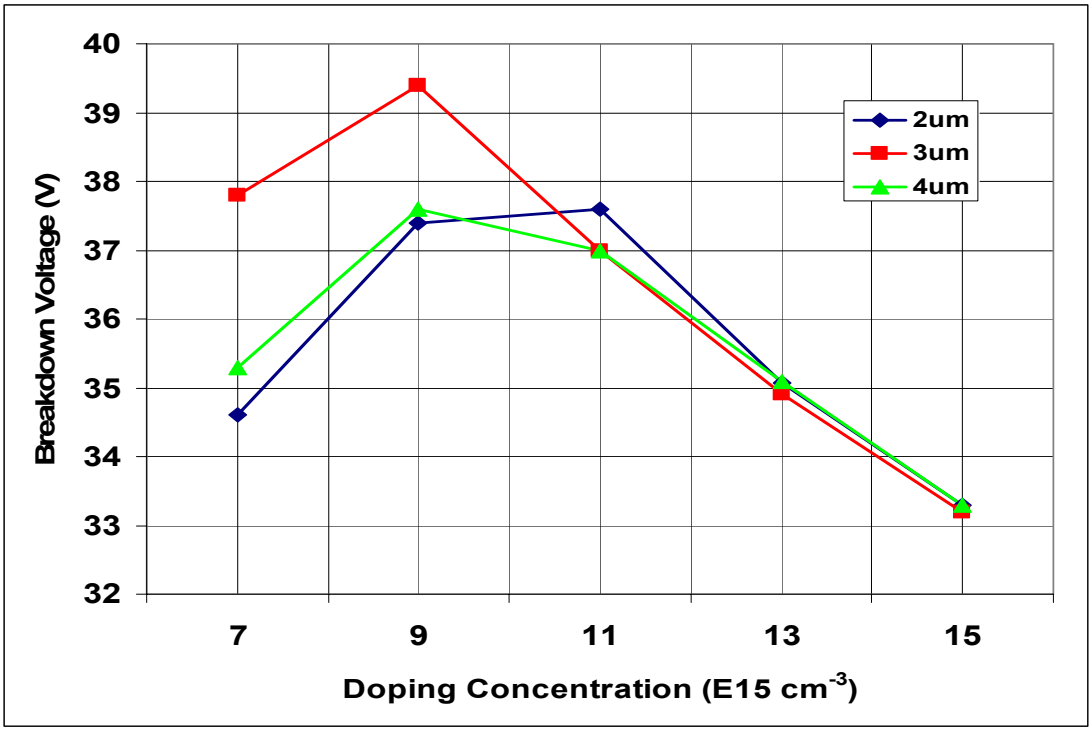

Figure 51: Breakdown Voltage vs. Doping for Device with SOI layer with P epi on P+ Substrate

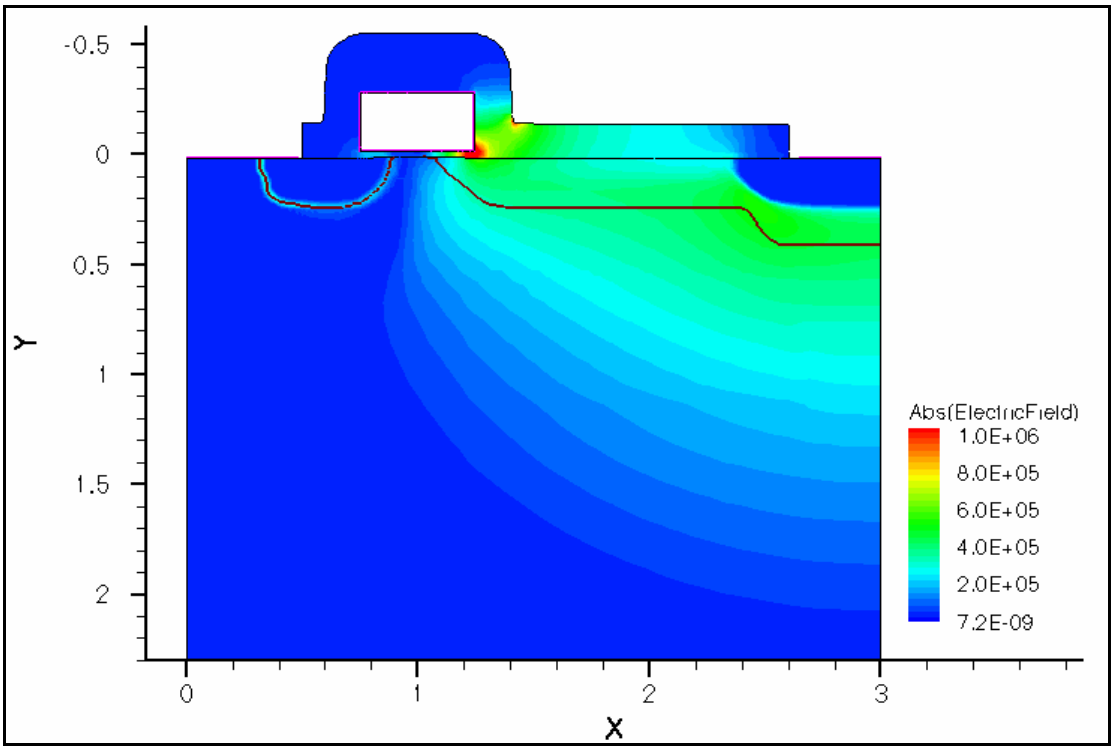

Figure 52: Electric Field Potential where breakdown occurs

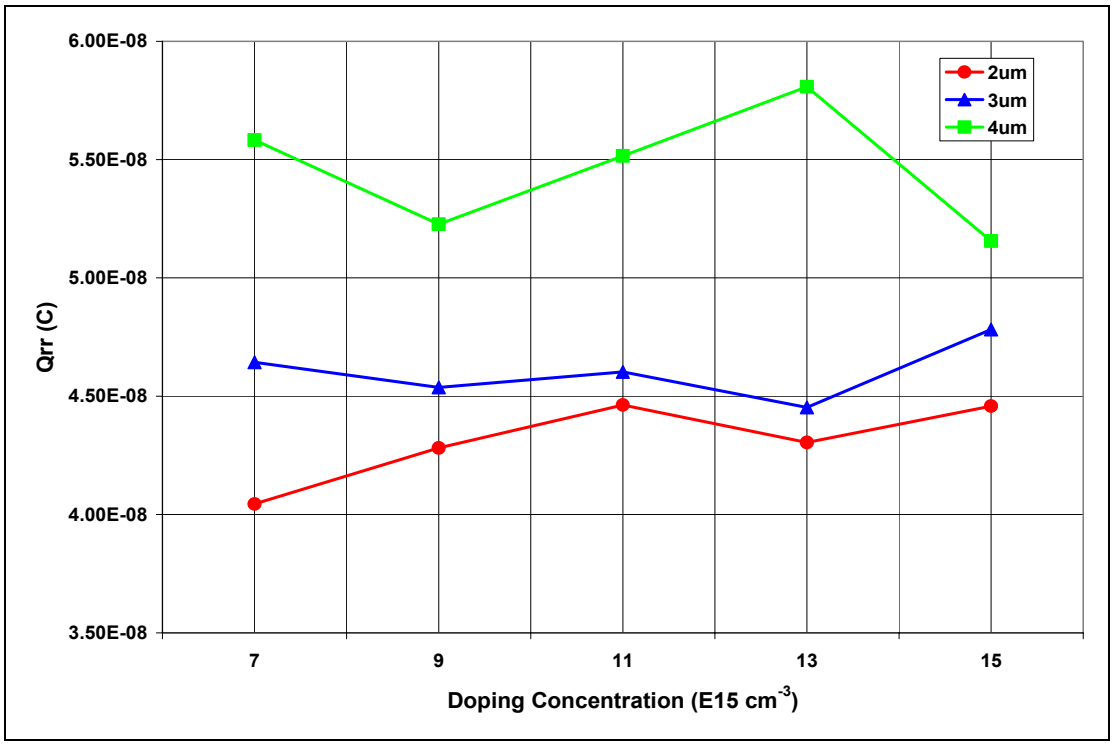

Figure 53: Qrr vs. Doping Concentration for SOI layer Device with P epi on P+ substrate

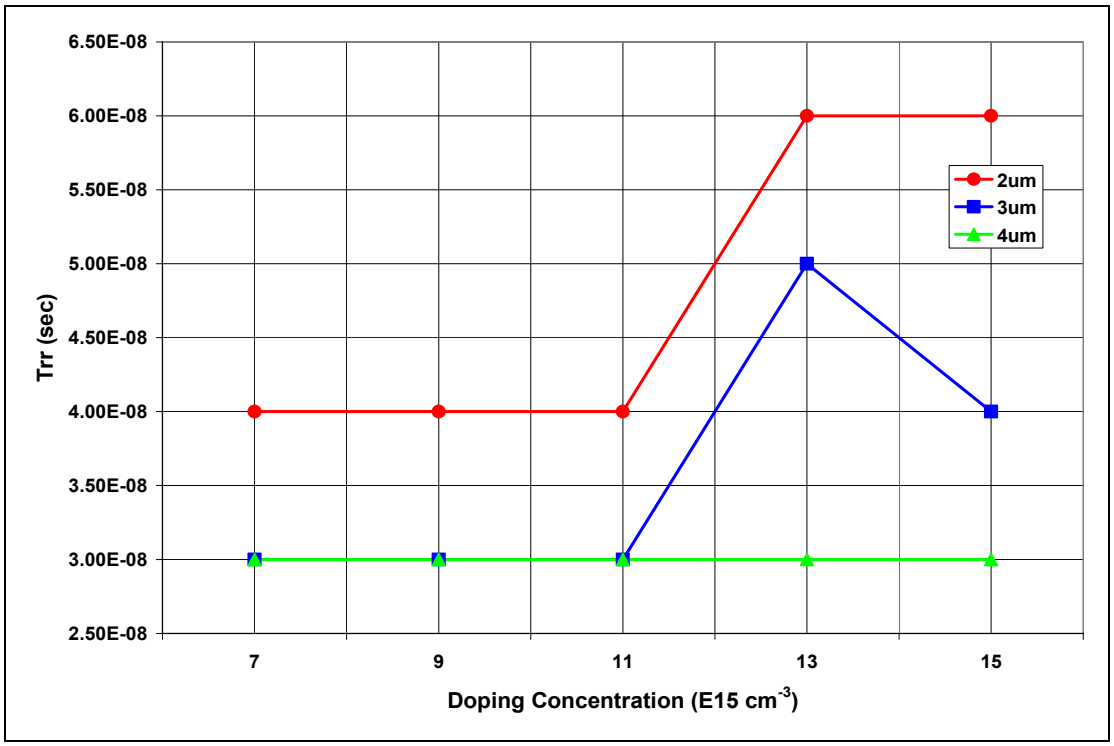

Figure 54: Trr vs. Doping Concentration for SOI layer Device with P epi on P+ substrate

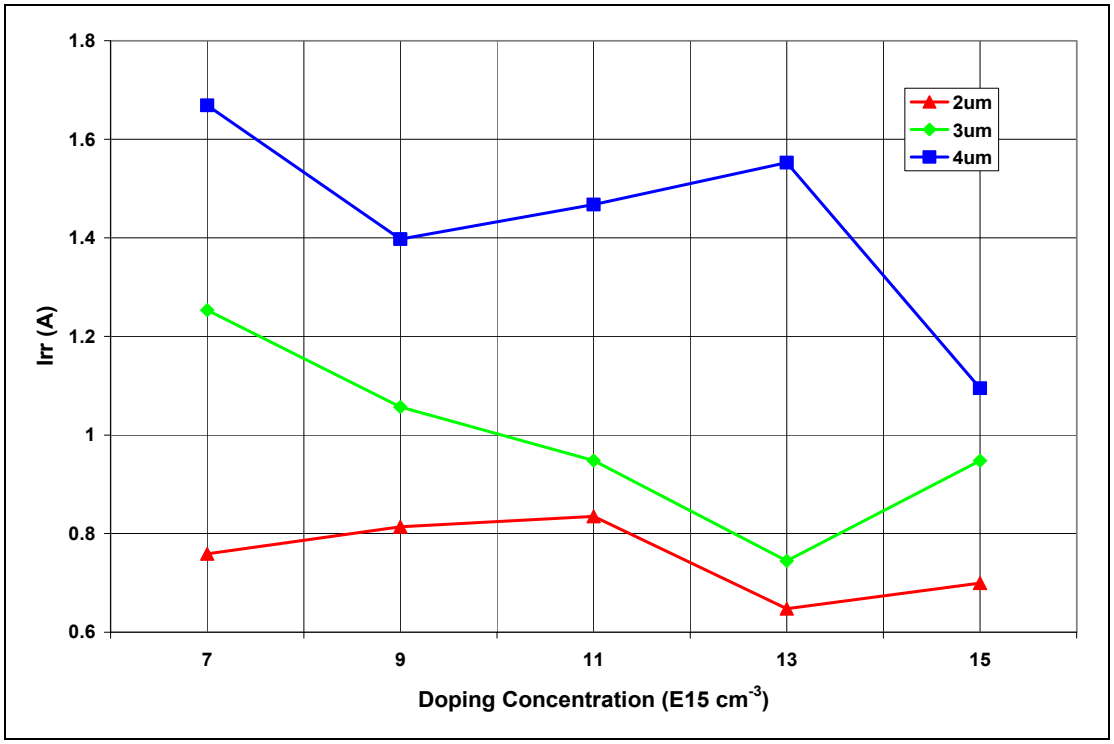

Figure 55: Irr vs. Doping Concentration for SOI layer Device with P epi on P+ substrate

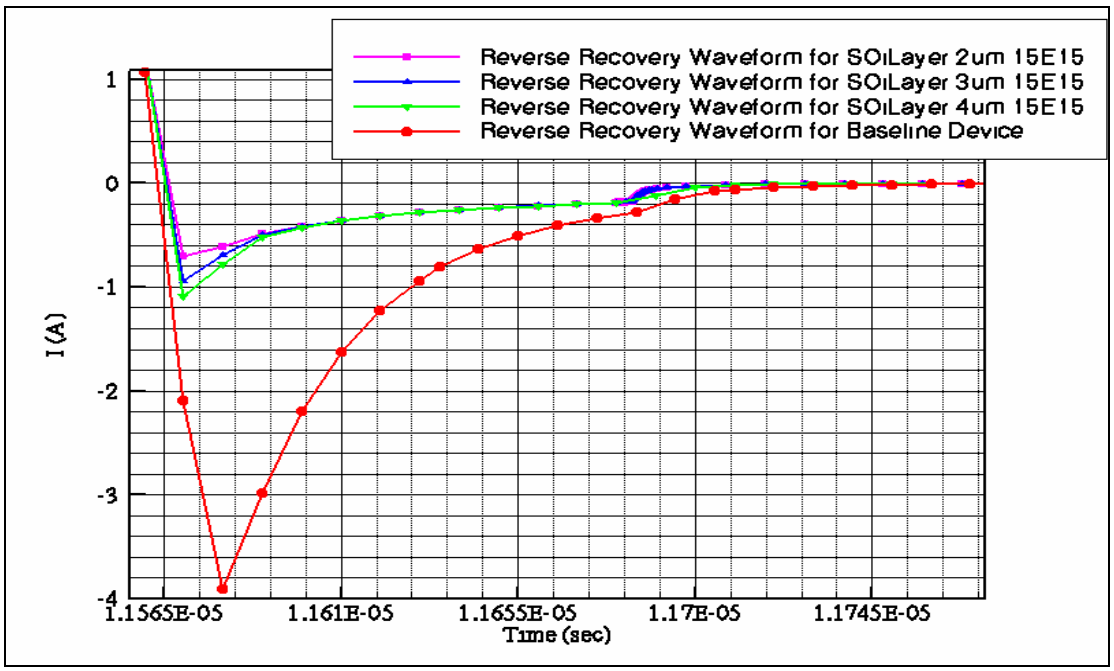

Figure 56: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 15E15 cm^{-3} of different thickness on P+ substrates

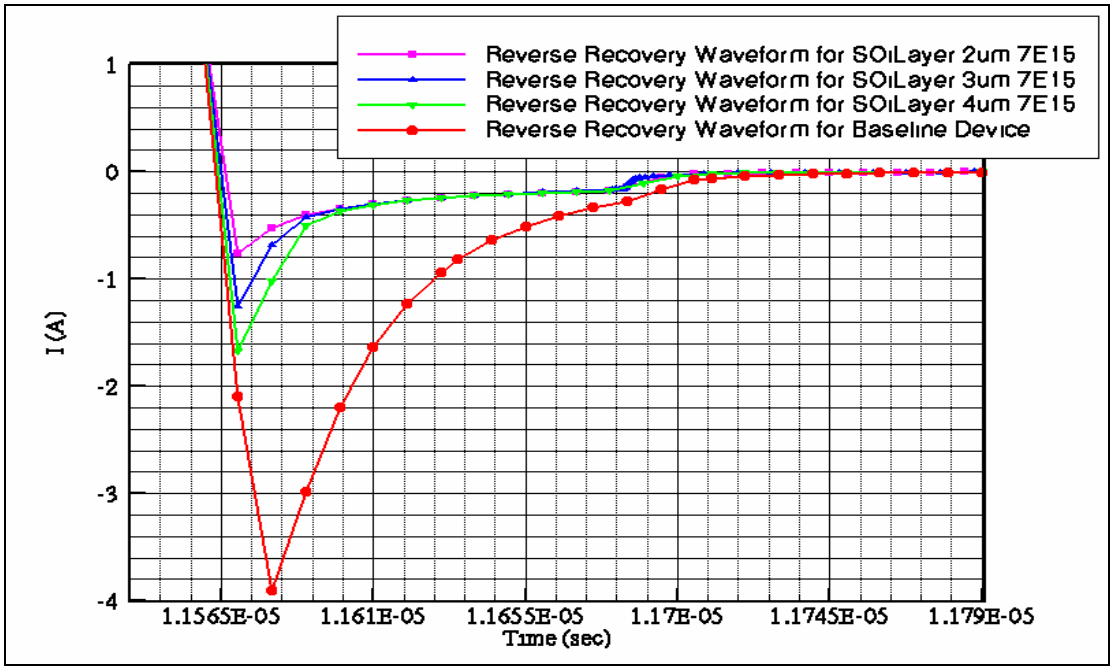

Figure 57: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 7E15 cm^{-3} of different thickness on P+ substrates

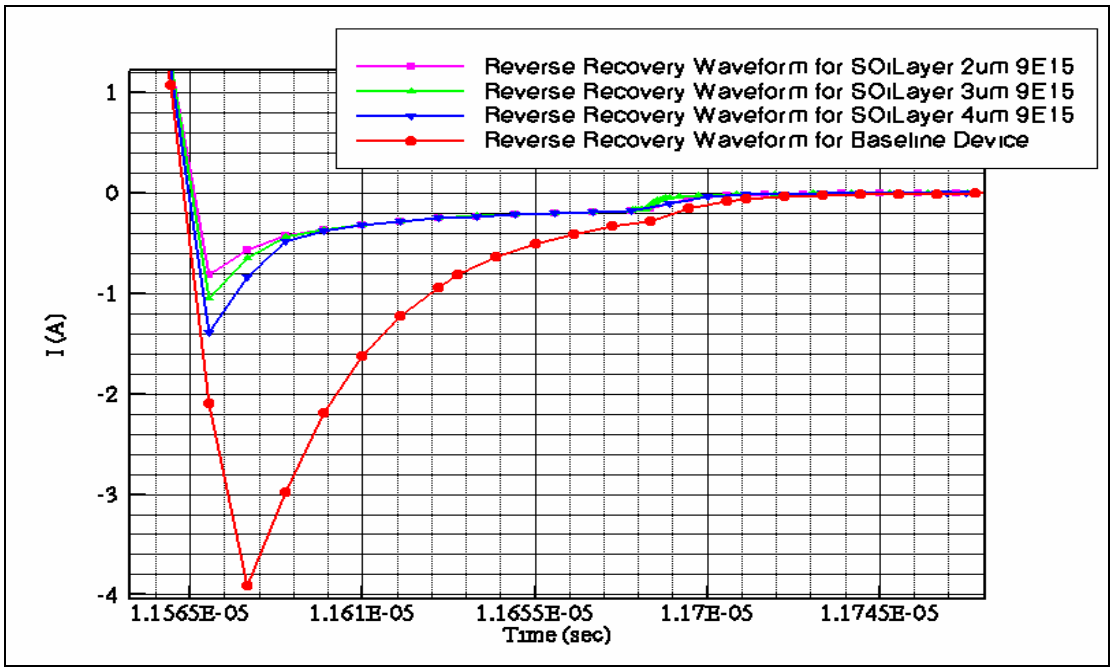

Figure 58: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 9E15 cm^{-3} of different thickness on P+ substrates

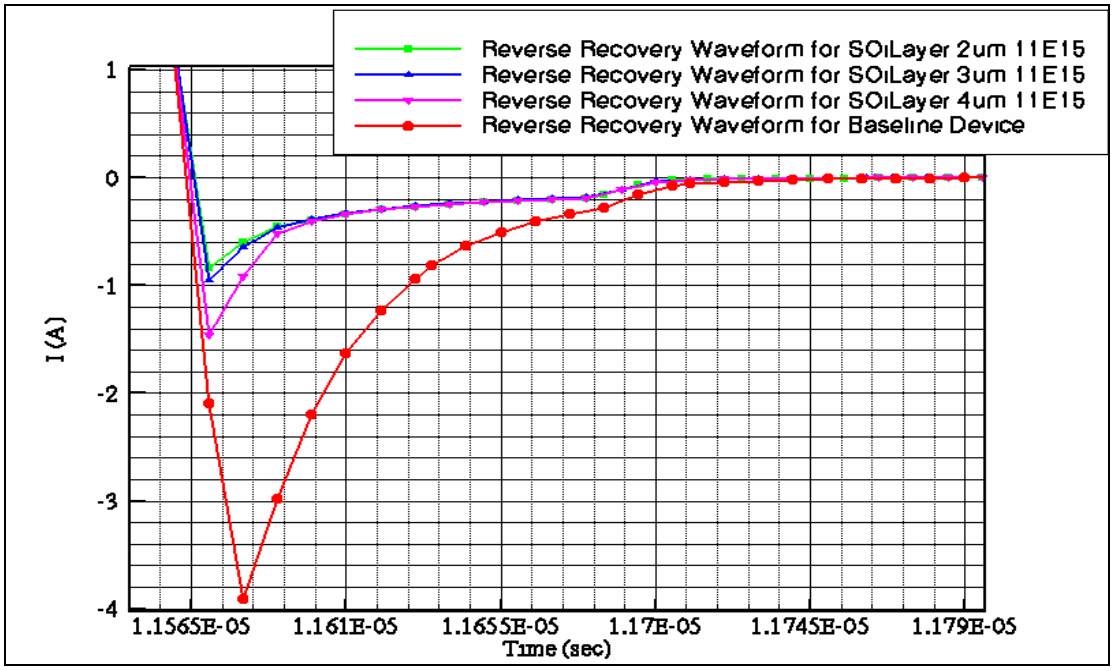

Figure 59: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 11E15 cm^{-3} of different thickness on P+ substrates

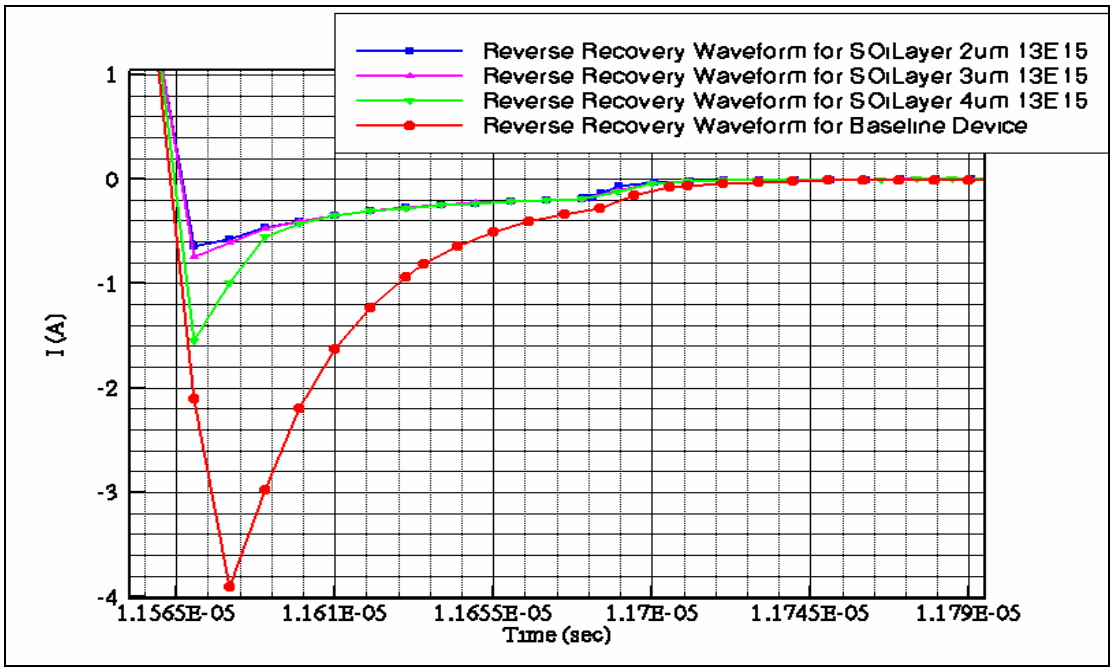

Figure 60: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a doping concentration of 13E15 cm^{-3} of different thickness on P+ substrates

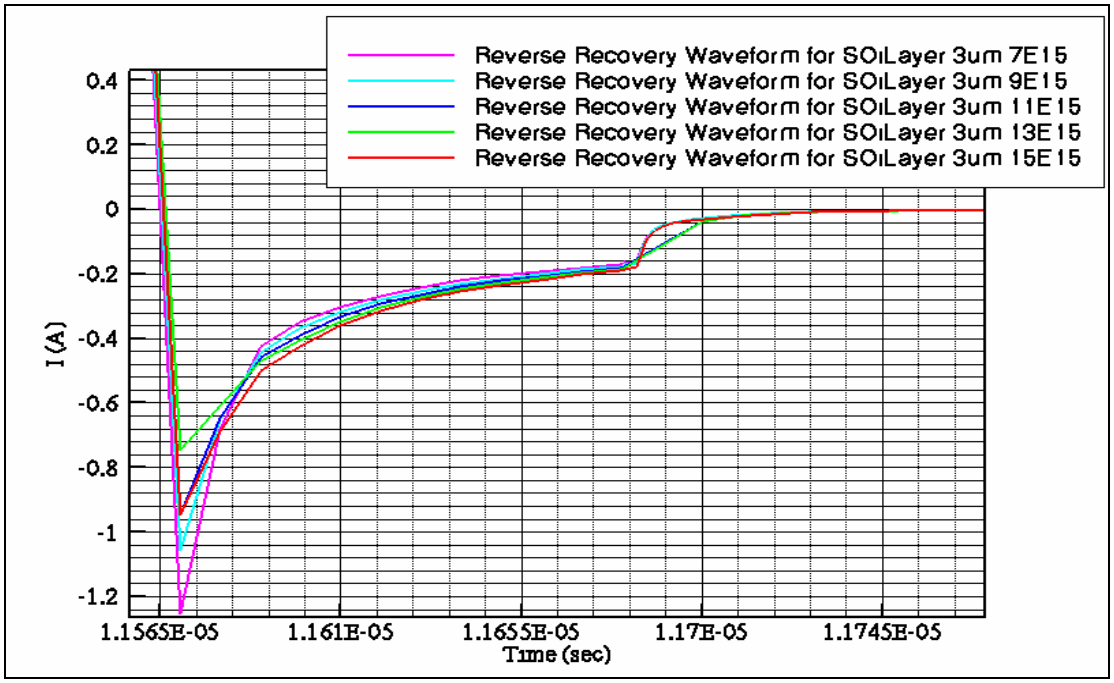

Figure 61: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 3µm and different doping concentrations on P+ substrates

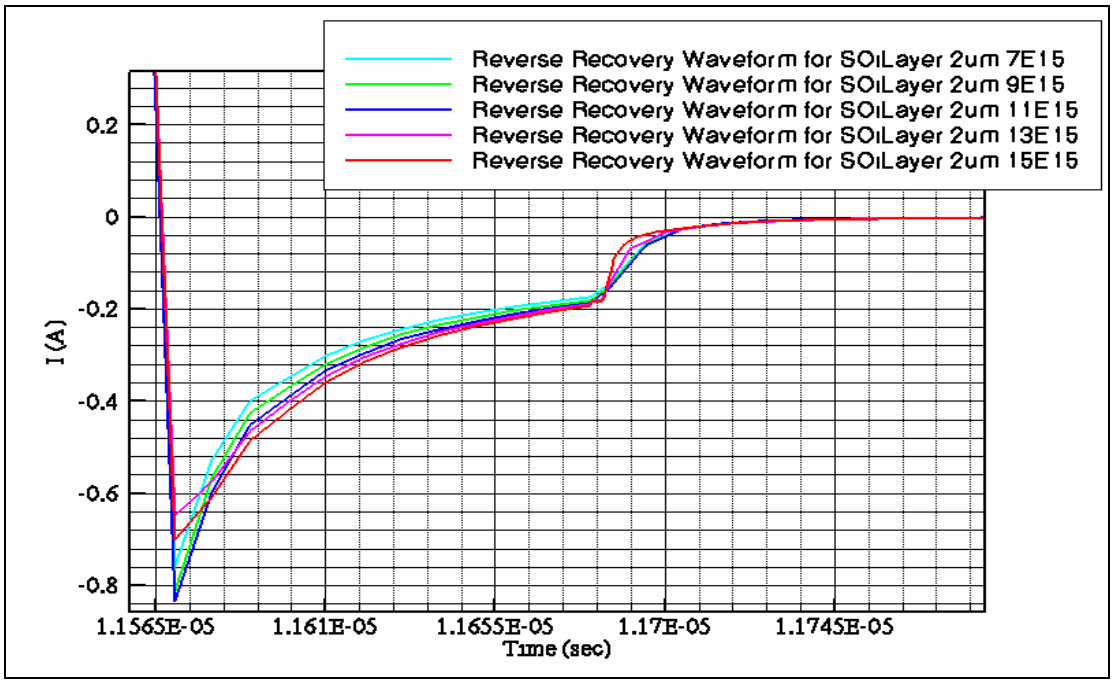

Figure 62: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 2µm and different doping concentrations on P+ substrates

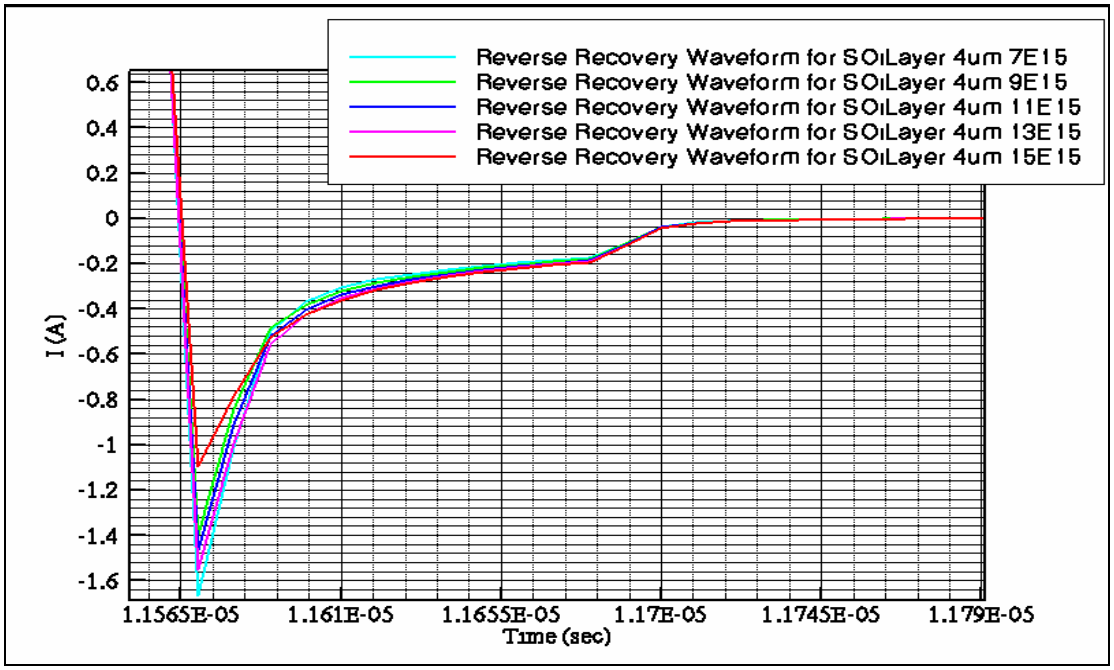

Figure 63: Reverse Recovery waveforms for devices with a SOI layer and P epi layers with a thickness of 4µm and different doping concentrations on P+ substrates

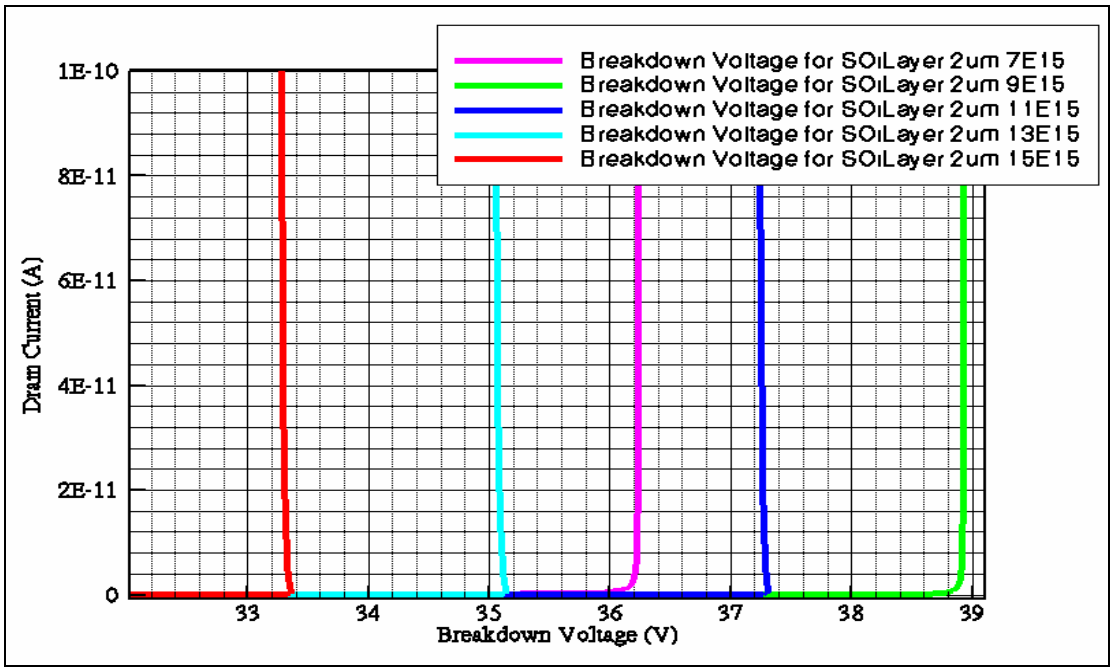

Figure 64: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 2µm and different doping concentrations on P substrates

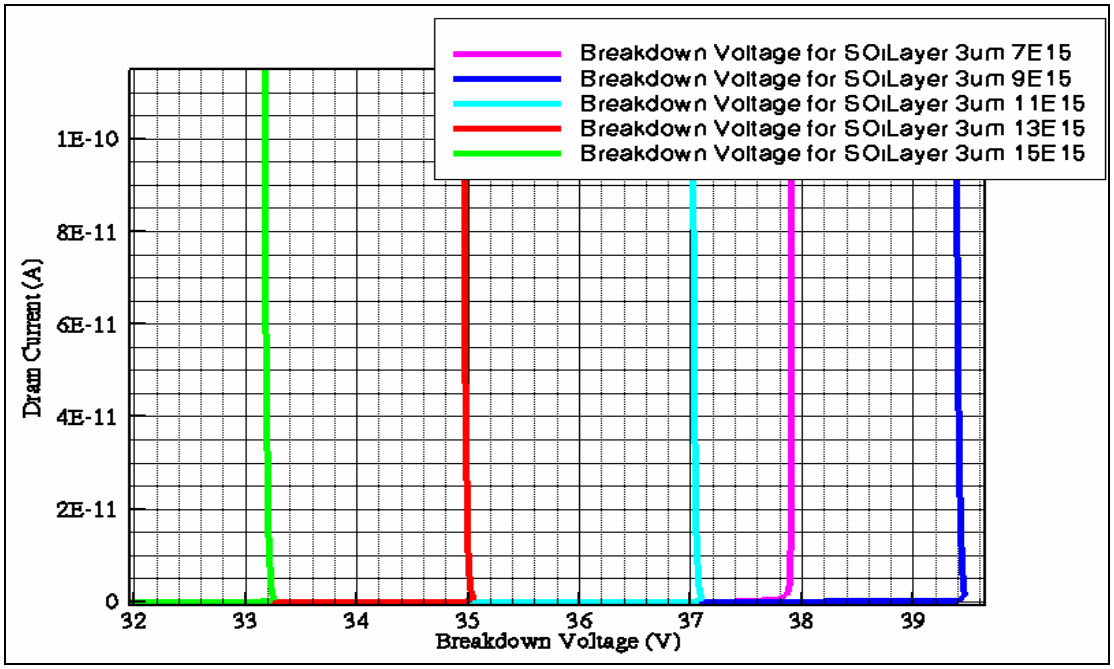

Figure 65: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 3µm and different doping concentrations on P substrates

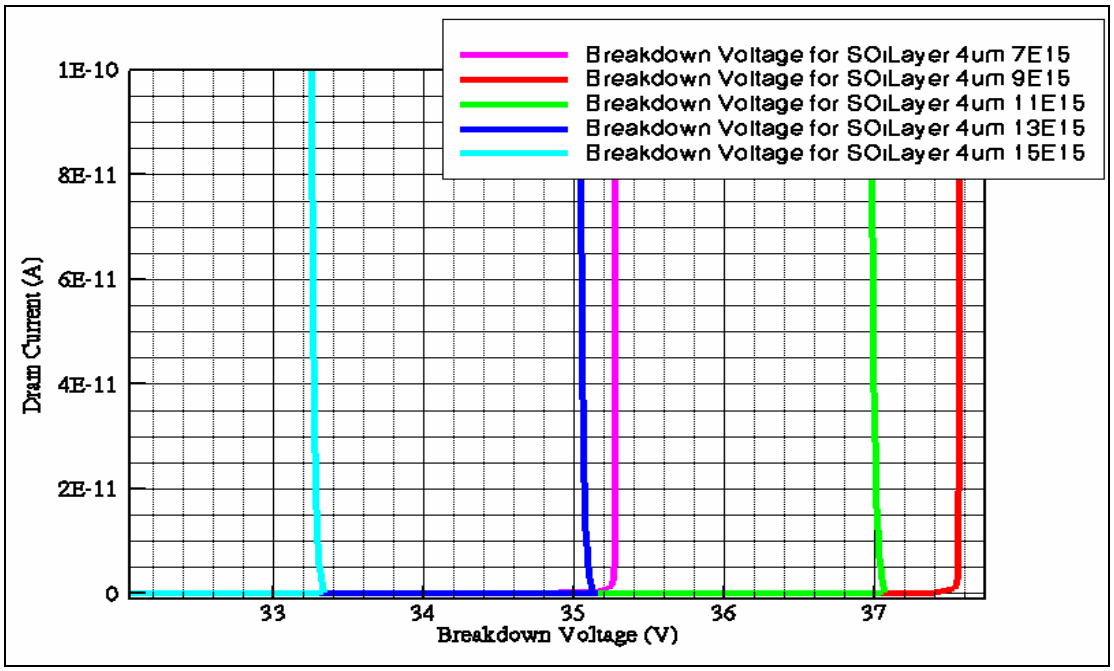

Figure 66: Breakdown Voltages for devices with a SOI layer and P epi layers with a thickness of 4µm and different doping concentrations on P substrates

E Physical Mechanisms for Improved Q_{rr} in Our Solutions

All of the solutions presented in this research study have shown significant reduction in the reverse recovery charge compared to the baseline device. All of the solutions reduce the reverse recovery charge by reducing the total amount of charge that can be stored. This is done by employing a "barrier" by different means described in each solution. Figure 68 shows a cross-sectional area of the baseline device and of one of the solutions, the P epi layer on a P+ substrate device. It is obvious that the total amount of electrons is less in the solution, thus the total storage charge is also reduced. Figure 67 shows the same thing, but as a quantitative representation. As you go further down into the device from the top the electron concentrations starts to decrease.

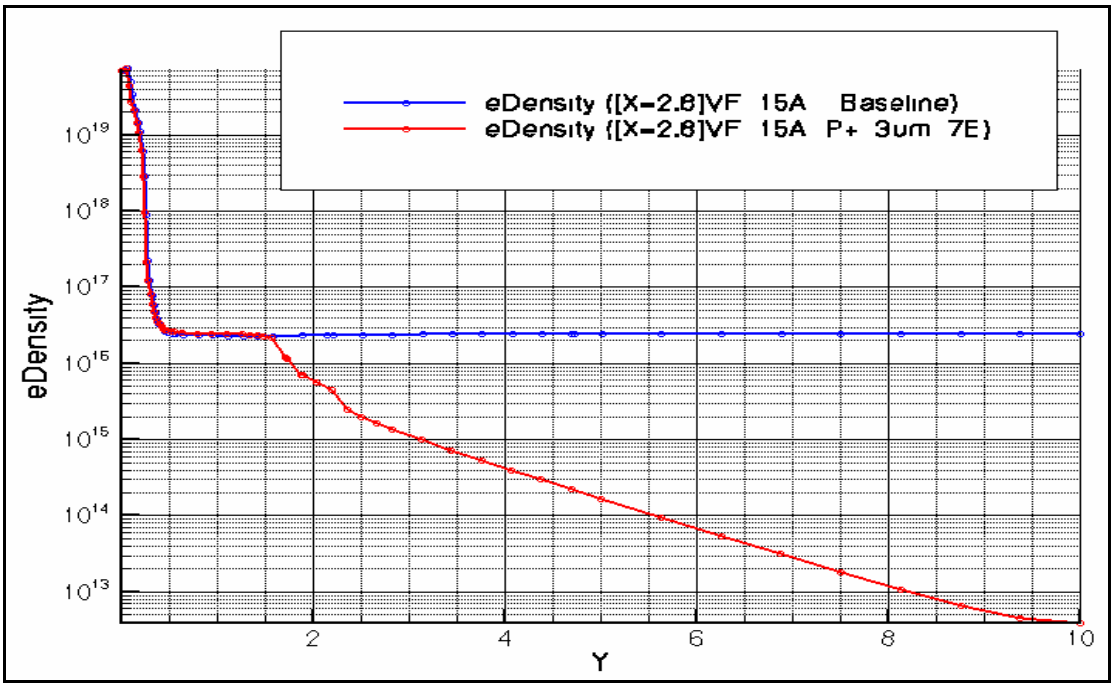

Figure 67: Logarithmic graph of electron density in the baseline device and one of the solutions

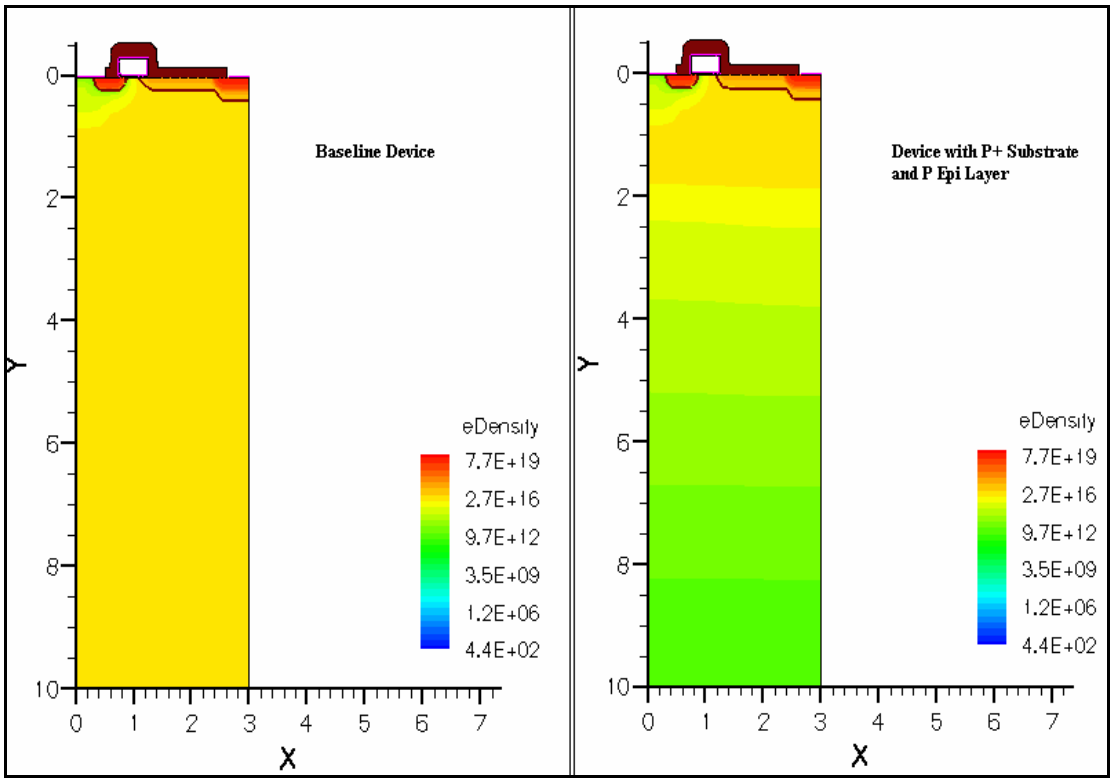

Figure 68: Cross-sectional areas of electron density in the baseline device and one of the solutions

VI CONCLUSIONS

Four solutions to the poor reverse recovery characteristics of a LDMOS synchronous MOSFET have been presented. These solutions have been verified through extensive ISE-TCAD device and circuit simulation. All four solutions met the following requirements. The solutions will reduce the body diode reverse recovery characteristics of original LDMOS transistor without employing an additional Schottky diode, increasing the Figure of Merit, or decreasing the breakdown voltage past 30 volts. They will also achieve a 75% reduction in reverse recovery charge (Qrr).This investigation has lead to the following conclusions and recommendations:

- The reduction of the reverse recovery characteristics of a LDMOS transistor can be accomplished by either employing a SOI layer as a depletion layer barrier or a heavily doped substrate next to a lightly doped substrate as a depletion layer barrier.
- Employing either one of these techniques will reduce the body diode power losses by at least 77% or better.
- Doping concentration of an epi layer doesn't play that much of a role in reducing the reverse recovery characteristics, but further investigation is warranted into whether it affects other important characteristics of the LDMOS transistor.
- Further physical experimentation should be done to verify the simulated results.

APPENDIX: ISE CODE

Here is an example of the DESSIS code that tests for different electrical characteristics. The first sample of code tests for the breakdown voltage of the device. The next sample of code tests the reverse recovery time of the device.

```
BVdss_des.cmd
File{
 * Input Files
  Grid      = "mesh_mdr.grd"
  Doping    = "mesh_mdr.dat"

 * Output Files
  Plot      = "BV_des.dat"
  Current   = "BV_des.plt"
  Output    = "BV_log"
}

Electrode{

  { Name="Gate"    Voltage=0.0 }
  { Name="Source"  Voltage=0.0 }
  { Name="Drain"   Voltage=0.0 Resistance=1.0e12}
}

Physics{
  * DriftDiffusion
  EffectiveIntrinsicDensity( OldSlotboom )
  Mobility(
    DopingDep
  )
  Recombination(
    SRH( DopingDep )
    Avalanche( GradQuasiFermi )
   )
}

Plot{
*--Density and Currents, etc
  eDensity hDensity
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi

*--Temperature
```

```
  eTemperature Temperature * hTemperature

*--Fields and charges
  ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
  Doping DonorConcentration AcceptorConcentration

*--Generation/Recombination
  SRH Band2Band * Auger
  AvalancheGeneration eAvalancheGeneration hAvalancheGeneration

*--Driving forces
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
  BandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eQuantumPotential
}

Math {
  Extrapolate
  Avalderivatives
  Iterations=20
  Notdamped =100
  RelErrControl
  ErRef(Electron)=1.e10
  ErRef(Hole)=1.e10
  BreakCriteria{ Current(Contact="Drain" AbsVal=1e-10) }
  CNormPrint
}

Solve {
  *- Build-up of initial solution:
  Coupled(Iterations=100){ Poisson }
  Coupled{ Poisson Electron Hole }

  Quasistationary(
    InitialStep=1.0e-10 Increment=1.35
    MinStep=1.0e-16 MaxStep=0.01
    Goal{ Name="Drain" Voltage=1.0e8 }
  ){ Coupled{ Poisson Electron Hole } }
```

```
}


Rev_Rec_des.cmd
Device DIODE {
  File{
 * Input Files
   Grid      = "Mesh_mdr.grd"
   Doping    = "Mesh_mdr.dat"

 * Output Files
   Plot      = "Rev_Rec_des.dat"
   Current   = "Rev_Rec_des.plt"
  }

  Electrode{
   { Name="Source"    Voltage=0.0 }
   { Name="Drain"     Voltage=0.0 }
   { Name="Gate"      Voltage=0.0 }
  }

  Physics{
    AreaFactor=10.0e6

    Mobility(
      DopingDep
     )

    Recombination(
      SRH( DopingDep)
      Auger
    )

    EffectiveIntrinsicDensity (OldSlotboom)
  }
}


File {
    Output = "Rev_Rec_des"
    SPICEPath = "."
}


Plot{
*--Density and Currents, etc
```

```
  eDensity hDensity
  TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi

*--Temperature
  Temperature
   hTemperature

*--Fields and charges
  ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
  Doping DonorConcentration AcceptorConcentration

*-Generation/Recombination
 SRHRecombination Band2Band AugerRecombination
 AvalancheGeneration eAvalancheGeneration hAvalancheGeneration
 TotalRecombination
 eLifeTime hLifeTime


*--Driving forces
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal

*--Band structure/Composition
  BandGap
  BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eQuantumPotential
}

Math {
  Extrapolate
  Avalderivatives
  Iterations=20
  Notdamped =100
  RelErrControl
  ErRef(Electron)=1.e10
  ErRef(Hole)=1.e10
  CNormPrint
  Transient=BE
}
```

```
System {
  Vsource_pset vcc (4 0) { dc=0}

  Vsource_pset vin (1 0) {
    pulse = (0.0       # dc
             5.0       # amplitude
             3e-7      # td
             3e-7      # tr
             3e-7      # tf
             5e-6      # ton
             11e-6)    # period
  }

  DIODE d1 ( "Source"=3 "Drain"=4 "Gate"=3 )
  MOSFET_pset sw1 (3 2 0 0) {
    l = 3e-6
    w = 3
    ad = 1e-5
    as = 1e-5
    pd = 6
    ps = 6
  }

  Resistor_pset rg (1 2) { resistance = 20 }
  Inductor_pset l  (3 4) { inductance = 5e-6}

  Plot "Rev_Rec_waveform.plt" (
    time ()
    v(1)
    v(2)
    v(3)
    v(4)
    i(d1,4)
    i(l,3)
    i(sw1,3)
  )
}

Solve {

# ini
   NewCurrentFile="init"
   Coupled(Iterations=100){ Poisson }
   Coupled{ Poisson Electron }
   Coupled{ Poisson Electron Hole}
```

```
  Coupled{ Poisson Electron Hole Contact Circuit}

# ramp Vcc
  Quasistationary
   (  InitialStep=1e-3 Increment=1.35
      Maxstep=0.05 MinStep=1e-5
      Goal { Parameter=vcc.dc voltage=10 }
   ){ Coupled { Poisson Electron Hole Contact Circuit} }

# switch
  NewCurrentFile=""
  Transient (
   InitialTime=0 FinalTime=16e-6
   InitialStep=5e-9 Increment=2
   MaxStep=1e-8 MinStep=1e-13
  ){ Coupled { Poisson Electron Hole Contact Circuit} }
```

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