DESIGN OF LOW-CAPACITANCE AND HIGH-SPEED ELECTROSTATIC DISCHARGE (ESD) DEVICES FOR LOW-VOLTAGE PROTECTION APPLICATIONS

by

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ABSTRACT

Electrostatic discharge (ESD) is defined as the transfer of charge between bodies at different potentials. The electrostatic discharge induced integrated circuit damages occur throughout the whole life of a product from the manufacturing, testing, shipping, handing, to end user operating stages. This is particularly true as microelectronics technology continues shrink to nano-metric dimensions. The ESD related failures is a major IC reliability concern and results in a loss of millions dollars to the semiconductor industry each year. Several ESD stress models and test methods have been developed to reproduce the real world ESD discharge events and quantify the sensitivity of ESD protection structures. The basic ESD models are: Human body model (HBM), Machine model (MM), and Charged device model (CDM). To avoid or reduce the IC failure due to ESD, the on-chip ESD protection structures and schemes have been implemented to discharge ESD current and clamp overstress voltage under different ESD stress events.

Because of its simple structure and good performance, the junction diode is widely used in on-chip ESD protection applications. This is particularly true for ESD protection of low-voltage ICs where a relatively low trigger voltage for the ESD protection device is required. However, when the diode operates under the ESD stress, its current density and temperature are far beyond the normal conditions and the device is in danger of being damaged. For the design of effective ESD protection solution, the ESD robustness and low parasitic capacitance are two major concerns. The ESD robustness is usually defined after the failure current It2 and on-state resistance Ron. The transmission line pulsing (TLP) measurement is a very effective tool for evaluating the ESD robustness of a circuit or single element. This is particularly helpful in

characterizing the effect of HBM stress where the ESD-induced damages are more likely due to thermal failures.

Two types of diodes with different anode/cathode isolation technologies will be investigated for their ESD performance: one with a LOCOS (Local Oxidation of Silicon) oxide isolation called the LOCOS-bound diode, the other with a polysilicon gate isolation called the polysilicon-bound diode. We first examine the ESD performance of the LOCOS-bound diode. The effects of different diode geometries, metal connection patterns, dimensions and junction configurations on the ESD robustness and parasitic capacitance are investigated experimentally. The devices considered are N+/P-well junction LOCOS-bound diodes having different device widths, lengths and finger numbers, but the approach applies generally to the P+/N-well junction diode as well. The results provide useful insights into optimizing the diode for robust HBM ESD protection applications.

Then, the current carrying and voltage clamping capabilities of LOCOS- and polysilicon-bound diodes are compared and investigated based on both TCAD simulation and experimental results. Comparison of these capabilities leads to the conclusion that the polysilicon-bound diode is more suited for ESD protection applications due to its higher performance. The effects of polysilicon-bound diode's design parameters, including the device width, anode/cathode length, finger number, poly-gate length, terminal connection and metal topology, on the ESD robustness are studied. Two figures of merits, FOM_It2 and FOM_Ron, are developed to better assess the effects of different parameters on polysilicon-bound diode's overall ESD performance.

As latest generation package styles such as mBGAs, SOTs, SC70s, and CSPs are going to the millimeter-range dimensions, they are often effectively too small for people to handle with fingers. The recent industry data indicates the charged device model (CDM) ESD event becomes

increasingly important in today's manufacturing environment and packaging technology. This event generates highly destructive pulses with a very short rise time and very small duration. TLP has been modified to probe CDM ESD protection effectiveness. The pulse width was reduced to the range of 1-10 ns to mimic the very fast transient of the CDM pulses. Such a very fast TLP (VFTLP) testing has been used frequently for CDM ESD characterization.

The overshoot voltage and turn-on time are two key considerations for designing the CDM ESD protection devices. A relatively high overshoot voltage can cause failure of the protection devices as well as the protected devices, and a relatively long turn-on time may not switch on the protection device fast enough to effectively protect the core circuit against the CDM stress. The overshoot voltage and turn-on time of an ESD protection device can be observed and extracted from the voltage versus time waveforms measured from the VFTLP testing. Transient behaviors of polysilicon-bound diodes subject to pulses generated by the VFTLP tester are characterized for fast ESD events such as the charged device model. The effects of changing devices' dimension parameters on the transient behaviors and on the overshoot voltage and turn-on time are studied. The correlation between the diode failure and poly-gate configuration under the VFTLP stress is also investigated.

Silicon-controlled rectifier (SCR) is another widely used ESD device for protecting the I/O pins and power supply rails of integrated circuits. Multiple fingers are often needed to achieve optimal ESD protection performance, but the uniformity of finger triggering and current flow is always a concern for multi-finger SCR devices operating under the post-snapback region. Without a proper understanding of the finger turn-on mechanism, design and realization of robust SCRs for ESD protection applications are not possible. Two two-finger SCRs with different combinations of anode/cathode regions are considered, and their finger turn-on

uniformities are analyzed based on the I-V characteristics obtained from the transmission line pulsing (TLP) tester. The dV/dt effect of pulses with different rise times on the finger turn-on behavior of the SCRs are also investigated experimentally.

In this work, unless noted otherwise, all the measurements are conducted using the Barth 4002 transmission line pulsing (TLP) and Barth 4012 very-fast transmission line pulsing (VFTLP) testers.

To my parents Li Xianshu and Zhang Guizhen

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LIST OF ACRONYMS

ESD	Electrostatic Discharge
ICs	Integrated Circuits
CMOS	Complementary Metal-Oxide-Semiconductor
HBM	Human Body Model
MM	Machine Model
CDM	Charged Device Model
DUT	Device Under Test
ESDA	ESD Association
JEDEC	Joint Electron Device Engineering Council
IEC	International Electrotechnical Commission
TLP	Transmission Line Pulsing
VFTLP	Very-fast Transmission Line Pulsing
GGNMOS	Grounded-Gate NMOS
SCR	Silicon Controlled Rectifier
BiCMOS	Bipolar Complementary Metal-Oxide-Semiconductor
STI	Shallow Trench Isolation
LOCOS	Local Oxidation of Silicon
TCAD	Technology Computer Aided Design
FOM	Figure of Merit
MLSCR	Modified Lateral SCR
LVTSCR	Low-Voltage Triggering SCR

ACASCR	Anode-Cathode-Anode SCR
CACSCR	Cathode-Anode-Cathode SCR

CHAPTER 1. INTRODUCTION

Electrostatic discharge (ESD) is defined as the transfer of charge between bodies at different potentials. Most people have such a shock experience when touching the metal doorknob after walking across a carpeted floor or sliding the car seat. The shock is a result of discharging the accumulated charges on human body through the conductive metal doorknob. Normally, this electrostatic discharge can reach a few kilo-volts and sparks can even be seen due to the ionization of air gap between the charged human body and zero-potential surface of doorknob. The ESD is a rather general concept and occurs almost everywhere. One should never overlook the kind of damages caused by ESD. Before going through the details of ESD phenomenon, we start from the understanding of how electrostatic charge occurs.

1.1 Static electricity

The electrostatic charge, or static electricity, is defined as an electrical charge caused by an imbalance of electrons on the surface of a material. The very first documented observation of static electricity generation is back to 600 B.C. The Greeks rubbed amber with a piece of fur and observed attraction of lightweight objects to the amber. A charge can be generated on a material in several ways: triboelectric charging, induction, ion bombardment and contact with another charged object. Triboelectric charging is the most common electrostatic generation mechanism, where the static electricity is created by the contact and separation of two materials. For example, when a person walks across a carpeted floor, the static charges are accumulated on the human body as the shoe soles contact and then separate from the surface of floor. Based on the nature of materials, the electrons transfer from one material to the other during the contact and separation

procedures. The material that loses electrons becomes positively charged and the other object that gets electrons becomes negatively charged. The opposite polarities of electrostatic charges lead to different electrostatic potentials for the two materials. However, the process of material contact, electron transfer and separation is a complex mechanism. The amount of accumulated charge is affected by material types, speed of contact and separation, humidity and several other factors.

1.2 Electrostatic discharge (ESD)

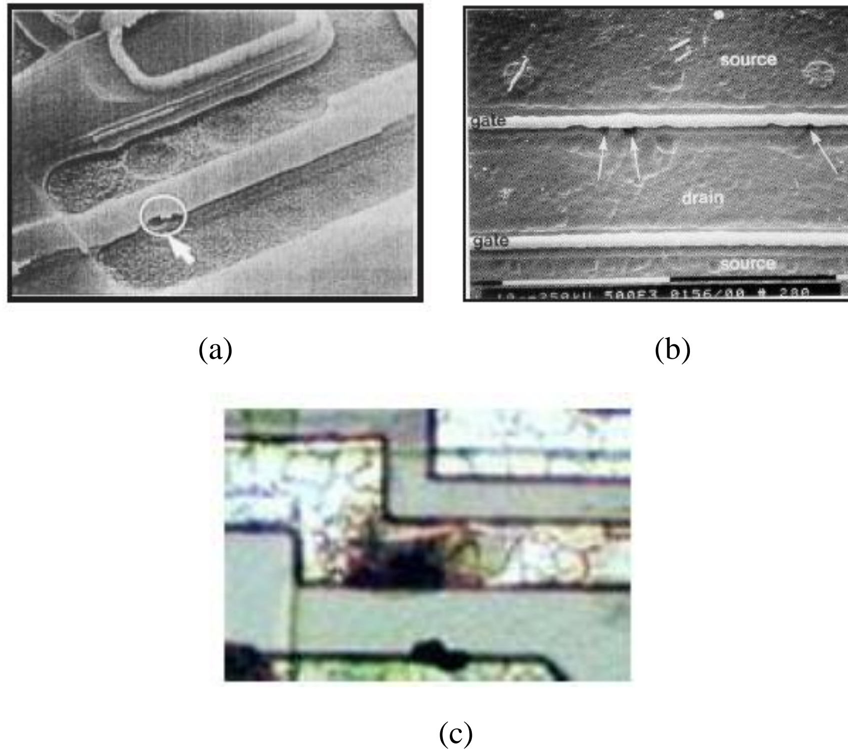
Once the charge is created on the material, it becomes an "electrostatic" charge. When two objects with different electrostatic potentials are brought into close proximity, this charge may transfers from one object to the other and creates the electrostatic discharge (ESD) event. In the semiconductor industry, the ESD events occur throughout the whole life of a product. The exposure to the undetected ESD starts in the fabrication environment during process [1] and extends through the various manufacturing stages up to the system level.

Though ESD only gives harmless shock to the human body, it is lethal to sensitive electronic components and integrated circuits (ICs). In a typical working environment, a human with body capacitance of 150 pF can accumulate the amount of charge up to 0.6 μC, which leads to an electrostatic potential of over 4000 V. Any contact between the charged human body and grounded object such as a pin of ICs will results a discharge for about 100 ns with several amperes peak discharge current. The energy associated with the electrostatic discharge is released into an object with small volume, such as a device in the integrated circuit and generates the "self-heating". The heat gives rise to a sudden temperature increase inside the body of semiconductor device. If the heat cannot be dissipated quickly enough, the device will be

damaged as the temperature arrive the melting point of either the silicon or metal. On the other hand, the high discharging current could also lead to voltage drop that may be high enough to cause the breakdown of gate oxide in thin gate MOS processes.

The ESD induced integrated circuit failures occur in any environment from manufacturing, testing, handling to customer operating. The damage caused by an ESD event can be latent defect, which is also named as soft failure. In the case of soft failure, the performance of device or circuit is partially degraded after exposed to the ESD pulse, such as an increased leakage current or decreased reverse breakdown voltage. The soft failure usually occurs when an ESD pulse is not strong sufficiently to destroy the device and is more difficult to identify due to the basic functionalities of device or circuit still operative. The other type of damage to the electronic devices is catastrophic, or named hard failure. In the case of hard failure, the device is permanently destroyed during the ESD event and cannot function any more. The ESD induced hard failure can be associated with different mechanisms, such as the dielectric rupture, junction burnout and metal melting [2]-[4]. The junction burnout and metal melting are mainly due to the thermal damages, which are caused by high current induced Joule-heating, localized over-heating and heat distribution. On the other hand, the dielectric rupture is usually caused by high electric field density under high voltage stresses, where gate oxide breakdown in CMOS transistors is the typical failure signature.

Figure 1.1(a)-(c) show the photos of gate oxide damage to an input buffer after the CDM stress, drain-junction burnout in an NMOS after HBM stress and a fused metal line respectively.



(a) (b)

(c)

Figure 1.1: Photos of three ESD failure mechanisms: (a) gate oxide breakdown, (b) junction burnout, and (c) metal melting

The ESD failure is a profound reliability problem in semiconductor industry. Statistics indicated over 30% of IC failures might be attributed to ESD, which cost millions dollars to the semiconductor industry each year [5]-[6]. Thus, the precautions to suppress ESD become important topics through all phases of an IC's life.

1.3 ESD stress models and test methods

In an IC environment, the static charges can be accumulated in different objects, such as a human body, a manufacturing machine or an integrated circuit itself. When the charged objects contact a grounded surface, the discharge waveforms are not the same due to their different parasitic capacitance, resistance, and inductance in the discharging paths. The manufacturers and users of ICs have derived several ESD stress models and test methods based on different cases of

real-world ESD phenomenon. These ESD models and test methods produce repeatable discharge pulses to characterize and classify the sensitivity and robustness of ESD protection structures under different ESD events. The typical ESD models include human body mode (HBM), machine model (MM), charged device model (CDM) and system-level IEC61000-4-2 model. The simplified RLC equivalent circuits with ideal switches are developed to describe those different models. Their implementation in real ESD test system is associated with additional distributed parasitic elements connected to the stressed ICs. The values of resistor, inductor and capacitor in model circuits are based on the different system parasitic parameters. Different standardization groups such as ESD Association (ESDA) and Joint Electron Device Engineering Council (JEDEC) still continuously review and re-edit these models to specify globally applied and cost-effective test methods.

1.3.1 HBM model

The human body mode (HBM) was developed to represent the ESD event caused by charged human body discharging the current into a grounded IC. Under various conditions, the human body can be charged with static electricity. When the charged human body contacts a grounded semiconductor device or integrated circuit directly, the static charge will transfer from the human body into the device or circuit. The HBM model is the most classical and commonly used discharge model in semiconductor industry. Several HBM simulation circuits and pulse waveforms exist based on different standardized test models. The primary HBM standards include JEDEC JESD22-A114-B [7] and ESDA STM5.1-1998 [8]. Figure 1.2 shows the simplified equivalent circuit of HBM model, where the value of $\mathrm{C_{HBM}} = 100\mathrm{pF}$, $\mathrm{R_{HBM}} = 1.5\mathrm{k\Omega}$,

and $L_{HBM} = 7500nH$ are typically used to model the capacitor, resistor and inductor of a charged human body.

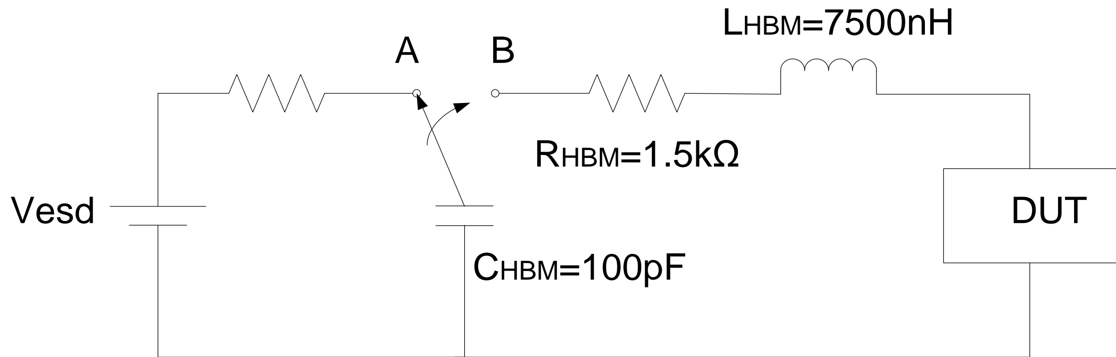


Figure 1.2: A simplified equivalent circuit for HBM ESD model

1.3.2 MM model

In addition to human body, the manufacturing machines can also accumulate static charges in semiconductor fabrication environment. Once the charged machine is in contact with a grounded device or circuit, the accumulated charges can transfer from the machine into the device or circuit. The machine model (MM), intended by the Japanese IC manufacturers to create a worst-case HBM event, replicates the discharging event from a charged machine into a grounded IC. The primary MM standards include JEDEC JESD22-A115-A [9], ESDA STM5.2-1999 [10] and AEC-Q100-003-Rev-E [11]. A simplified equivalent circuit of MM model is shown in Figure 1.3, where the $C_{MM} = 200pF$ and $L_{MM} = 750nH$. The damage on IC caused by MM ESD stress is similar to HBM event. However, due to the higher parasitic capacitance and lower overall impedance during the MM discharge, the MM damages usually occur at a much lower threshold level.

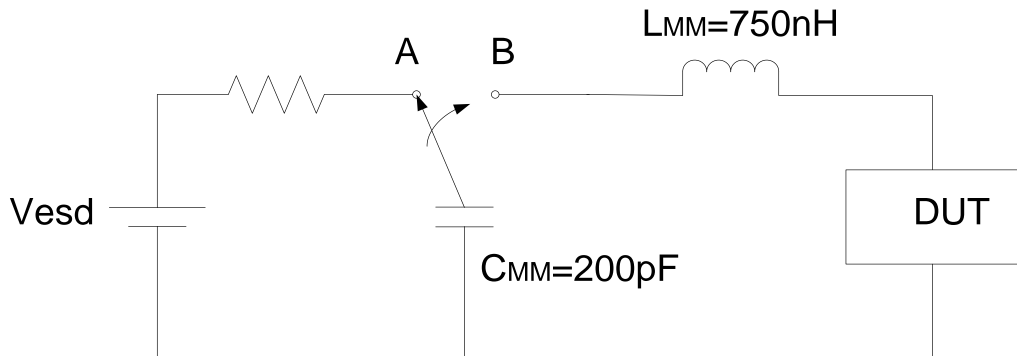


Figure 1.3: A simplified equivalent circuit for MM ESD model

1.3.3 CDM model

Both HBM and MM models replicate the ESD events occur when charged objects (e.g., human body or manufacturing machine) discharge current into a grounded semiconductor device or integrated circuit. However, the device or circuit itself can also store static charges during various manufacturing and automatic handling stages. When any pin of a charged IC-package is toughed by a grounded surface, the electrostatic discharge happens from the inside of IC to the outside ground. The charged device model (CDM) was developed to replicate the integrated circuit self-charging and self-discharging events. Two different methods are defined to charge the device under test (DUT): direct contact charging and filed-induced charging. The filed-induced charging is recommended by many test standards since the possible charging damage can be avoided with electrical field induction. The primary CDM standards are known as JEDEC JESD22-C101-A [12] and ESDA STM5.3.1-1999 [13]. Figure 1.4 shows the simplified equivalent circuit of CDM model, where the $\mathrm{C_{CDM}} = 10\mathrm{pF}$, $\mathrm{R_{CDM}} = 10\Omega$, $\mathrm{R_L} = 10\Omega$, and $\mathrm{L_S} = 10\mathrm{nH}$. The $\mathrm{C_{CDM}}$ is the sum of all capacitances in the device and package with respect to ground and $\mathrm{R_{CDM}}$ is the total resistance of discharge path. For CDM model, the parasitic capacitance, resistance and inductance is small due to the self-discharge nature of integrated circuit. The CDM levels are dependent on the package sizes and types.

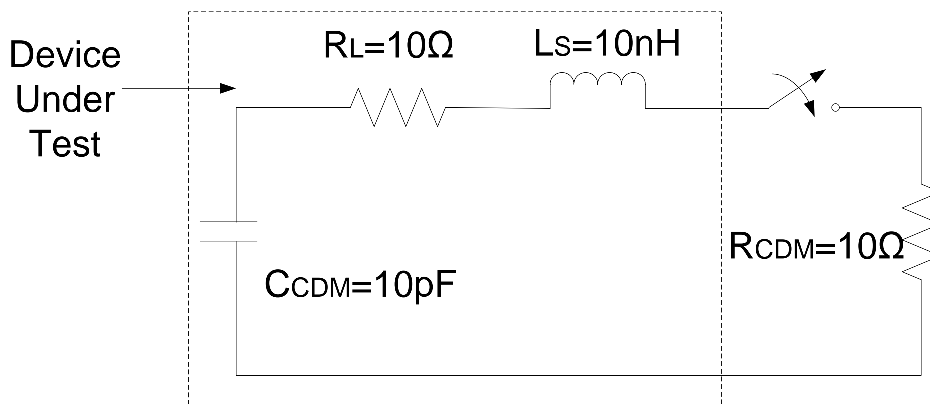


Figure 1.4: A simplified equivalent circuit for CDM ESD model

Figure 1.5 and Table 1.1 compares the different current discharge waveforms of HBM, MM, and CDM ESD models. As shown in Figure 1.5, the HBM pulse has the lowest current peak and longest duration. Under a 2 kV HBM ESD stress, the typical value of peak current is 1.2~1.48 A with a rise time of 2~10 ns and decay time of 130~170 ns. The MM current waveform shows a damped sinusoidal oscillation characteristic and has higher peak current than HBM pulse. A 200 V MM ESD event can generate the current peak reaching 3.5 A in a typical rise time of 10~15 ns and with the pulse duration of approximately 40 ns. Although the pulse width of MM appears to be less than HBM stress, the power dissipation in the ICs is dominated by the time at the peak current level, and this is nearly the same for both HBM and MM events. Different from the HBM and MM models, the CDM ESD is the fastest transient event with highest value of current peak. The CDM discharge can arrive a peak current as high as 12 A within a rise time of only 200 ps under a typical 1 kV CDM ESD stress and dissipates most of its energy in about 1 ns. The resulting damage due to such direct discharge is normally the gate oxide breakdown [14].

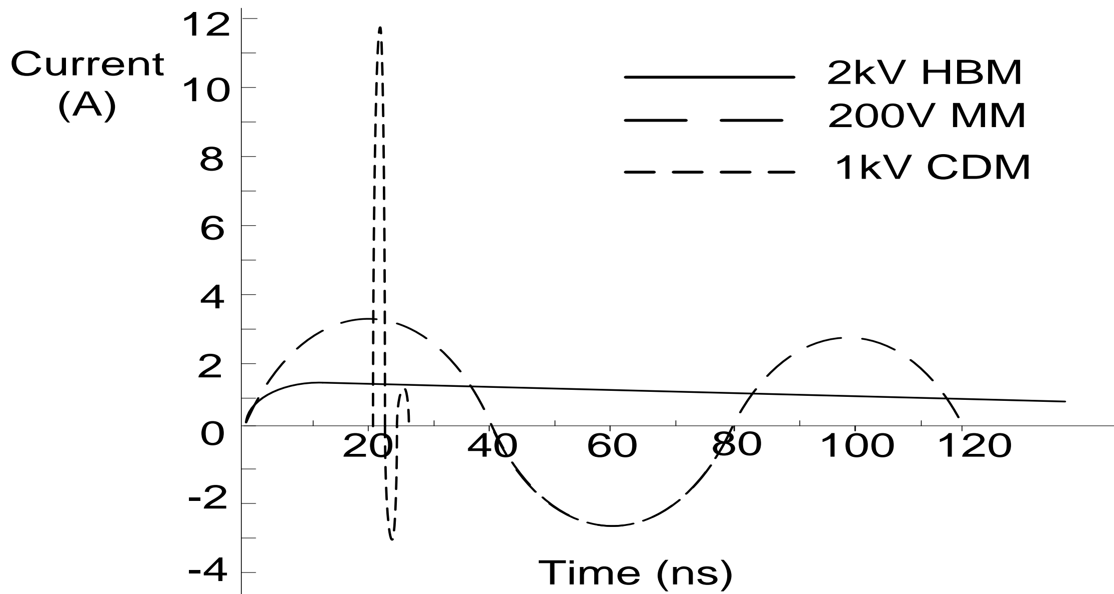


Figure 1.5: Current waveforms of HBM, MM and CDM ESD models

Table 1.1: The comparison of HBM, MM and CDM ESD models

Model	Voltage Level	Peak Current	Rise Time	Pulse Duration
HBM	2kV	1.33A	2~10ns	~150ns
MM	200V	3.5A	10~15ns	~40ns
CDM	1kV	12A	100~500ps	~1ns

1.3.4 IEC model

The traditional HBM, MM and CDM models are developed to ensure the integrated circuits survive being assembled into a finished system during manufacturing environment. However, they are not sufficient for system level testing, where both the voltage and current level of ESD strikes can be much greater in the system end user environment. The purpose of system level testing is to ensure the finished product can survive normal operation where the user of the product usually will not take any ESD precautions to lower ESD stress to the product. The new testing standard IEC61000-4-2 was developed for system level ESD testing [15]. A typical

IEC discharge pulse has a rise time of less than 1 ns and dissipates most of its energy in the first 30 ns with current peak of several tens of amperes. Two different testing methodologies, contact discharge and air-gap discharge, are suggested by IEC test model.

1.3.5 TLP testing

The limitation of existing HBM, MM, CDM and IEC ESD test methods is that they only offer the results of ESD failure threshold for the ESD protection structures, however, without insights into the current-voltage characteristics of those structures during ESD stress and the possible failure mechanisms, which are also critical considerations for designing of ESD protection devices. The transmission line pulsing (TLP) testing technique was introduced by Maloney and Khurana [16] in 1985 to provide such information. The principle for TLP testing is to produce a stable square waveform to stress the device under test by charging a transmission line with high-voltage DC source. Figure 1.6 shows a schematic diagram of current-source TLP system. The transmission line is charged by a high voltage DC source first. When the transmission line discharges, the pulses it creates inject current into the device under test. The TLP testing can provide reliable, repeatable and constant amplitude waveforms. The TLP tester typical begins with low voltage pulses and successively increases in amplitude. The instantaneous current-voltage curves and leakage current information are obtained and visualized with an oscilloscope to describe the behaviors of device under ESD stress.

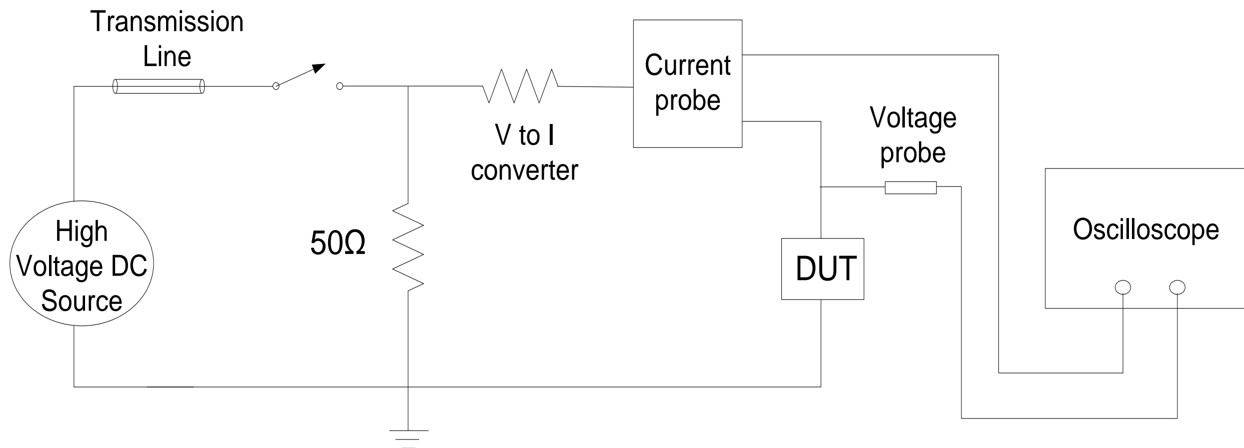


Figure 1.6: Schematic diagram of current-source TLP system

The TLP pulse waveform with a 50-200 ns pulse width and 2-10 ns rise time provides correlation to the HBM pulse of 150 ns exponential pulse width. The TLP and HBM measurement results of different test structures implemented in 0.35 μm [17] and 0.18 μm [18] CMOS technologies verify this correlation. Another technique, named very fast TLP (vf-TLP) testing [19], offers the capability of transient behavior description of ESD protection structures for CDM application.

The use of TLP and vf-TLP testing techniques in ESD industry are now in increasing number. In this work, most of measurements were performed using pulses generated from the Barth 4002 transmission line pulsing (TLP) and Barth 4012 very fast transmission line pulsing (vf-TLP) testers.

1.4 ESD protection

As mentioned in previous section, the electrostatic discharge induced integrated circuit damages occur throughout the whole life of a product from the manufacturing, testing, shipping, handing, to end user operating stages. This is particularly true as microelectronics technology continues shrink to nano-metric dimensions. The ESD related failures is a major IC reliability

concern and results in a loss of millions dollars to the semiconductor industry each year [20]. To avoid or reduce the IC failure due to ESD, two methods are widely used in semiconductor industry. One is using static control and awareness programs to reduce the buildup of static charges and the exposure of ICs to ESD [21]-[22]. It can be achieved by following several rules, such as any person handing the ICs should be grounded with a wrist strap, using work surface made of static-dissipative material, and neutralizing all insulator materials with ionizer. The other method is implementing on-chip ESD protection devices and circuits to shunt high discharge current and keep ESD strikes away from protected internal circuit during ESD event [23]-[24]. Static control and awareness are two important programs to combat ESD in the semiconductor manufacturing stage. However, they are not enough to guarantee the total ESD immunity especially in the end user environment. With the proper design of on-chip ESD protection structures, the threshold of sustainable ESD stress can be significantly increased, resulting in improved reliability of the ICs and electronic systems [25]-[26]. A good on-chip ESD protection structure should achieve high current carrying and voltage clamping capabilities, low leakage current at operating voltage, fast turn-on speed and minimized parasitic effect based on different protection applications.

1.4.1 ESD protection schemes

According to the ESD testing standards, an ESD event should be delivered between any two pins of an integrated circuit. To adequately protect the ICs from damage during ESD event, an ESD protection network must provide the current discharge path between those two pins and must also limit the voltage drop on any sensitive devices, such as gate oxide of an NMOS output driver. There are four kinds of pin combinations for achieving a whole-chip ESD test, which are

known as Pin-to-VDD, Pin-to-VSS, Pin-to-Pin, and VDD-to-VSS [27]-[28]. The VDD and VSS are power supply pin and ground pin respectively. Most ESD solutions rely on shunting current from an I/O pin to a power supply, from which the current can be distributed to other I/O pins or supplies. These solutions fall into two general categories: VDD-based and VSS-based ESD protection [29]. Figure 1.7(a) shows the VDD-based protection scheme, which is comprised of a single-direction ESD protection structure from I/O to VDD (ESD-Cell-1) and VSS to I/O (ESD-Cell-2) paths and a bi-directional power supply clamp between VDD and VSS path. The other VSS-based protection scheme is shown in Figure 1.7(b). It has a dual-direction ESD protection structure (ESD-Cell-3) between I/O and VSS path and a bi-directional power supply clamp between VDD and VSS path. Both VDD- and VSS-based schemes can provide whole-chip ESD protection for the ICs, however, the difference between these two methods becomes apparent when examining the current discharge path under various pin combinations. For example, under the Pin-to-VSS combination, a positive ESD stress is applied to I/O pin when the VSS pin is connected to ground. For the VSS-based protection scheme, the ESD current can flows directly from the ESD-cell-3 to the VSS. On the other hand, for the VDD-based scheme, since there is no shunt path between I/O to VSS directly, the ESD discharge will flows through the ESD-cell-1 onto VDD rail first and reaches the VSS through the power supply clamp. For both cases, the voltage drop on the discharge path should be lower than the failure voltage of devices that they appear in parallel with in the core circuit. The choice of different protection schemes is based on the technology, available ESD protection devices, and the design widow under different protection applications.

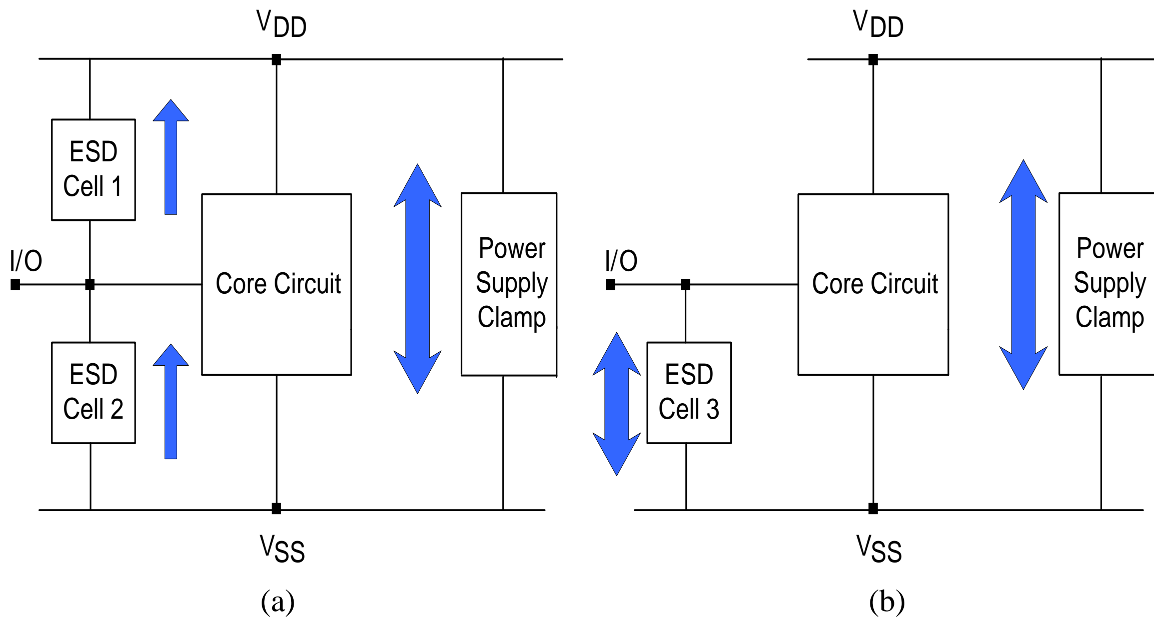
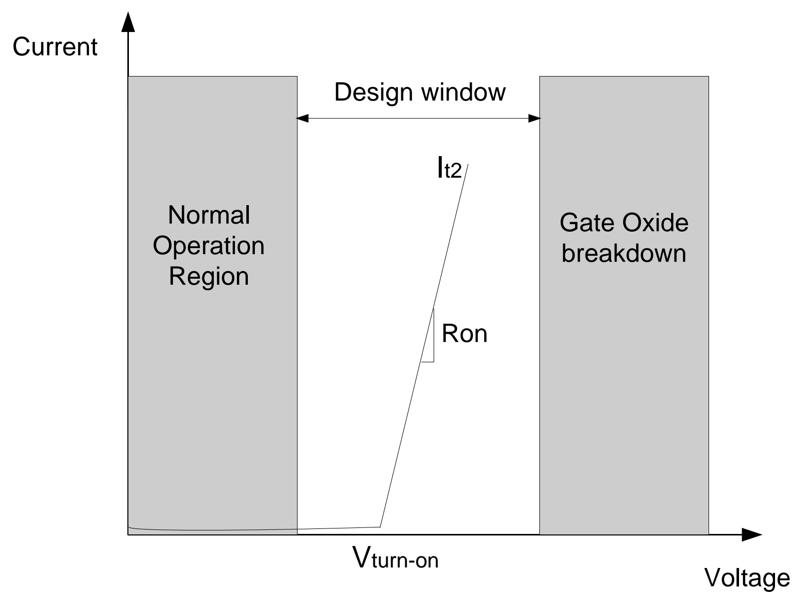


Figure 1.7: The (a) VDD-based and (b) VSS-based ESD protection schemes

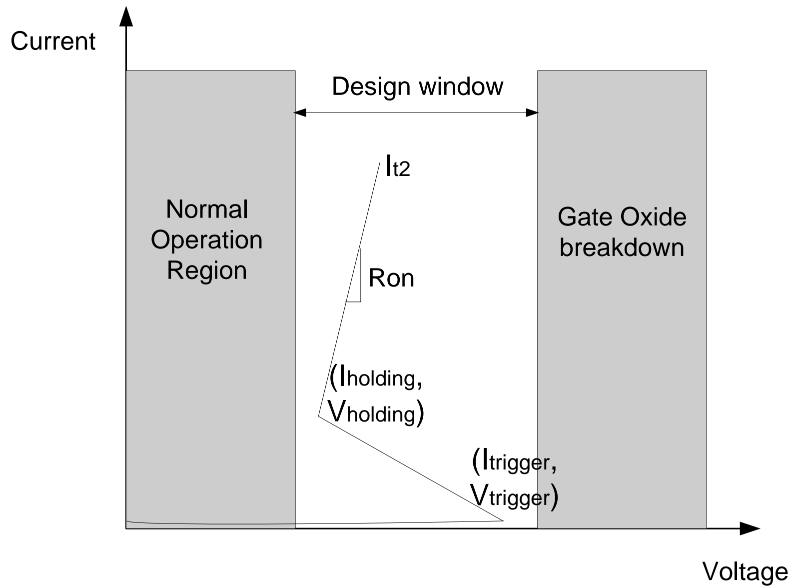
1.4.2 ESD protection devices

ESD is a high current and high energy event. Therefore, the ESD protection structures in discharge path are required to carry amperes of current without be destroying and clamp the voltage drop under a safe region. A number of semiconductor devices can be used as candidates for ESD protection at I/O pins and power supply rails of ICs. Base on the shape of their current-voltage characteristics, they are divided into two main categories: non-snapback devices and snapback devices. The I-V curve and design window of non-snapback device are shown in Figure 1.8(a). For non-snapback device, the voltage on the device increases gradually with a small current first. After the voltage reaches a certain value (e.g., turn-on voltage), the current starts to increase rapidly while the voltage remains almost constant. The key design parameters for non-snapback devices include the turn-on voltage $V_{turn-on}$, on-state resistance Ron and failure current It2. The snapback devices has S-type I-V characteristic as shown in Figure 1.8(b). The trigger voltage $V_{trigger}$, holding voltage $V_{holding}$, on-state resistance Ron and failure current

It2 are their key design considerations. The ESD protection devices should be in off state during normal circuit operation, turning on to discharge current under ESD stress, clamping the voltage across protected structure under safe region, such as breakdown voltage of gate oxide, and turning off after the ESD event. The design window gives ESD designers the guideline for realizing effective ESD protection without interfering with the normal operation of the protected circuits. The key considerations for effective ESD design include: (1) the turn-on voltage $V_{turn-on}$ for non-snapback device or trigger voltage $V_{trigger}$ for snapback device and the clamping voltage at the required ESD protection level have to be lower than the breakdown voltage of internal circuitry, (2) the holding voltage $V_{holding}$ of snapback device as supply clamp has to be larger than the power supply voltage to avoid latch-up problems, (3) low leakage current at operating voltage and (4) good robustness, i.e., high failure current It2.



(a)



(b)

Figure 1.8: I-V characteristics and design windows of (a) non-snapback and (b) snapback device

The most commonly used non-snapback ESD protection devices are PN junction diode, zener diode and diode string. Because of its simple structure and good performance, the junction diode is widely used for ESD protection at I/O pins of integrated circuits [30]-[32]. The forward-biased junction diode can conduct significant current with very low on-state resistance when the applied voltage is greater than its turn-on voltage which is normally 0.7 V. Zener diode and diode string with higher turn-on voltages compared to junction diode are usually used as power supply clamp [33]-[35]. Zener diode formed by highly doped N+ and P+ diffusion regions works under reverse bias condition and has lower triggering voltage than regular reverse-biased junction diode. Diode string with forward-biased junction diodes in series gives the flexibility to control its turn-on voltage by adjusting the number of diodes. The cross section of junction diode, zener diode and diode string are shown in Figure 1.9, respectively.

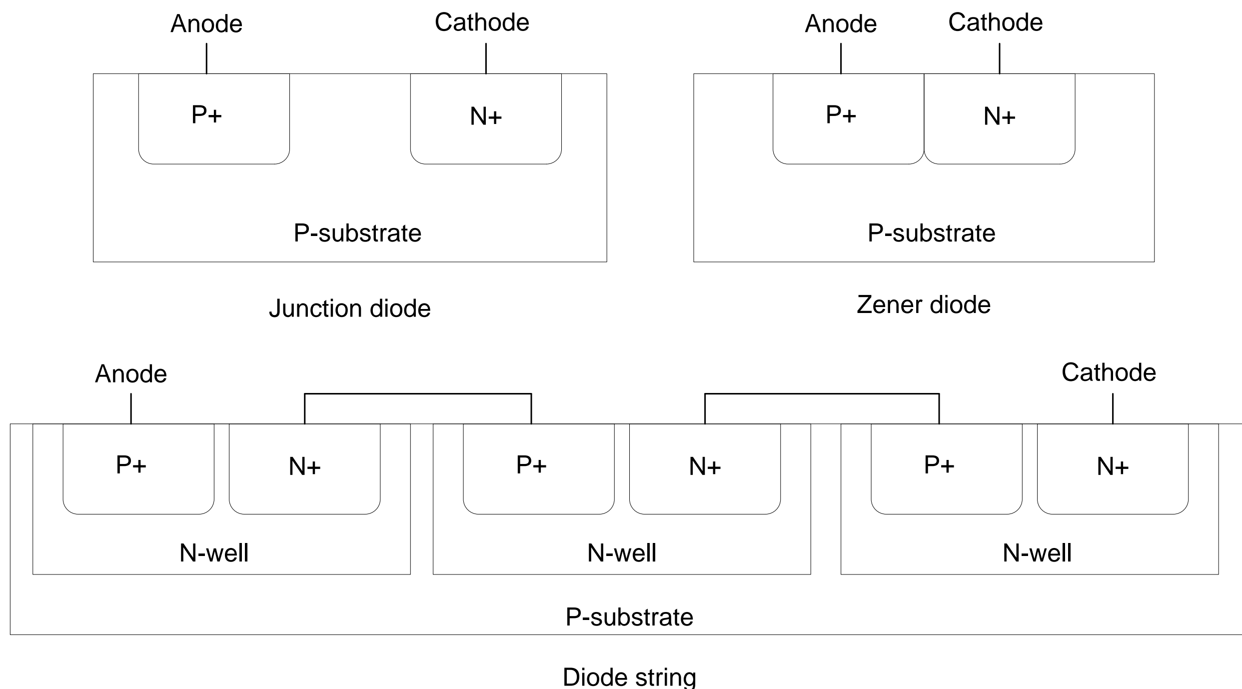


Figure 1.9: Cross sections of junction diode, zener diode and diode string

The snapback devices with controllable triggering and holding voltages are widely used for ESD protection applications at I/O pins and power supply rails. The Grounded-Gate NMOS (GGNMOS) [36]-[37] and Silicon-Controlled Rectifier (SCR) are two most important snapback devices in the CMOS technology [38]-[40].

Figure 1.10 shows the cross section and equivalent circuit of a GGNMOS device. The gate and source contacts of NMOS transistor are shortened to ensure turn-off of NMOS function at all times. When ESD pulse stresses on the drain contact of GGNMOS, the parasitic NPN bipolar transistor formed by the N+ drain contact, the P-substrate and N+ source contact turns on to sink the ESD current under a certain voltage and current. The GGNMOS goes into snapback operation region. One drawback of GGNMOS device is that it can suffer long-term reliability problems if a relatively large electric field is applied at the gate during the ESD event.

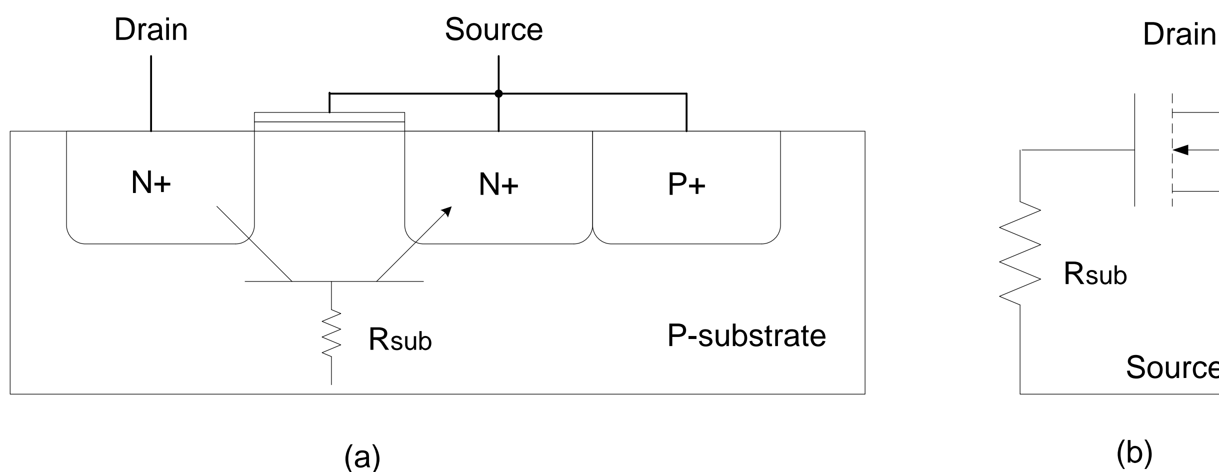


Figure 1.10: (a) Cross section and (b) equivalent circuit of GGNMOS

SCR is also known as the thyristor. Figure 1.11 shows the cross section and equivalent circuit of a SCR device. The SCR consists of a PNPN structure. Its anode and cathode are formed by the P+ diffusion region in N-well and the N+ diffusion region in P-substrate, respectively. The trigger of SCR is followed by the turn-on of parasitic NPN (N-well/P-substrate/N+ cathode) bipolar and PNP (P+ anode/N well/P-substrate) bipolar transistors. SCR is the most efficient protection structure in terms of ESD performance per unit area. However, its compact model is not widely available due to the operation of SCR for ESD protection is in high-current and breakdown regimes which the regular circuit models do not cover.

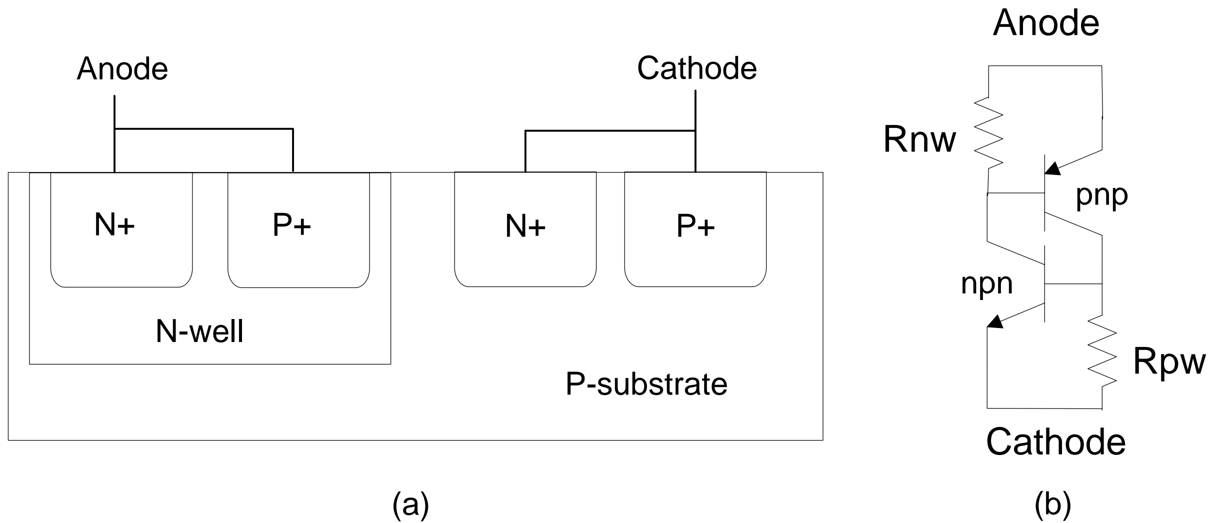


Figure 1.11: (a) Cross section and (b) equivalent circuit of SCR

1.5 Summary

The static charges are generated in both fabrication and end user environments, including all the stages through the manufacturing, testing, shipping, handing to user operating. The electrostatic discharge can occur as the result of a discharge to the device, from the device, or field-induced discharge. The ESD induced failures can be catastrophic, where the semiconductor devices or integrated circuits are damaged immediately, or ESD can result in latent defect that may escape immediate attention. Several ESD stress models and test methods are developed by semiconductor industries to simulate the real world ESD phenomenon and characterize the sensitivity of device or circuit attributed to different types of ESD events in an IC environment. The on-chip ESD protection structures and schemes are implemented to effectively guard the microchips against ESD induced damage.

The organization of the dissertation is as following. Chapter 2 starts with design and optimization of LOCOS-bound diode. The effects of different diode geometries, metal connection patterns, dimensions and junction configurations on the ESD robustness and parasitic

capacitance are investigated experimentally. The results provide useful insights into optimizing the diode for robust HBM ESD protection applications. Chapter 3 compares the current carrying and voltage clamping capabilities of LOCOS- and polysilicon-bound diodes based on both TCAD simulation and experimental results. The better performed polysilicon-bound diode will then be investigated in more detail. Two figures of merits are developed to better assess the effects of different design parameters on polysilicon-bound diode's overall ESD performance. Chapter 4 investigates the transient behavior of polysilicon-bound diodes under fast ESD events such as CDM. The effects of changing devices' dimension parameters on the overshoot voltage and turn-on time are studied experimentally using pulses generated by the very-fast TLP tester. The correlation between the diode failure and poly-gate configuration under the VFTLP stress is also investigated. In chapter 5, the turn-on uniformity of two multi-finger silicon-controlled rectifiers (SCRs) with different combinations of anode/cathode regions are studied using the transmission line pulsing (TLP) tester. The finger turn-on mechanisms of these devices are explained from the current flow path and equivalent circuit views. The dV/dt effect of pulses with different rise times on the finger turn-on behavior of the SCRs are also investigated experimentally. Chapter 6 comes summary and conclusion of the dissertation.

CHAPTER 2. DESIGN AND OPTIMIZATION OF LOCOS-BOUND DIODES FOR ESD PROTECTION APPLICATIONS

Because of its simple structure and good performance, diodes are frequently used in providing on-chip electrostatic discharge (ESD) protection solutions for various integrated circuits [41]-[44]. However, when the diode operates under the ESD stress, its current density and temperature are far beyond the normal conditions and the device is in danger of being damaged. To this end, the failure current level It2 is an important indicator as it dictates the robustness of ESD protection devices. This current is defined as the point where the measured transmission line pulsing (TLP) I-V curve deviates significantly from its linearly extrapolated value or the leakage current increases considerably from its normal value [45].

For the design of effective ESD protection solutions, the ESD robustness and low parasitic capacitance are two major considerations. ESD robustness is usually defined as high failure current It2 and low on-state resistance Ron, which can be affected by several design factors such as the device's dimension, geometry, finger number, junction configuration, and metal connection pattern. In this work, we will focus on LOCOS-bound diodes fabricated using the IBM BiCMOS technology. Diodes with various layouts, metal patterns, geometries, and dimensions will be considered, and their It2 and Ron measured using Barth 4002 TLP tester with a pulse width of 100 ns and rise time of 10 ns will be compared and discussed. The work will provide useful information on design and optimization of LOCOS-bound diodes for low-voltage ESD protection applications.

2.1 LOCOS-bound diode

LOCOS, short for Local Oxidation of Silicon, is a traditional fabrication process for growing oxide insulation structures. The silicon dioxide is formed in the selected regions of a silicon wafer with Si-SiO_2 interface lower than the rest of silicon surface. Figure 2.1 shows the cross section of an N+/P-well junction LOCOS-bound diode, where the grey areas denote the LOCOS oxide separating the P+ anodes and N+ cathode of diode, and La and Lc are the length of anode and cathode diffusion regions, respectively.

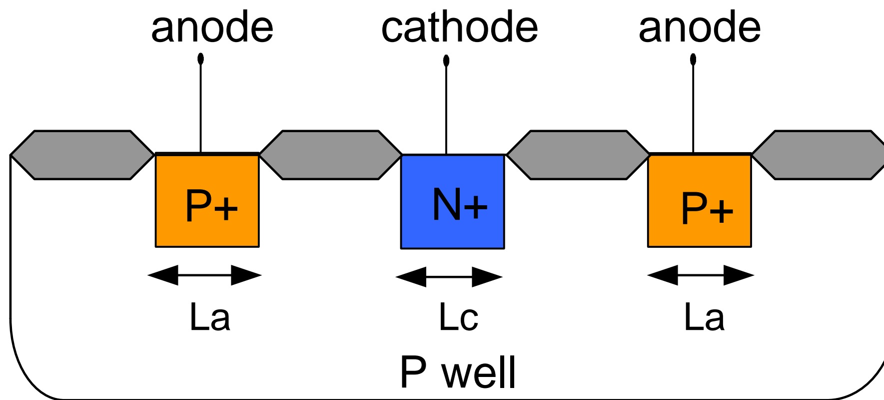


Figure 2.1: Cross section of N+/P-well junction LOCOS-bound diode

The ESD robustness and parasitic capacitance of LOCOS-bound diode depends on several design factors, including the different layout structures of N+/P+ diffusion regions, different metal connection patterns, junction configurations, geometries and dimension parameters. In the following discussion, the effect of each factor will be investigated in detail and an optimal combination of those factors will be achieved for reaching the objectives of high performance ESD protection application.

All measurements will be conducted using the Barth 4002 TLP tester which generates pulses with a width of 100 ns and a rise time of 10 ns, a stress condition equivalent to that of the human body model (HBM).

2.2 Layout structures

Two different layout structures for N+/P-well LOCOS-bound diode are shown in Figure 2.2. The one on the left is called the stripe structure, where the N+ and P+ diffusion regions are laid out as stripes. The W and L are the width and length of diffusion region respectively. In this device, one N+ diffusion stripe is located in the middle and two P+ diffusion stripes are placed on each side. The majority of diode's current flows from the two P+ regions to the N+ region along the width W of the diffusion regions. The one on the right is called the waffle structure [46]-[47]. In this device, the N+ diffusion region is divided into several small squares, and each N+ square is surrounded by the P+ diffusion region. The current flows from the P+ region into the N+ regions along the perimeter of each N+ square. The red arrows show the current conduction paths. The two diode structures are designed with the same PN junction area, where for the stripe structure the junction area is W*L and for the waffle structure the area is d*d*N (N is the number of squares).

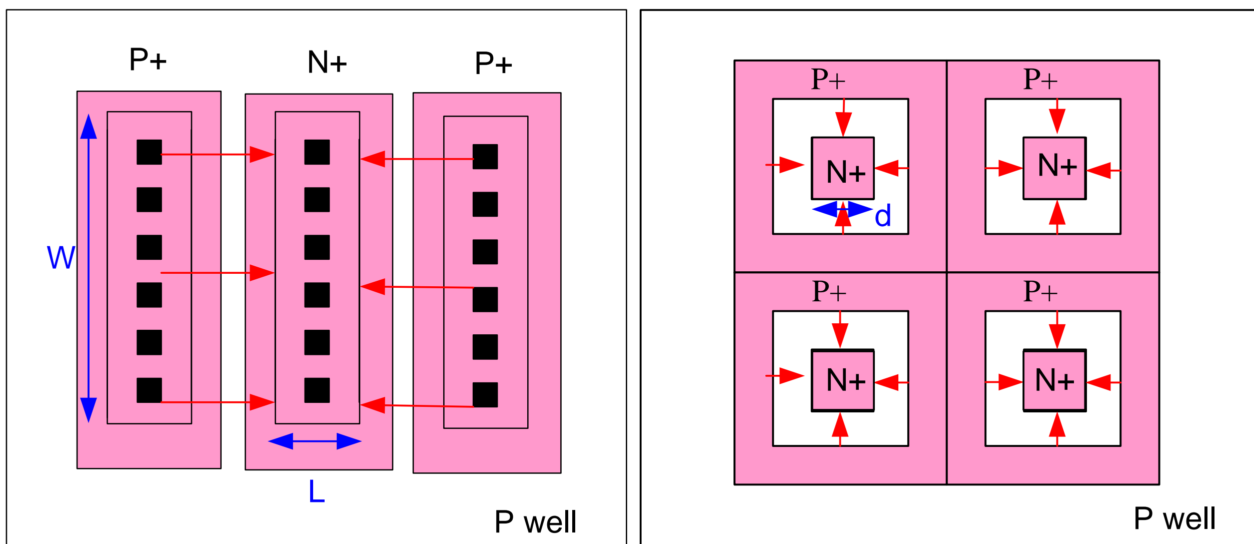


Figure 2.2: N+/P-well LOCOS-bound diodes having the stripe (left) and waffle (right) structures

Figure 2.3 shows the I-V characteristics of stripe and waffle structure LOCOS-bound diodes with the same junction area of 64 μm^2. For stripe structure diode, the W and L are 40 μm and 1.6 μm respectively. For waffle structure, the diode has square number N of 25 with the cell size d equal to 1.6 μm for each square, where the 1.6 μm is the smallest value can be used under this specified BiCMOS technology. As expected, the waffle structure diode shows a higher failure current It2 (3.9 A) than its stripe counterpart (3.5 A) since the current distribution is more uniform along the perimeters of multiple N+ squares. However, the ESD performance of waffle structure diode highly depends on the combinations of its d and N values under a same PN junction area.

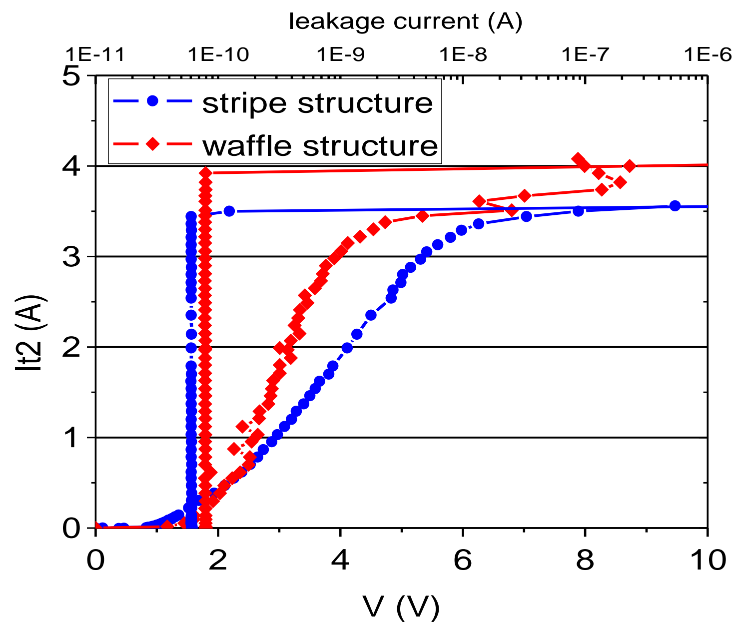


Figure 2.3: I-V characteristics of stripe and waffle N+/P-well LOCOS-bound diodes

Figure 2.4 shows the failure current It2 of waffle structure diodes having cell size d increasing from 1.6, 2, 4 to 8 μm and square number N decreasing from 25, 16, 4, to 1. It can be seen, increasing d and reducing the number N of squares, while keeping the same total PN

junction area, the waffle structure diode's failure current decreases significantly from 3.75 A to 2.1 A. The combination of smaller cell size and more square numbers gives higher ESD protection performance for diode with waffle structure layout. However, since the d with 1.6 μm is the smallest value available for this specified technology, the highest failure current for waffle structure diode is limited to 3.75 A. Considering the complex and time-consuming layout required for the waffle structure, the minor ESD robustness improvement does not warrant the use of such a structure. As such, we will focus on the stripe LOCOS-bound diode in the following discussion.

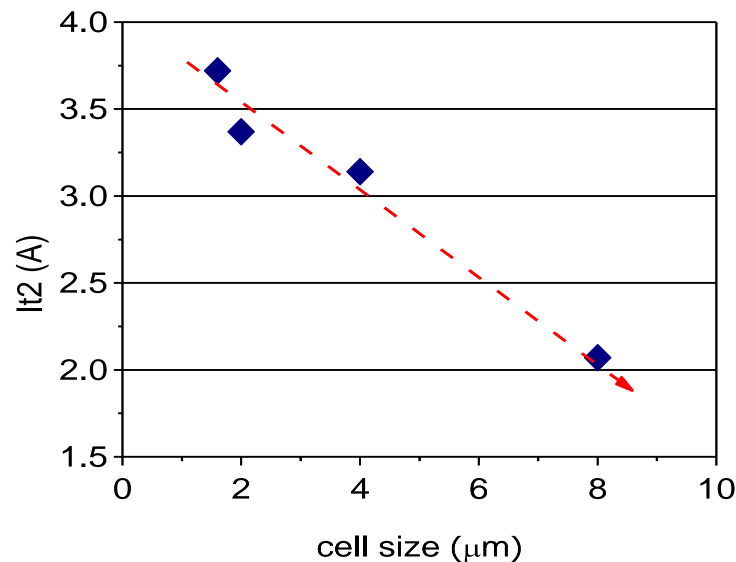


Figure 2.4: Failure current It2 of waffle structure diodes with different cell sizes

2.3 Metal connection patterns

There are several different metal connection patterns for the N+/P-well diode: the parallel pattern [48]-[49], tapered pattern [48], [50], and crossing pattern [45], [49]. Different metal

connection patterns affect diode's current carrying and voltage clamping capabilities and consequently its failure current and on-state resistance.

2.3.1 Parallel metal pattern

Figure 2.5 shows the layout of the parallel metal pattern. The N+ and P+ diffusion regions are covered by low level metal-1 lines (pink color) and the high level metal-2 lines (green color) are placed in parallel with the diffusion regions and connected to metal-1 lines by multiple vias. W_m is the metal width, and L and W are the length and width of the N+/P+ diffusion regions, respectively. The width W of the diffusion region is also defined as the diode width. Under the forward ESD stress condition, the current starts from diode's anode on the right hand side, flows perpendicularly across the LOCOS oxide region between the P+ and N+ diffusion regions, and exits from the cathode on the left hand side. However, the distribution of current in the diode is highly non-uniform. A higher current density occurs in the areas close to the electrodes (i.e., anode and cathode) and a lower current density occurs in the mid-section of the diffusion regions. The further away from the electrodes, the lower is the current density. The non-uniform current distribution phenomenon of LOCOS-bound diode with parallel metal pattern can be verified by the following two groups of experiments.

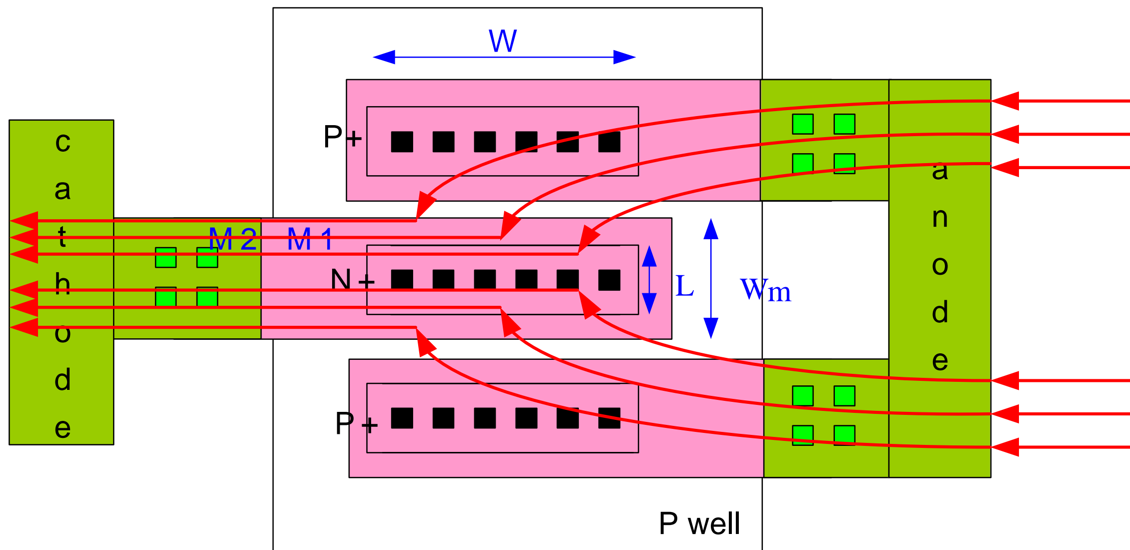


Figure 2.5: Layout of LOCOS-bound diode with parallel metal pattern

Experiment 1 investigates the width of metal-1 line (W_{m1}) affecting on the failure current and on-state resistance of LOCOS-bound diode. As shown in Figure 2.6, the diode-1 at the left side has metal-1 width of 2.8 μm (e.g. W_{m1}= 2.8 μm), which is the largest value available for this specified BiCMOS technology to avoid any layout error under design rule check. Keeping all other design parameters same, the diode-2 at the right side reduces the width of metal-1 line to half of diode-1's (e.g., W_{m1}=1.4 μm). Two groups of N+/P-well LOCOS-bound diodes are fabricated under the same junction area for comparison. The diodes in group 1 have long diffusion width (W=20 μm) and less anode/cathode fingers (5 fingers) and diodes in group 2 have short diffusion width (W=10 μm) and more finger numbers (10 fingers). Table 2.1 compares the failure current It2 and on-state resistance Ron of diodes in the two groups. It's clear to see, the diode-2 in both groups have lower failure current and higher on-state resistance than diode-1. This is because the narrow width of metal-1 line causes the increase of current density at regions near the electrodes and finally results in the melting of metal lines.

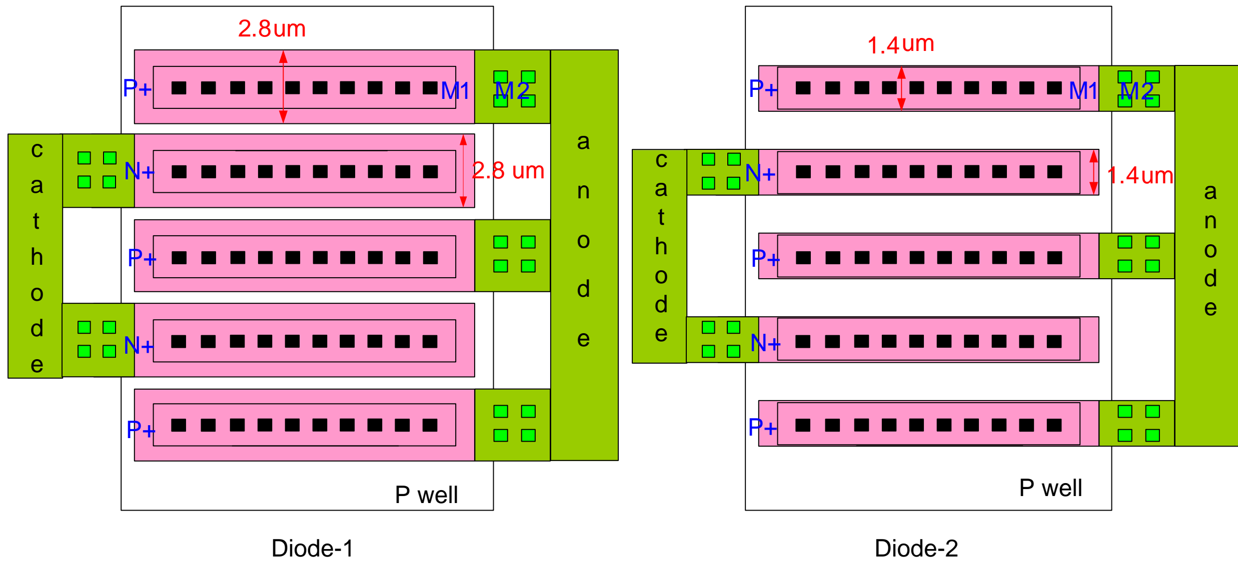


Figure 2.6: Experiment 1: Diode-1 (left) with W_{m1}=2.8 μm and Diode-2 (right) with W_{m1}=1.4 μm

Table 2.1: Failure current and on-state resistance of Diode-1 and Diode-2 in two groups

	Diode-1 10fingers W=10 μm W_{m1}=2.8 μm	Diode-2 10fingers W=10 μm W_{m1}=1.4 μm	Diode-1 5 fingers W=20 μm W_{m1}=2.8um	Diode-2 5 fingers W=20 μm W_{m1}=1.4 μm
Failure current It2 (A)	8.65	7.37	6.53	4.02
On-state resistance Ron (Ω)	0.52	0.6	0.63	1.04

In experiment 2, the LOCOS-bound diodes with parallel and tapered metal connection pattern are compared. Figure 2.7 shows the layout of diode-3 with the tapered metal pattern, where the metal-1 lines are divided into three parts with equal length. The parts nearest to the electrodes (i.e., anode and cathode) have the widest metal-1 width of 2.8 μm which is the same as that of diode-1 device, then the width reduces to 2.1 μm for those in the middle regions, and the parts furthest to the electrodes have the narrowest metal-1 width of 1.4 μm. All other design parameters are kept the same and two groups of diodes are fabricated. Table 2 shows the It2 and Ron of diodes in the two groups. In contrast to diode-2 shown in table 1, the diode-3 with tapered

metal pattern and diode-1 with parallel metal pattern have same value of failure current and on-state resistance for both groups. This is because diode-3 has the same metal-1 width (e.g., W_{m1}=2.8 μm) as diode-1 at the regions close to the electrodes, the current density is reduced and gives uniform current distribution.

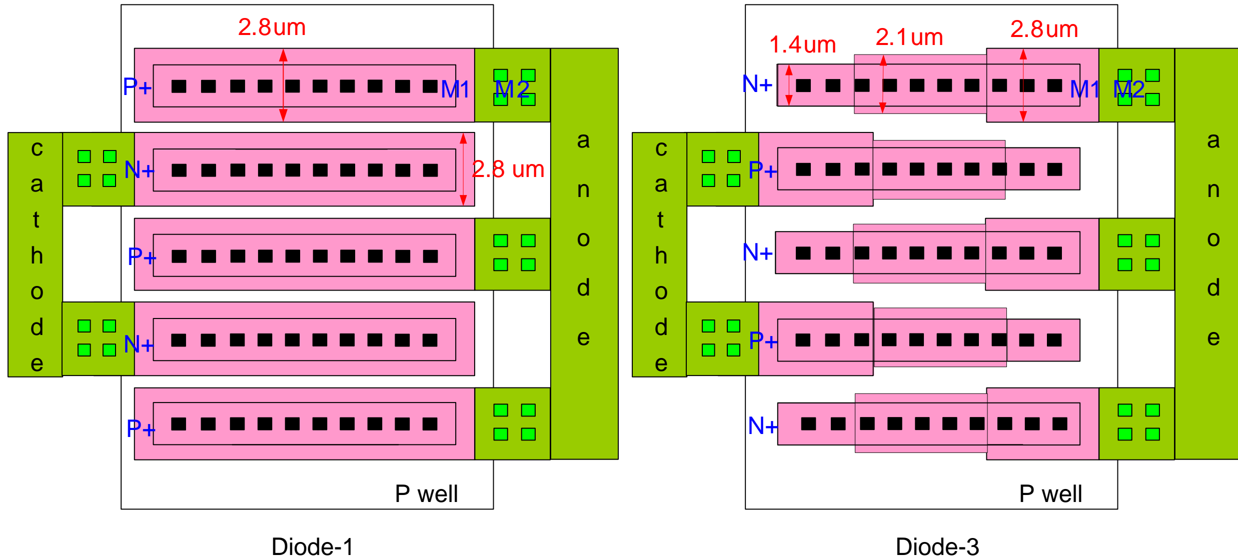


Figure 2.7: Experiment 2: Diode-1 (left) with parallel metal pattern and Diode-3 (right) with tapered metal pattern

Table 2.2: Failure current and on-state resistance of Diode-1 and Diode-3 in two groups

	Diode-1 10 fingers W=10 μm Parallel pattern	Diode-2 10 fingers W=10 μm Tapered pattern	Diode-1 5 fingers W=20 μm Parallel pattern	Diode-2 5 fingers W=20 μm Tapered pattern
Failure current It2 (A)	8.65	8.66	6.53	6.54
On-state resistance Ron (Ω)	0.52	0.51	0.63	0.62

The measurement results in experiment 1 and 2 reveal the phenomenon that current distribution in the LOCOS-bound diode with parallel metal pattern is highly non-uniform, with a higher current density occurs in the areas close to the electrodes (i.e., anode and cathode) and a

lower current density occurs in the mid-section of the diffusion regions. The further away from the electrodes, the lower is the current density. The non-uniform current distribution decreases diode's current carrying capability and consequently degrades its ESD robustness, especially for diodes with a large W. Figure 2.8 shows the It2 of parallel metal pattern diodes with L=1.6 μm and W changing from 10 to 40 μm. It is shown that It2 increases linearly with increasing W when W is smaller than 20 μm. However, beyond 20 μm, It2 is saturated. This is because the metal width W_m is independent of W, and for a relatively large W, W_m becomes the main factor limiting the current carrying capability. As such the metal lines can be damaged even the diffusion regions can survive the ESD stress.

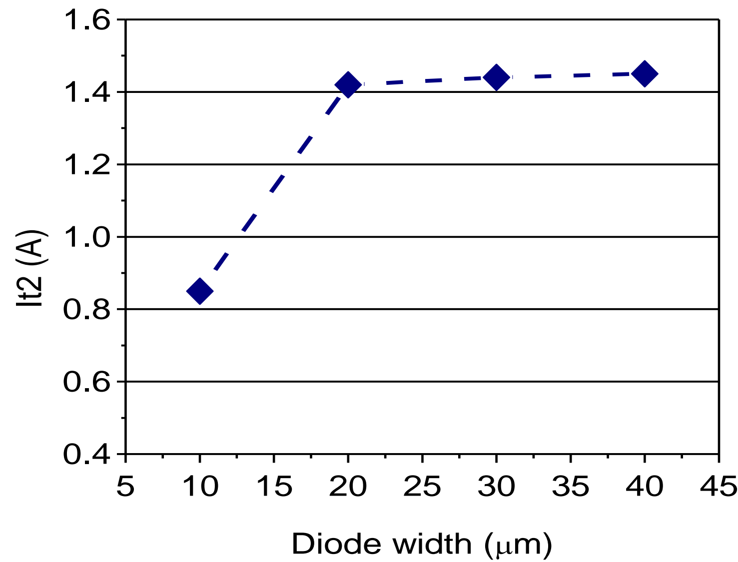


Figure 2.8: It2 of parallel metal pattern diodes having different widths

The junction area of the diode is equal to W*L. Diodes with the parallel metal pattern exhibit very low failure current It2 per junction area, especially when the diode width W is large. One solution to this problem is keeping a short diode width and using multiple anode/cathode fingers. Figure 2.9 shows the results of diodes having a fixed W of 10 μm and finger number

increasing from 1 to 4. Clearly, It2 increases linearly with increasing finger number. However, the expenses of having too many fingers are the larger die size and increased parasitic capacitance.

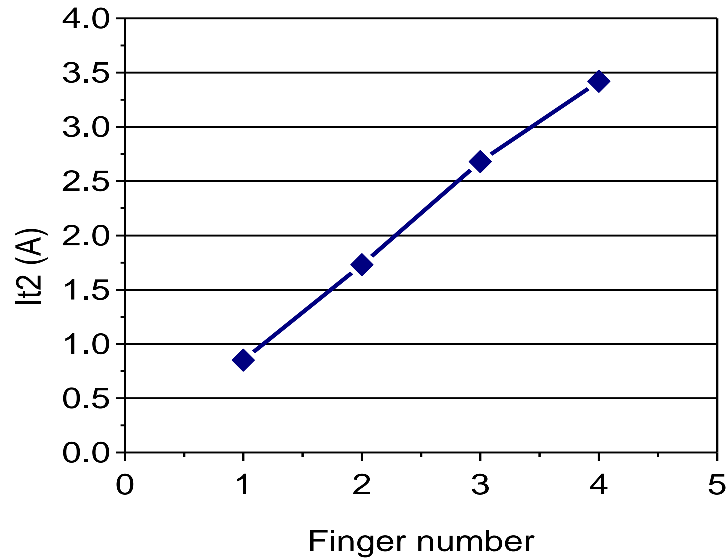


Figure 2.9: It2 for parallel metal pattern diodes having different finger numbers

2.3.2 Crossing metal pattern

Another type of metal connection called the crossing metal pattern is shown in Figure 2.10. The N+ and P+ diffusion regions are still covered by the low level metal-1 lines, however, the high level metal-2 lines are placed across the diffusion regions. Multiple rows and columns of vias are then used to connect metal-1 and 2. Under the forward ESD stress condition, the current starts from the anode on the left hand side, flows in and out of the diode's diffusion regions from the different vias connected between metal-1 and metal-2, and then exits from the cathode on the right hand side. Because of the symmetry of the current paths, the current distribution in crossing metal pattern diode is more uniform and consequently the failure current It2 is higher than those of the parallel metal pattern diode.

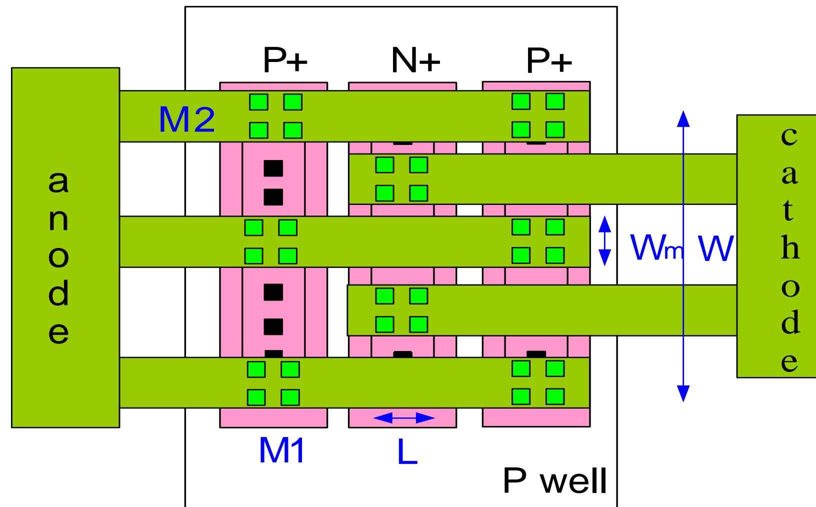


Figure 2.10: Layout of LOCOS-bound diode with crossing metal pattern

Figure 2.11 shows the results of crossing pattern diodes having L=1.6 μm and W changing from 10 to 40 μm. In contrast with the trend observed in Figure 2.8, the failure current It2 increase linearly and monotonically with increasing W. Since the diodes with the crossing metal pattern show superior current carrying capability, these devices will be the focus of our following analysis.

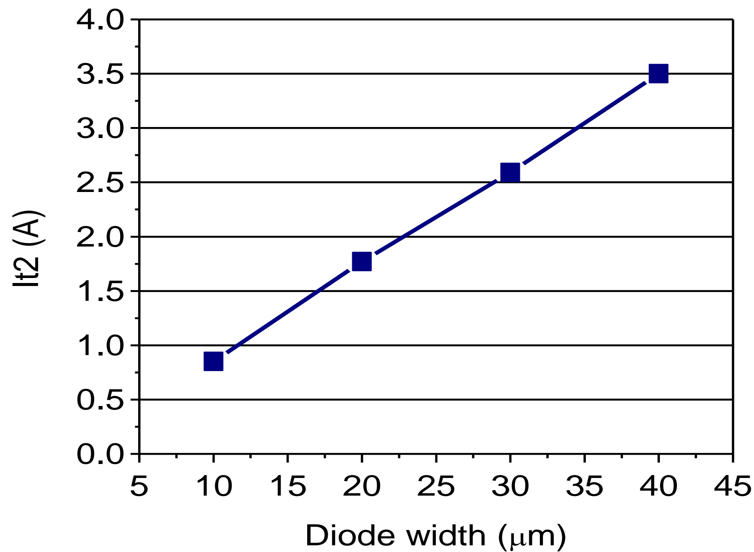


Figure 2.11: It2 for crossing pattern diodes having different widths

2.4 Dimension consideration

Figure 2.12 and 2.13 show the failure current It2 (blue line) and on-state resistance Ron (red line) of N+/P-well LOCOS-bound diode versus the anode length La and cathode length Lc, respectively. It is clear to see, both It2 and Ron are insensitive to La, whereas changing the cathode length Lc alters It2 and Ron quite significantly as It2 increases and Ron decreases almost linearly with increasing Lc from 1.6 to 4.8 μm.

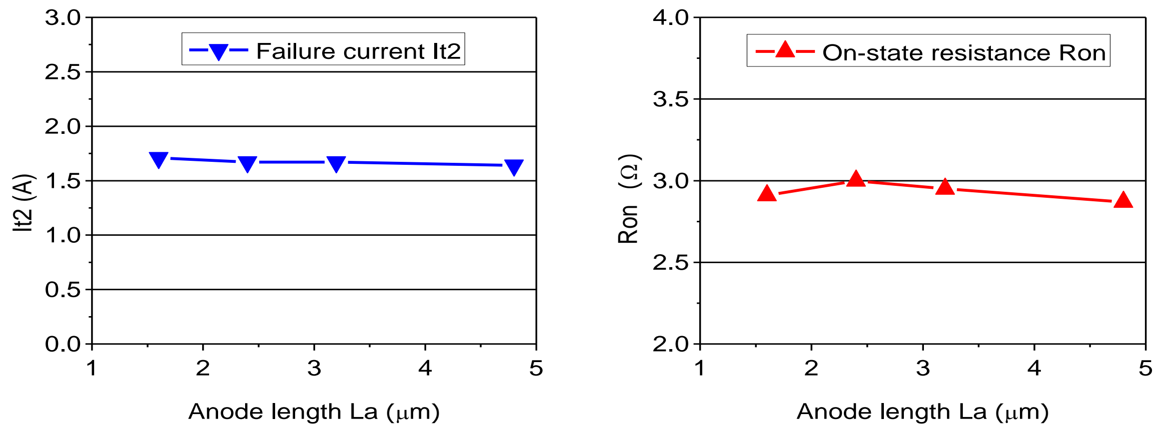


Figure 2.12 It2 (left) and Ron (right) of N+/P-well LOCOS-bound diode vs. anode length La

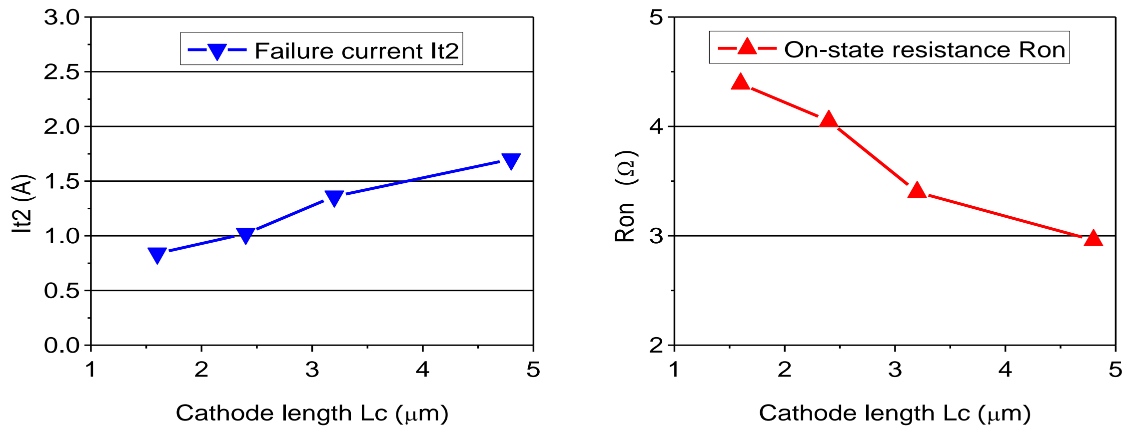


Figure 2.13: It2 (left) and Ron (right) of N+/P-well LOCOS-bound diode vs. cathode length Lc

Figure 2.14 shows the I-V characteristics of N+/P-well diodes having the same total width but different finger numbers. Diode 1 has 1 finger with a width of 80 μm, diode 2 has 2 fingers each with a width of 40 μm, and diode 3 has 4 fingers each with a 20 μm width. While these devices have the same total width, their failure current It2 and on-state resistance Ron differ considerably. Diode 1 possesses the highest It2 and lowest Ron. This is due to the fact that the total width of metal-2 lines in such a device is the largest among the three diodes considered.

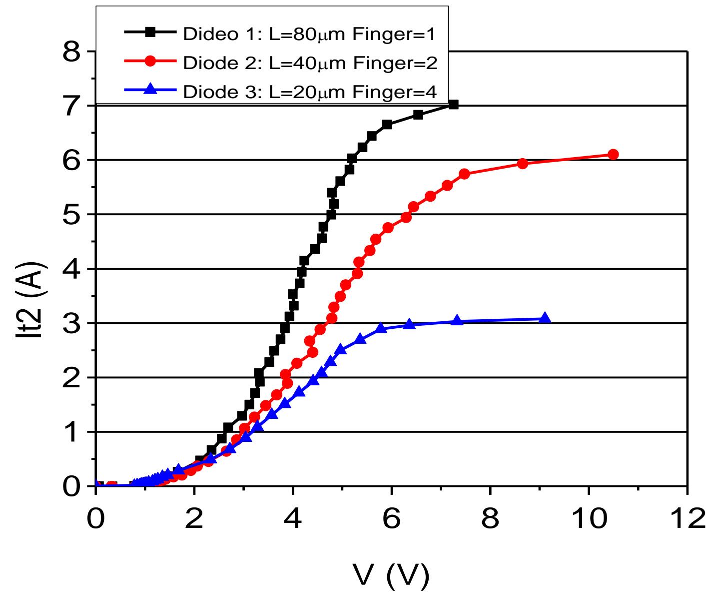


Figure 2.14: I-V characteristics of N+/P-well diode having the same total width but different finger numbers

2.5 Geometry consideration

As mentioned above, the diode width W, cathode length Lc and finger number N all affect the ESD performance of the N+/P-well diodes. Since the diode's parasitic capacitance primarily depends on the area of its N+ region, keeping the same N+ area and finding an optimal combination of those parameters to achieve the highest It2 and lowest Ron is highly desirable for

reaching the objectives of robust ESD protection and low capacitance. Figure 2.15 shows three different diode geometries with the same N+ diffusion area but different combination of W, Lc and N. Geometry 1 has a single finger, large diode width 2*W and short cathode length Lc. Geometry 2 has two fingers, a small diode width W and short cathode length Lc. Geometry 3 has a single finger, small diode width W and long cathode length 2*Lc.

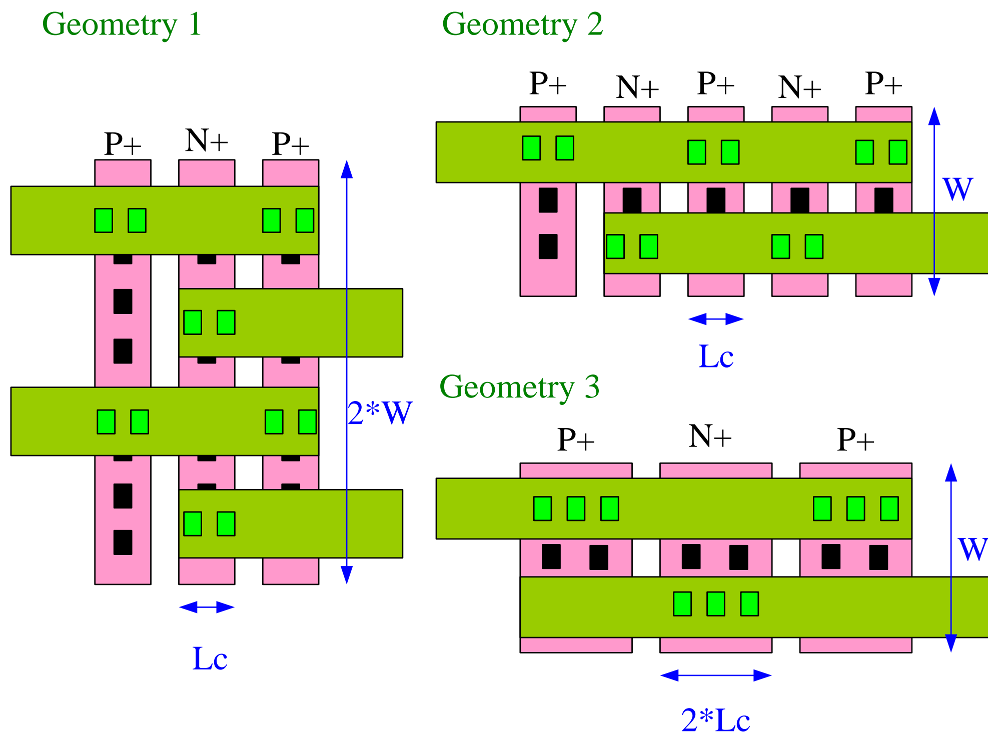


Figure 2.15: Three different N+/P-well diode geometries having different diode widths, cathode lengths and finger numbers

Table 2.3 compares the results of It2 and Ron obtained from the following two groups: Group one consists of diodes with the three different geometries (Geometries 1, 2 and 3) but the same N+ diffusion area of 32 μm^2, and Group two consists of diodes with the three geometries but the same area of 48 μm^2. Clearly, It2 increases and Ron decreases with increasing N+ area for all three geometries. Under the same N+ area, Geometry 1 diode (single finger, large diode

width, and short cathode length) has the highest It2 and lowest Ron, whereas Geometry 3 diode (single finger, small diode width, and long cathode length) has the lowest It2 and highest Ron. The superior ESD performance of Geometry 1 diode can be attributed to the presence of 4 metal-2 layer lines, instead of 2 metal-2 layer lines in Geometries 2 and 3, in such a device. For diodes having the same number of metal-2 layer lines (i.e., Geometries 2 and 3 diodes), It2 increases and Ron decreases with increasing finger number.

Table 2.3: It2 and Ron of N+/P-well diodes having three different geometries but the same N+ area of 32 μm^2 (Group 1) and 48μm^2 (Group 2)

Geometry	W*Lc*N	Total area (μm^2)	It2 (A)	Ron (Ω)
1	20*1.6*1	32	1.77	2.65
2	10*1.6*2	32	1.66	2.97
3	10*3.2*1	32	1.37	3.4
1	30*1.6*1	48	2.59	1.82
2	10*1.6*3	48	1.95	2.55
3	10*4.8*1	48	1.76	3.21

2.6 Parasitic capacitance

The dual-diode structure with an effective power supply clamp between VDD and VSS is the most commonly used ESD protection scheme [51]-[53]. Usually, one P+/N-well junction diode is located between I/O pin and power rail VDD and another N+/P-well junction diode is placed between I/O pin and ground rail VSS. In this approach, diodes are operated in forward mode to provide low impedance discharge paths for ESD pulse and prevent the internal circuitry from being destroyed. During normal working operation, both two diodes are under reverse-biased condition and should be in off state. However, the parasitic capacitance associated with ESD diodes will introduce inevitable parasitic effects to the internal circuitry, such as RC delay,

substrate noise coupling, and impedance mismatch. Such ESD-induced parasitic effects seriously degrade the performance of the protected core circuit. This is particularly true for very high frequency applications. Thus, the low parasitic capacitance is another key consideration for designing of ESD protection diode.

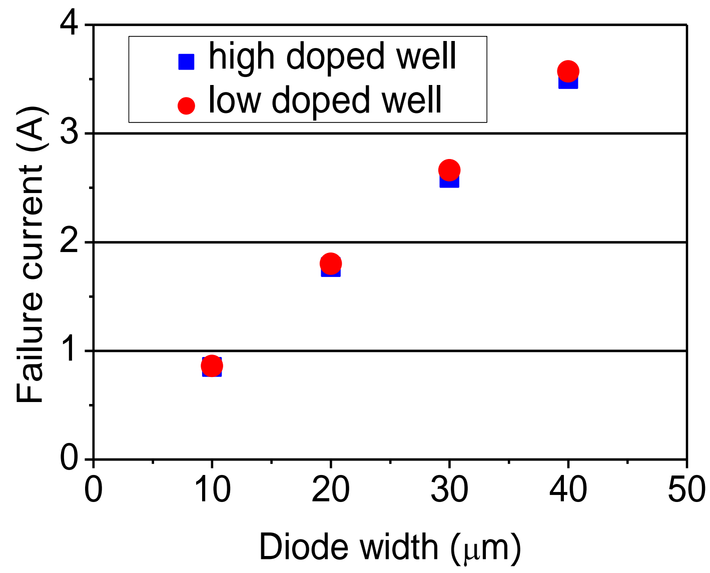
The parasitic capacitance of a reverse-biased diode is dominant by its depletion capacitance, which is defined by equation (2.1) [54]:

$$C_{dep}(V) = A_{eff} * [\frac{\varepsilon_0 \varepsilon_{Si} q N_A N_D}{2(N_A+N_D)(V_{bi}-V)}]^{\frac{1}{2}} \quad (2.1)$$

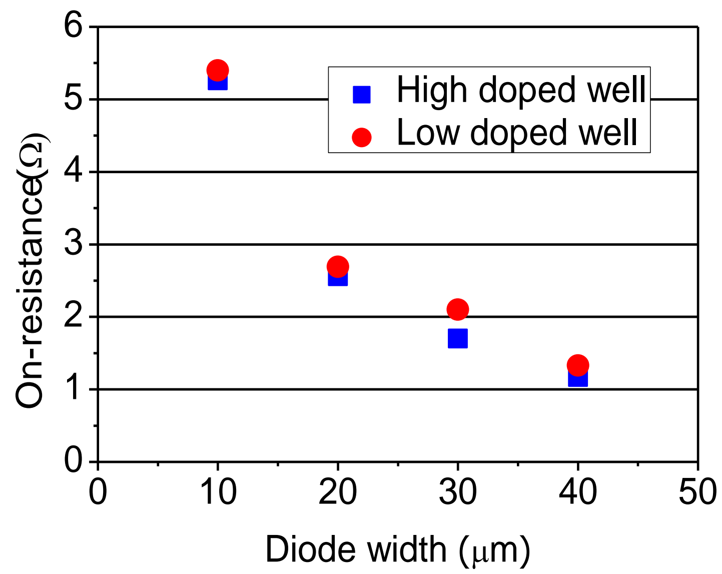
where $A_{eff}$is the effective area of PN junction, N_A and N_D are the doping concentration of anode and cathode regions, respectively. As shown in equation (2.1), the depletion capacitance of diode is the function of junction area, doping concentration and the voltage applied on the diode.

2.6.1 High/Low well doping concentration

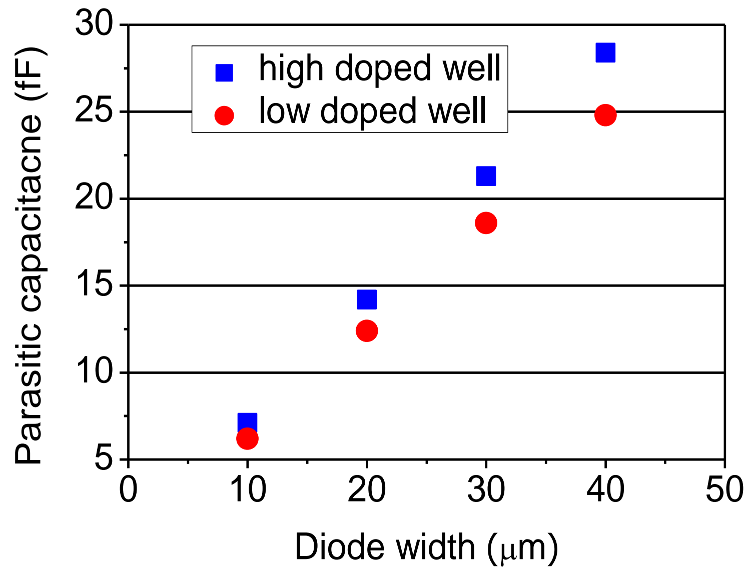
There are several ways to reduce diode's parasitic capacitance. One is reducing the junction area, this however will also decreases the ESD robustness of diode as shown in Table 2.3. Another way is reducing the junction doping concentrations. In the BiCMOS process, the availability of multiple implants and diffusion layers gives a degree of flexibility in choosing the junction configurations for low parasitic capacitance. Figures 2.16(a)-(c) compares the failure current It2, on-state resistance Ron and parasitic capacitance of diodes constructed using high and low-doped well layers. The width of diodes increase from 10 to 40 μm. Figures 2.16(a) and (b) show that It2 is almost unchanged and Ron is reduced slightly when using a high doped well layer. However, in such a case, the parasitic capacitance is increased notably, especially for a relatively large diode width W, as can be seen in Figure 2.16(c). This suggests that diodes fabricated using the low doped well are more promising for ESD applications.



(a)



(b)



(c)

Figure 2.16: (a) Failure current It2, (b) on-state resistance Ron, and (c) parasitic capacitance of N+/P-well LOCOS-bound diodes constructed using high and low doped well layers

2.6.2 Total capacitance

The flatness of total pad capacitance versus pad bias is another consideration. For the circuit with supply rail VDD powered up to 5 V and VSS rail being grounded, as the voltage at I/O pad increasing from 0 to 5 V, the voltage drop on the N+/P-well and P+/N-well junction diodes are 0 V ~ -5 V and -5 V ~ 0 V, respectively.

Figure 2.17 shows the parasitic capacitance of N+/P-well (left) and P+/N-well (right) diodes versus pad voltage. It is clear to see the capacitance of N+/P-well diode decreases, while on the other hand, the capacitance of P+/N-well diode increases with increasing of pad voltage from 0 V to 5 V. By adjusting the sizes of two diodes, good capacitance linearity versus pad bias

can be achieved for this dual-diode ESD protection structure because the compensation of parasitic capacitance between N+/P-well and P+/N-well diodes.

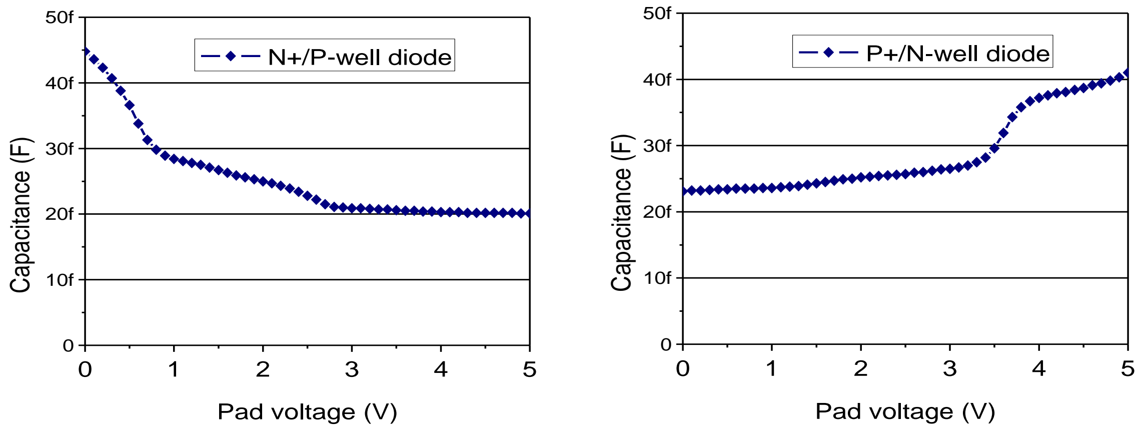


Figure 2.17: Capacitance of N+/P-well (left) and P+/N-well (right) diode vs. pad voltage

The total pad capacitance is the sum of parasitic capacitance for N+/P-well diode between I/O and VDD rail and P+/N-well diode between I/O and VSS rail. Figure 2.18 compares the total capacitance at the I/O pad using a pair of diodes with high or low doped well layer. The pair of high doping diodes has a maximum capacitance of 70 fF and minimum capacitance of 50 fF within a voltage range of 0 to 5 V. On the other hand, the pair of low doping diodes has a total capacitance varying between 30 and 40 fF. Thus, using a pair of low doping diodes is more beneficial from the perspective of lower and flatter total capacitance at the I/O pad.

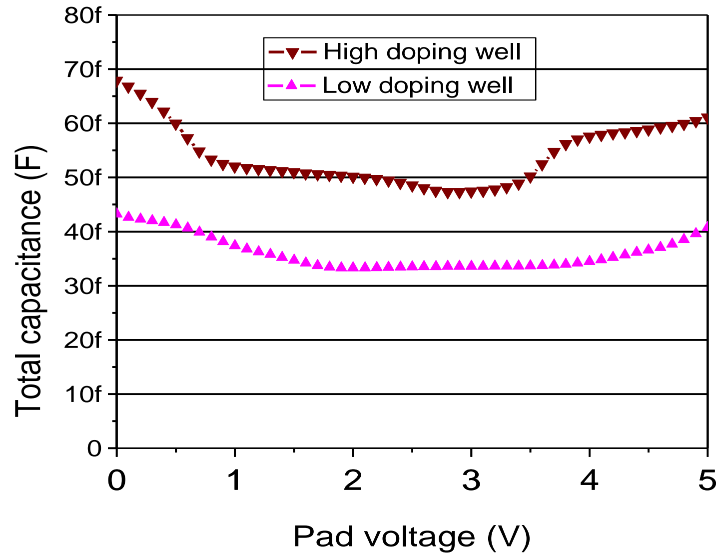


Figure 2.18: Total pad capacitance versus pad voltage using a pair of diodes with high or low well doping concentration

2.7 Summary

The effects of diffusion region's layout structure, metal connection pattern, dimension, geometry and junction configuration on the LOCOS-bound diode's ESD protection performance have been investigated experimentally using pulses generated by Barth 4002 transmission line pulsing (TLP) tester.

For diodes with the parallel metal connection, a smaller diode width and larger number of fingers give rise to higher failure current It2 and lower on-state resistance Ron. On the other hand, diodes with the crossing metal connection would work more effectively when a multiple-finger and/or multiple-metal line structure was used. To account for both the ESD robustness and lowest parasitic effect to the protected circuit, the diode having a stripe structure, crossing metal pattern, large device width, and low doped well layer yields the best overall ESD protection performance and lowest parasitic capacitance. The devices considered are N+/P-well junction

LOCOS-bound diodes having different device widths, lengths and finger numbers, but the approach applies generally to the P+/N-well junction diode as well. The results provide useful insights into optimizing the LOCOS-bound diode for robust HBM ESD protection applications.

CHAPTER 3. DESIGN OF POLYSILICON-BOUND DIODES FOR ROBUST ESD PROTECTION APPLICATIONS

As discussed in chapter 2, the junction diode is widely used in on-chip electrostatic discharge (ESD) protection applications because of its relatively simple structure and good performance. This is particularly true for ESD protection of low-voltage IC's where a relatively low trigger voltage for ESD protection device is required. Nonetheless, the ESD robustness of the diode is a major concern, which is usually defined after the on-state resistance Ron and failure current It2. Research works have demonstrated that different technologies for the isolation between the diode's anode and cathode regions can play an important role on the diode's ESD robustness. These technologies include the shallow trench isolation (STI-bound), LOCOS oxide (LOCOS-bound), and polysilicon gate (polysilicon-bound) [55]-[56]. It has been reported that, for ESD protection purposes, diodes with STI are inferior to those with other isolations [57]-[58].

In this chapter, we will first study and compare the ESD performances of the LOCOS- and polysilicon-bound diodes fabricated in a BiCMOS technology. The better performed device will then be investigated in more details in an effort to identify an optimal diode structure for robust ESD protection applications.

In 1998, the first polysilicon gated diode was developed by Voldman et al. in bulk CMOS technology for ESD protection [57]. Figure 3.1 shows the cross section of an N+/P-well junction polysilicon-bound diode, where the polysilicon gate (with a length L_{gate}) separates the diode's anode and cathode region. The La and Lc are the length of anode and cathode diffusion regions, respectively.

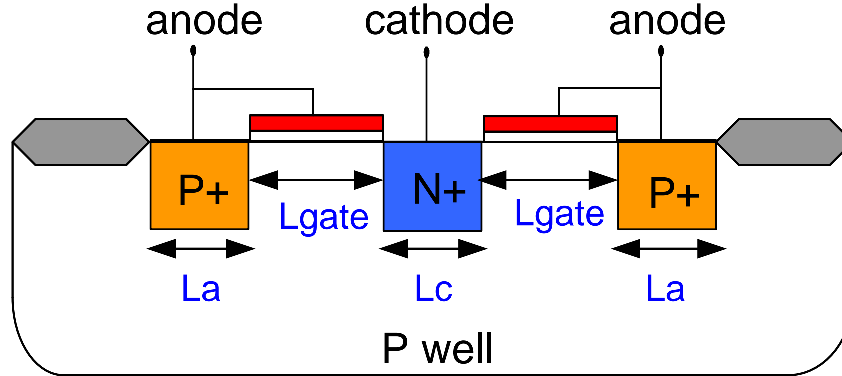


Figure 3.1: Cross section of N+/P-well polysilicon-bound diode

The critical ESD figures of merit, failure current It2 and on-state resistance Ron, of the diodes depend on various factors including the diode's dimension, geometry, junction configuration, and metal pattern [42], [59]. For the diode structure considered having two anode regions and one cathode region (see Figure 3.1), it had been found that the anode length La plays a marginal role on the diode's ESD performance [59]. Moreover, for the issue of metal topology, the crossing pattern was found to be the best metal layout for the diode's ESD robustness [59]. As such, we will in the following not account for the effect of La and will consider only diodes using the crossing metal pattern. Furthermore, unless noted otherwise, all measurements will be performance using pulses generated from the Barth 4002 transmission line pulsing (TLP) tester with a pulse width of 100 ns and a rise time of 10 ns, a stress condition equivalent to a well-known ESD event called the human body model (HBM).

3.1 Comparison of LOCOS- and Polysilicon-bound diodes

Figure 3.2 compares the I-V characteristics of N+/P-well and P+/N-well LOCOS- and poly-bound diodes with the same dimension and metal connection pattern. The anode length La and cathode length Lc are both 1.6 μm. The diode width W, or the width of anode/cathode region,

is 40 μm. The anode to cathode distance (i.e., isolation length) for both diode types is 2 μm. It can be seen the poly-bound diodes have higher failure current It2 (i.e., the currents at which the I-V curves ended in Figure 3.2) than that of the LOCOS-bound diode for both the N+/P-well and P+/N-well junction configurations (i.e., 4.3 vs. 3.7 A for P+/N-well and 3.9 vs. 3.4 for N+/P-well). As such, the poly-bound diode possesses a better ESD current carrying capability than the LOCOS-bound diode. The lower It2 in the LOCOS-bound diode is due mainly to the higher current density induced in the bird beak region.

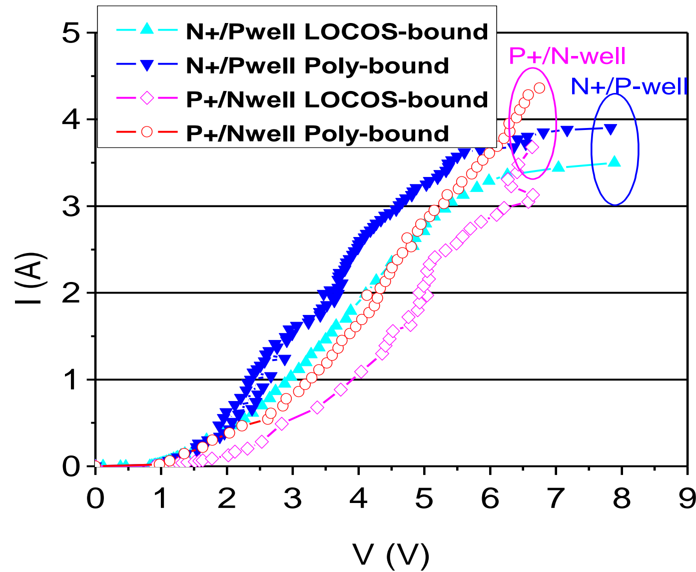


Figure 3.2: I-V characteristics of LOCOS- and poly-bound diodes

In addition to It2, the voltage drop or voltage clamping on a diode is also important to robust ESD applications, and a good voltage clamping capability (i.e., producing a low voltage drop) is needed to minimize the possibility of ESD induced core circuit damage. Such a capability is directly related to the on-state resistance Ron of the diode, since a lower on-state resistance leads to a smaller voltage drop after the diode is triggered by an ESD event. For the LOCOS-bound diode, the current between the anode and cathode must pass underneath the

curved LOCOS oxide. For the poly-bound diode, on the other hand, since the polysilicon gate is flat and not penetrating into the silicon, the current flows straight between the anode and cathode. As a result, the current path for the poly-bound diode is shorter compared to that for the LOCOS-bound diode, and hence a smaller on-state resistance for the poly-bound diode. This reasoning is consistent with Ron values given in Table 3.1 extracted from the TLP I-V curves in Figure 3.2. Clearly, the poly-bound diode shows a better voltage clamping capability than the LOCOS-bound diode for both the N+/P-well and P+/N-well junction configurations.

Table 3.1: On-state resistance Ron of LOCOS- and poly-bound diodes

Isolation	N+/P-well junction diode	P+/N-well junction diode
LOCOS-bound	1.25 Ω	1.4 Ω
Polysilicon-bound	1.02 Ω	1.21 Ω

TCAD simulation was also carried out to provide physical insights of the two different diodes. Figure 3.3 shows the current density contours of the N+/P-well LOCOS- and poly-bound diodes under the forward operation condition. Note that the hot spot (i.e., region of the highest current density) of the two devices is located near the cathode region. For the LOCOS-bound diode, the hot spot at the interface between the LOCOS oxide and N+ diffusion region has a current density of $6.8 * 10^6 A/cm^2$, which will also be the place most likely to fail under the ESD stress. For the poly-bound diode, on the other hand, because of the absence of the LOCOS oxide, the current distribution is more uniform with the highest current density being $5.56 * 10^6 A/cm^2$. These simulation results are consistent with data given in Figure 3.2 indicating that the poly-bound diode is more robust than the LOCOS-bound diode. The ESD robustness of the poly-bound diode will be analyzed in details below.

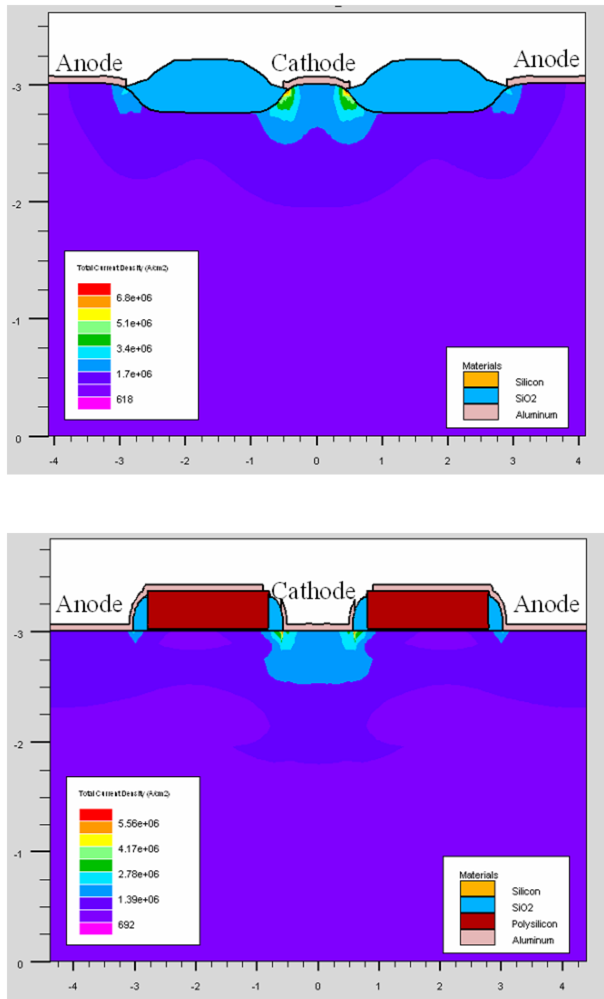


Figure 3.3: Simulated current density contours for LOCOS- (top) and poly-bound (bottom) diodes under the same forward ESD condition

For a fast ESD transient event such as the charged device model (CDM), the diode's turn-on speed becomes another key consideration. Figure 3.4 shows the voltage vs. time waveforms of the N+/P-well and P+/N-well LOCOS- and poly-bound diodes subject to a very-fast TLP pulse with a 100 ps rise time, 2 ns duration and 15 V amplitude. The device's turn-on speed can be characterized from such a transient as the time it takes from the point where the voltage peaks to the point where the voltage becomes relatively constant. Clearly, for both the N+/P-well and P+/N-well junction configurations, the poly-bound possesses a faster turn-on speed than the LOCOS-bound diode. This stems mainly from the fact that the voltage overshoot is less

prominent in the poly-bound diode [60]. The further study to understand the physical mechanism underlying this phenomenon will be addressed in detail in next chapter.

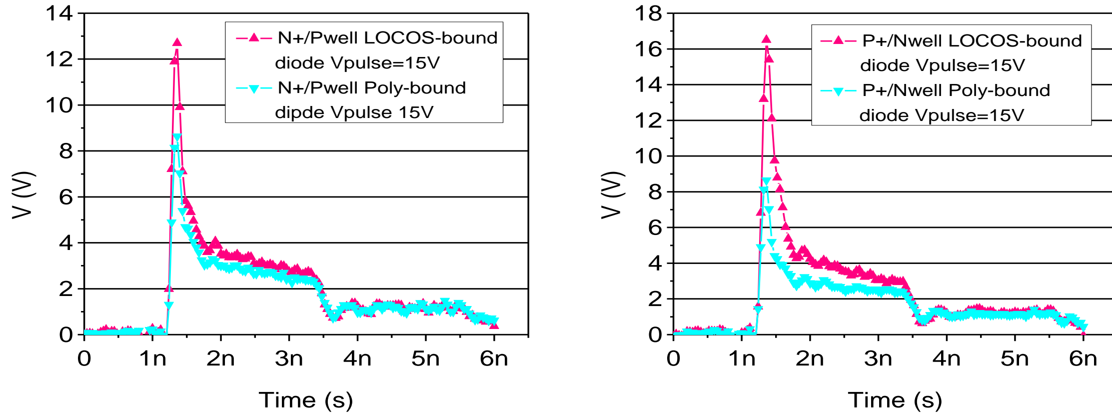


Figure 3.4: Transient voltage waveforms for N+/P-well (left) and P+/N-well (right) junction LOCOS- and poly-bound diodes subject to a very-fast TLP pulse with a 2 ns duration and 15 V amplitude

3.2 Optimization of poly-bound diode

The preceding analysis has illustrated clearly that the poly-bound diode is superior to the LOCOS-bound diode for ESD protection applications. In an effort for designing an optimal ESD diode, we will in the section investigate the factors that can influence the ESD robustness of the poly-bound diode. The optimization will be focused on the failure current and on-state resistance of the N+/P-well structure, but the approach applies generally to the P+/N-well diodes as well. Different device parameters will be varied and their effects on the poly-bound diode's ESD performance will be studied based on the TLP experimental data. In changing the parameters, a typical nominal value will first be selected, and an increment of about 50% of the nominal value will be used.

3.2.1 Diode width

The first consideration is the diode width (i.e., width of anode/cathode) W, which can influence considerably the poly-bound diode's failure current It2 and on-state resistance Ron. Figure 3.5 shows the I-V characteristics of N+/P-well poly-bound diode with anode length La = 1.6 μm, cathode length Lc = 1.6 μm, polysilicon gate length L_{gate} = 2 μm, and different diode width W of 20, 30 and 40 μm (i.e., 20 is the nominal value and increment is 50% of the nominal). It is expected that increasing W will increase It2 and decrease Ron due to the enlarged device size. This is indeed the case, as evidenced from the trends demonstrated in Figure 3.6.

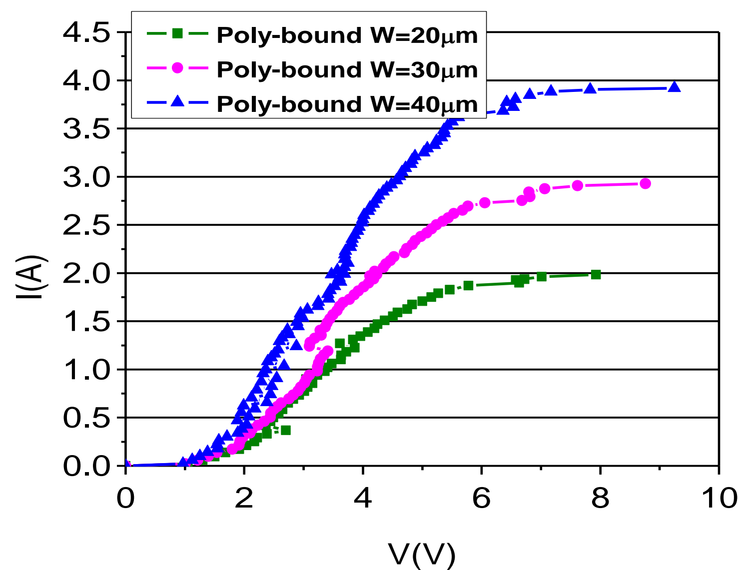


Figure 3.5: I-V characteristics of N+/P-well poly-bound diodes having different widths

It can be seen the failure current It2 increases linearly with increasing diode width (i.e., It2 are 1.98, 2.93, and 3.92 A, respectively) and the on-state resistance Ron decreases with increasing W. However, the drawback of increasing diode width W is the increased diode's size and associated parasitic effects, which will be accounted for later.

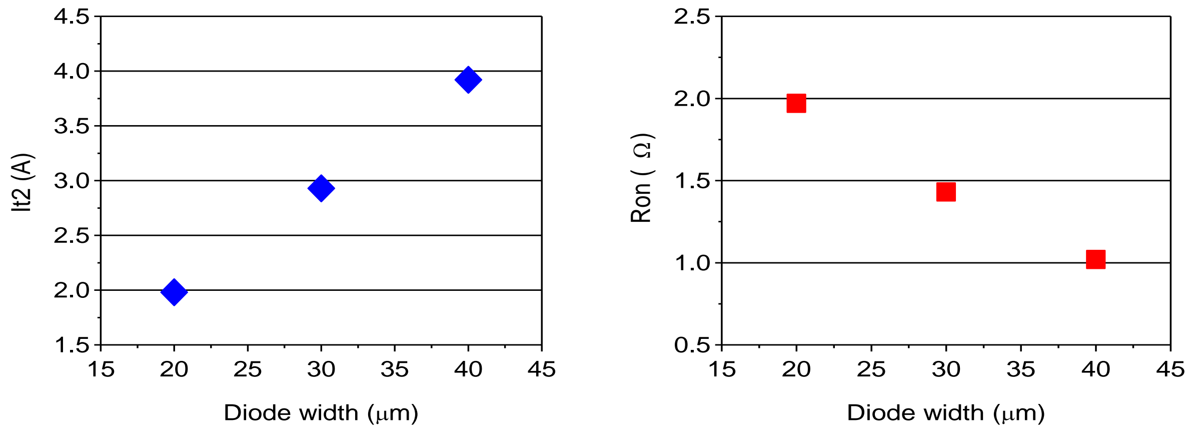


Figure 3.6: Failure current It2 (left) and on-state resistance Ron (right) of N+/P-well poly-bound diode having different widths

3.2.2 Finger number

The ESD robustness is also a function of the number of anode/cathode fingers. Figure 3.7 shows the I-V characteristics of poly-bound diodes having the same diode width of 40 μm but three different finger numbers. Diode 3 and 1 have the highest and lowest It2 and the smallest and largest Ron, respectively, indicating that increasing the finger number offers an appealing means in enhancing the poly-bound diode's ESD robustness. Nonetheless, when the total area is fixed and the finger number is increased (i.e., the diode width is reduced with increasing finger number), we have found that the diode actually becomes less robust due to the fact that the maximum metal width allowed on each finger is inversely proportional to the finger number.

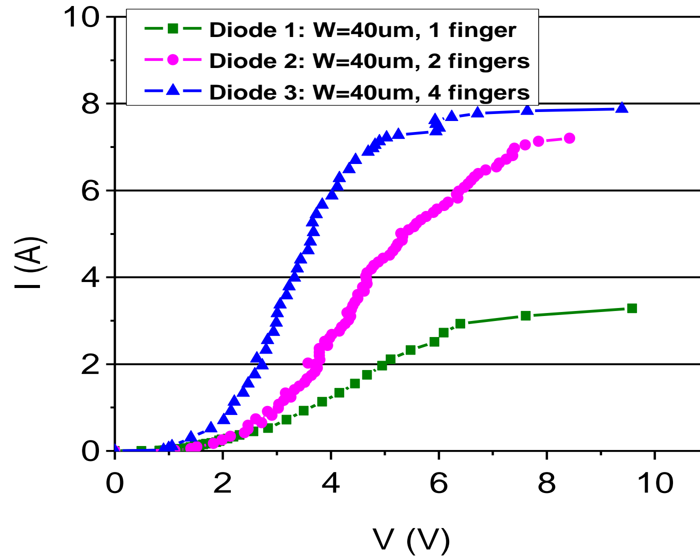


Figure 3.7: I-V characteristics of N+/P-well poly-bound diodes having different finger numbers

3.2.3 Cathode length

Changing the cathode length Lc can also affect notably the ESD performance of the poly-bound diode. Figure 3.8 shows that the failure current It2 increases from 2 to 3 A when Lc increases from 1.6 to 3.8 μm. The on-state resistance Ron decreases with increasing Lc, as can also be seen in the Figure 3.8. The improved ESD robustness stems from the fact that increasing the cathode length gives rise to a reduced current density and thus a lower temperature in the region. The down side of increasing Lc is of course an increased device size and increased parasitic capacitance. These effects will be discussed later.

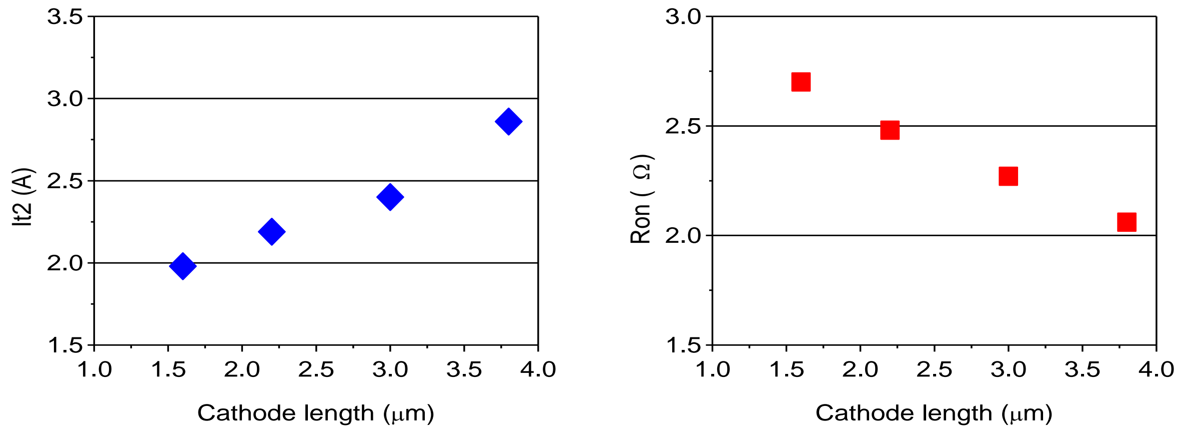


Figure 3.8: Failure current It2 (left) and on-state resistance Ron (right) of N+/P-well poly-bound diodes with different cathode lengths

3.2.4 Polysilicon gate length

Next we consider the effect of polysilicon gate length L_{gate}. Figure 3.9 shows the I-V curves of N+/P-well poly-bound diodes with polysilicon length L_{gate} increasing from 2 to 7 μm. It can be seen that the failure current It2 is almost unchanged for the different L_{gate} values. On the other hand, the larger polysilicon length gives rise to a longer current path from the anode and cathode and thus results in a higher on-state resistance Ron, as evidenced from the data given in Figure 3.10. So the use of a relatively small L_{gate} seems to be advantageous from the perspective of diode's voltage clamping capability.

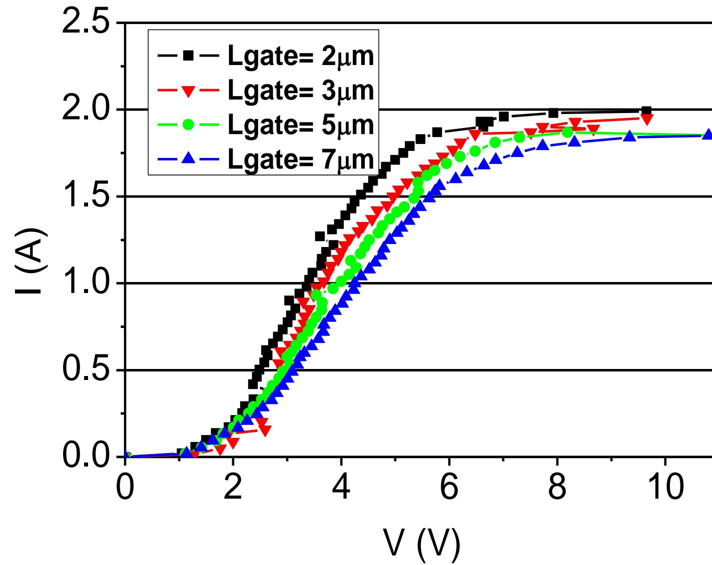


Figure 3.9: I-V characteristics of N+/P-well poly-bound diodes with different polysilicon gate lengths

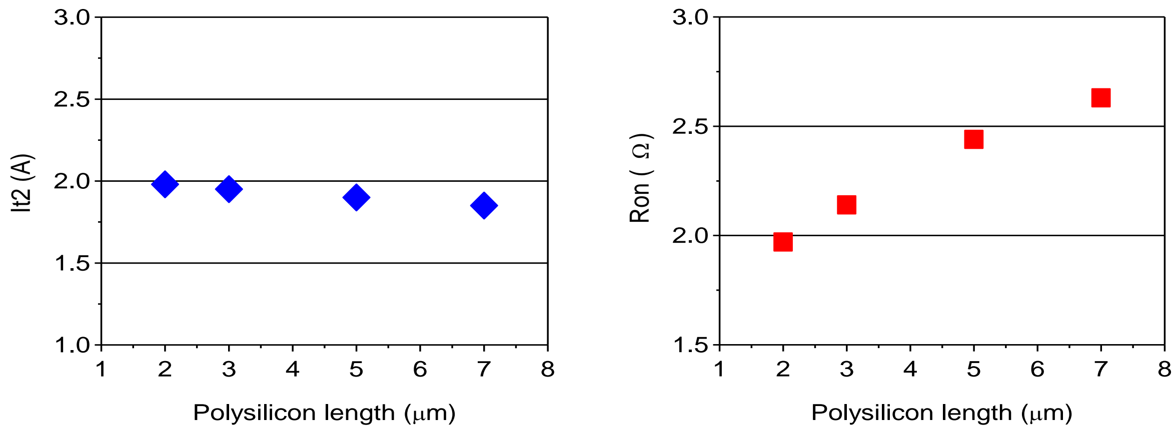


Figure 3.10: Failure current It2 (left) and on-state resistance Ron (right) of N+/P-well poly-bound diodes with different polysilicon gate lengths

However, the length of polysilicon gate cannot be reduced indefinitely and is subject to a minimal value as explained below. Table 3.2 shows the It2 results for different polysilicon lengths ranging from 1 to 7 μm. When the polysilicon lengths are higher than 2 μm, It2 increases slightly with decreasing L_{gate}. But when the polysilicon length reduces further from 2 to 1 μm,

It2 is decreased by 30%. This It2 reduction stems from the metal failure, as the maximum width of metal layer above the N+ cathode region is mandated by the layout design rule. Having a very small L_{gate} reduces the metal width, increases the current density in the metal, and consequently decreases It2. Junction punch-through is another factor limiting how small L_{gate} can be implemented. So, it can be concluded that the use of $L_{gate} < 2$ µm should be excluded from the design consideration.

Table 3.2: Failure current It2 of poly-bound diodes with different polysilicon gate lengths

L_{gate}	1 µm	2 µm	3 µm	5 µm	7 µm
It2	1.37 A	1.98 A	1.95 A	1.90 A	1.85 A

As illustrated, changing the above-mentioned design parameters, i.e., the diode width W, cathode length Lc, polysilicon gate length L_{gate}, and finger number, can influence considerably the poly-bound diode's It2 and Ron. Moreover, these changes also alter the device size and capacitance, two other important criterions related to the ESD device's compactness and parasitics. Table 3.3 shows the capacitances of the poly-bound diodes with different design parameters. It should be pointed out that the capacitance is a function of not just the device size, but also the junction perimeter length.

Table 3.3: Parasitic capacitances of poly-bound diodes having different design parameters

Diode width W (µm)	20	30	40	-
Capacitance (fF)	38.72	58.08	77.44	-
Cathode length Lc (µm)	1.6	2.2	3.0	3.8
Capacitance (fF)	38.72	47.4	58.92	70.22
Polysilicon length Lgate (µm)	2	3	5	7

Capacitance (fF)	38.72	43	51.54	60.08
Finger numbers	1	2	4	-
Capacitance (fF)	38.72	77.8	155.9	-

3.3 Figures of merit for It2 and Ron

To account for the effects of changing these design parameters on the ESD robustness, device size, and capacitance of the poly-bound diode in a more unified manner, we define the following two figures of merit (FOM) for It2 and Ron for the purpose of determining quantitatively how much ESD robustness is enhanced vs. an increased design parameter:

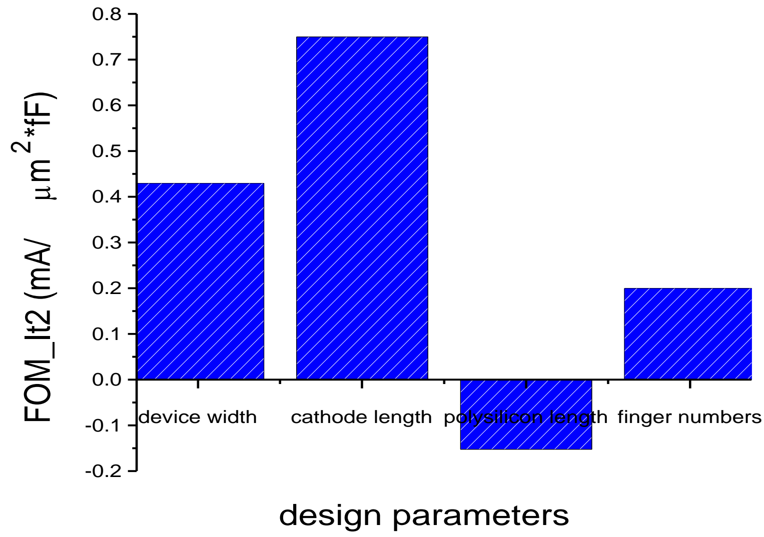
$$FOM_It2 = \frac{\Delta It2}{\Delta device_size * \Delta cap} \tag{3.1}$$

$$FOM_Ron = \frac{\Delta Ron}{\Delta device_size * \Delta cap} \tag{3.2}$$

where $\Delta It2$, ΔRon, $\Delta device_size$, and Δcap are increase of It2, Ron, diode size, and parasitic capacitance, respectively, due to the increase of a specific design parameter. These two FOMs can more effectively reflect the ESD robustness of the diode than It2 and Ron alone. The more positive the FOM_It2 and the more negative the FOM_Ron (i.e., Ron decreases with increasing design parameter), the more suitable is increasing the particular design parameter for ESD applications. Conversely, the more negative the FOM_It2 and the more positive the FOM_Ron, the more beneficial is decreasing the particular design parameter.

Figure 3.11 compares FOM_It2 and FOM_Ron values obtained for the four different design parameters considered. The results suggest that increasing the cathode length is the best way to enhance the diode's ESD robustness, followed by the diode width increase and finger

number increase. On the other hand, decreasing the polysilicon length is advantageous from the viewpoint of ESD diode optimization.



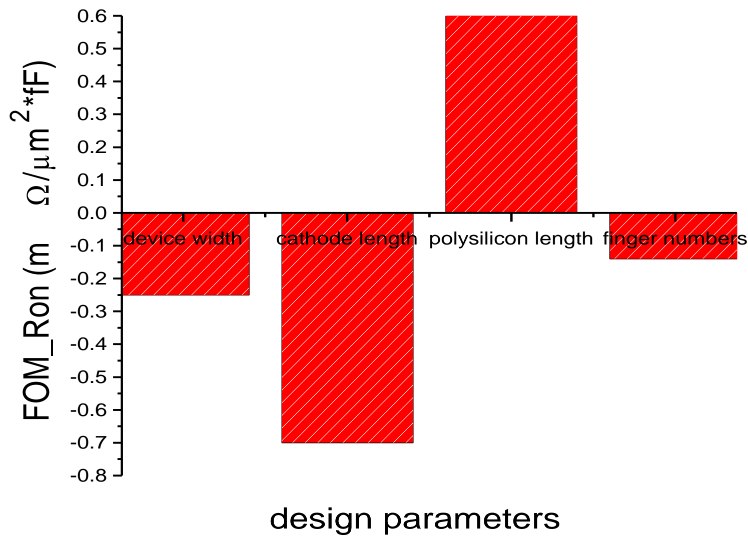


Figure 3.11: Figures of merit for It2 (top) and Ron (bottom) obtained for the four different design parameters

3.4 Gate connection and metal topology

Two more design parameters can affect the diode's ESD performance, but changing these parameters does not vary the device size and alters the capacitance only minimally. As such, these two parameters were not considered in the above-mentioned FOM_It2 and FOM_Ron.

3.4.1 Gate terminal connections

The first consideration is the different ways in which the polysilicon gate can be connected. The three possible ways are gate-to-anode, gate-to-cathode, and gate-floating [48]. Figure 3.12 shows the I-V characteristics of the poly-bound diode having the three different terminal connections and two different device widths of 20 and 40 μm. As can be seen in the figure, It2 is insensitive to the types of terminal connection for both the diode widths considered. However, allowing the polysilicon gate to float will be of a concern for the issue of gate potential uncertainty. For the case of polysilicon connecting to cathode, a risk of gate oxide breakdown can occur if a sufficiently high voltage is built between the polysilicon and P-well region. Thus the best connection is to tie the polysilicon gate to the P+ anode.

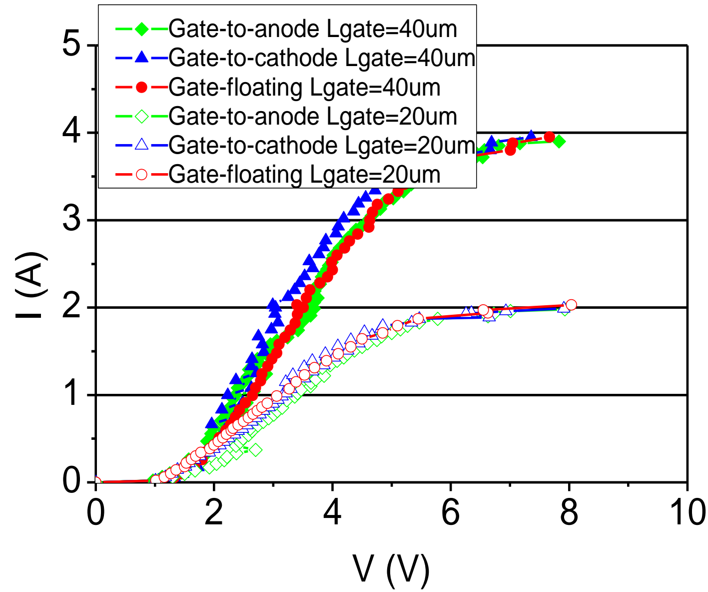


Figure 3.12: I-V characteristics of poly-bound diodes with gate-to-anode, gate-to-cathode, and gate-floating connections

3.4.2 Metal topologies

Lastly, we examine the effect of metal topology on the diode's ESD performance. Figure 3.13 shows N+/P-well poly-bound diodes having the same area but five different metal topologies using the crossing pattern. In the figure, the light purple color denotes the level-1 metal M1 placed on the diode's diffusion regions, and the light green color denotes the level-2 metal M2 connected to the vias. For example, Diode_A1C1 has 1 M2 line connected to the anode and 1 M2 line to the cathode. On the other hand, Diode_A4C4 has 4 M2 lines connected to the anode and 4 M2 lines to the cathode. The widths of each M2 line in Diode_A1C1 and in Diode_A4C4 are the widest and narrowest, respectively, among the five cases considered. Table 3.4 compares It2 and on-state resistance Ron obtained for the five different metal topologies. Diode_A4C4 has the highest It2 since its current flow can utilize the most inward and outward paths. The on-state resistance does not benefit from having a large number of metal lines,

however, and Diode_A2C2 exhibits the smallest Ron among the 5 different topologies. Overall, the topologies Diode_A2C2 and Diode_A3C3 seem to offer the best ESD performance.

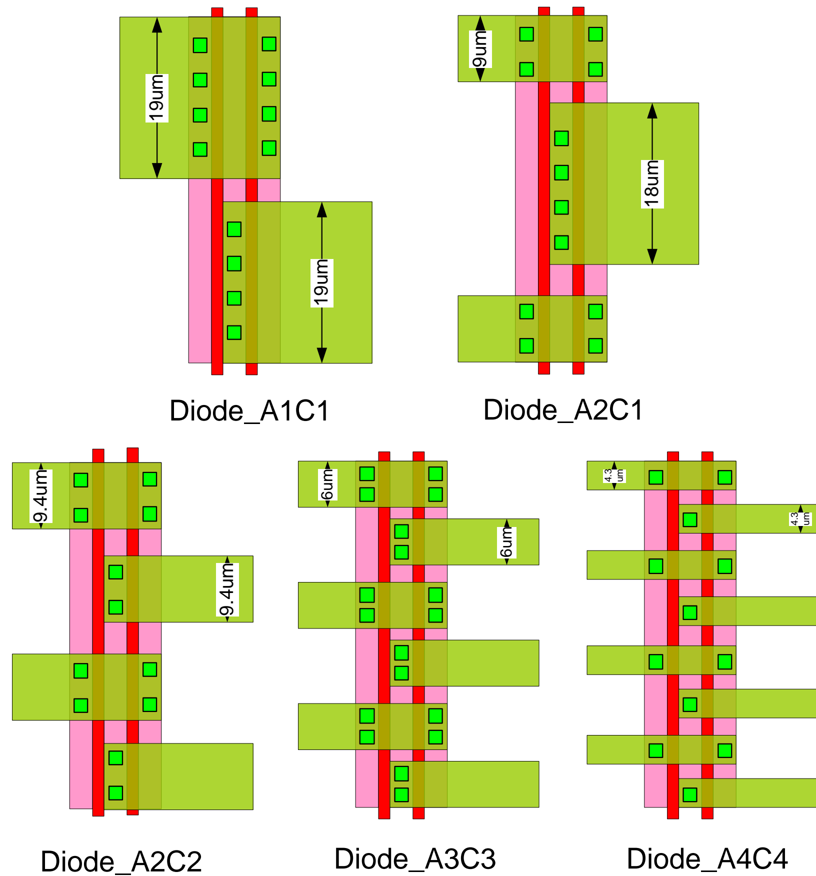


Figure 3.13: Poly-bound diodes having the same area but five different crossing metal topologies

Table 3.4: It2 and Ron of poly-bound diodes having the different metal topologies shown in Figure 3.13

	Diode_A1C1	Didoe_A2C1	Diode_A2C2	Diode_A3C3	Diode_A4C4
It2 (A)	3.05	3.52	3.49	3.55	3.56
Ron (Ω)	1.29	1.57	1.16	1.19	1.27

3.5 Summary

In this chapter, ESD robustness of the LOCOS- and polysilicon-bound diodes were first studied and compared based on TCAD simulation and experimental measurement results. Then

the better performed polysilicon-bound diode was investigated in more details in order to come up with an optimal diode structure for robust ESD protection applications.

Specially, the effects of the diode width, cathode length, finger number, polysilicon gate length, terminal connection, and metal topology on the diode's failure current and on-state resistance were considered. Two figures of merits were also developed to better judge the effects of these parameters on the overall diode's ESD performance. Our study suggested that a polysilicon-bound diode with a relatively large cathode length, relatively large diode width, relatively large number of fingers, relatively small polysilicon gate length, poly-to-anode terminal connection, and metal topology having 2 or 3 anode/cathode metal lines would be an excellent candidate for constructing effective HBM ESD protection solutions for low-voltage integrated circuits.

CHAPTER 4. EVALUATION OF TRANSIENT BEHAVIOR OF DIODES FOR FAST ESD APPLICATIONS

4.1 Introduction

Human body model (HBM) is a mature, well-understood electrostatic discharge (ESD) event for simulating charge transfer from a person's finger to an electric component. However, recently industry data indicates the HBM rarely simulates real-world ESD failures. For example, latest generation package styles such as mBGAs, SOTs, SC70s, & CSPs with millimeter-range dimensions are often effectively too small for people to handle with fingers. On the other hand, the charged device model (CDM) ESD event becomes increasingly important in today's manufacturing environment and packaging technology [61]-[63]. This event generates highly destructive pulses with a very short rise time and very small duration [64].

Transmission line pulsing (TLP) measurement is a very effective tool for evaluating the ESD robustness of a circuit or single element. This is particularly helpful in characterizing the effect of HBM stresses where the ESD-induced damages are more likely due to the thermal failures. TLP has been modified to probe CDM protection effectiveness [65]-[68]. The pulse width was reduced to the range of the 1-10 ns to mimic the very fast transient of the CDM pulses. Such a very fast TLP (VFTLP) testing has been used frequently for CDM ESD characterization.

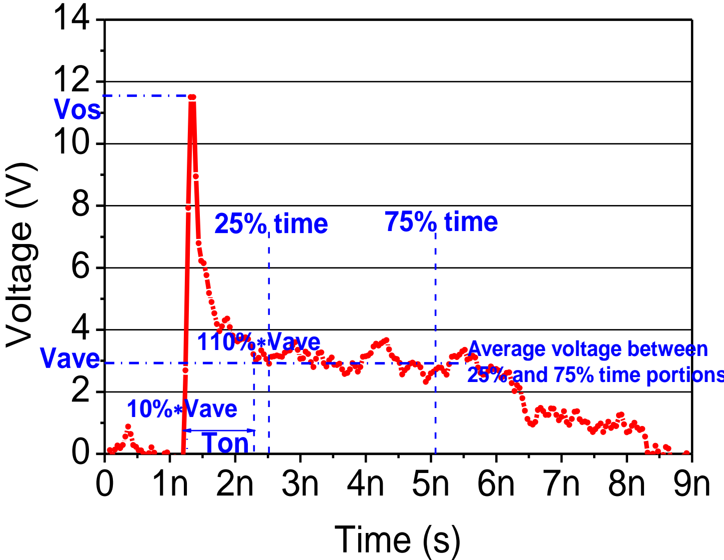
A commonly asked question is as to how closely the VFTLP characterization resembles CDM event. Due to the completely different current and time domains, the CDM testing does not correlate well with the HBM and thus the TLP testing, but the VFTLP technique satisfies these requirements [64], [69]. Specifically, the VFTLP with a rise time of 100 ps offers an attractive means to extract the CDM time domain parameters [70]. The exact VFTLP and CDM correlation, however, is difficult to establish and not yet available in the literature due to the fact that the

CDM testing is strongly influenced by the types of package used, an effect not accounted for in the VFTLP testing.

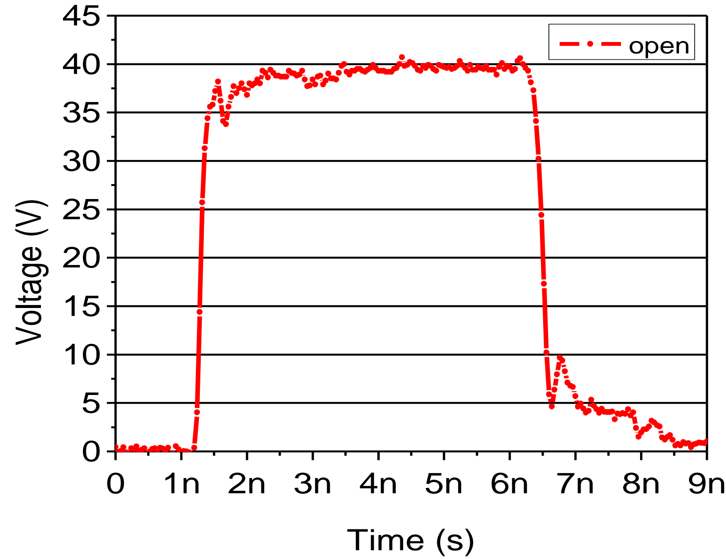
In this chapter, the transient behaviors of the ESD protection devices subject to the VFTLP stress will be studied and evaluated in details. Measurements will be carried out based on pulses generated by the Barth 4012 VFTLP tester.

4.2 Definition of overshoot voltage and turn-on time

The overshoot voltage and turn-on time are two key considerations for designing the CDM ESD protection devices. A relatively high overshoot voltage can cause failure of the protection devices as well as the protected devices, and a relatively long turn-on time may not switch on the protection device fast enough to effectively protect the core circuit against the CDM stress. The overshoot voltage and turn-on time of an ESD protection device can be observed and extracted from the voltage vs. time waveforms measured from the VFTLP testing.



(a)



(b)

Figure 4.1: Transient voltage waveform of (a) an ESD protection device and (b) an open apparatus subject to the VFTLP stress

A Barth Model 4012 system was used for the VFTLP testing and characterization. Figure 4.1(a) shows the time-dependent voltage waveform of an ESD protection device subject to a VFTLP pulse with a 5-ns duration (from 1.25 to 6.25 ns as shown in Figure 4.1(a)) and 100-ps rise time. Initially, the voltage on the device increases quickly to reach a peak value, which is defined as the overshoot voltage Vos, then the voltage decades exponentially and settles at a noisy but relatively constant value. An asymptote can be constructed using a linear regression for the relatively constant value [71]. However, it is not easy to obtain the linear regression accurately due to the noise in the region. Here, we create such an asymptote using a constant voltage Vave calculated by averaging the voltages between the 25% and 75% time portions of the voltage waveform (from 2.5 to 5 ns as shown in Figure 4.1(a)). The 10% Vave point is the point where the voltage increases to 10% of Vave from the start point. The 110% Vave point is the point where the voltage decreases to 110% of Vave after reaching the peak point. The turn-on

time Ton of the ESD protection device is defined as the time it takes to go from 10% Vave point to 110% Vave point. The voltage vs. time waveform of an open apparatus subject to the same VFTLP pulse is given in Figure 4.1(b) to demonstrate that the voltage overshoot observed in Figure 4.1(a) is not a result of the parasitics associated with the probes and cables.

4.3 Effect of stressed pulse

Figure 4.2 shows the cross-section view of the N+/P-well poly-bound diode considered in this study, where the Ld is the diffusion length, W is the diode width (in the third dimension, not shown in Figure 4.2), and the Lg is the poly-gate length. The devices were fabricated in a 0.6-μm BiCMOS process. In the ESD testing, the cathode and anode are connected to the VFTLP ground and signal probes, respectively.

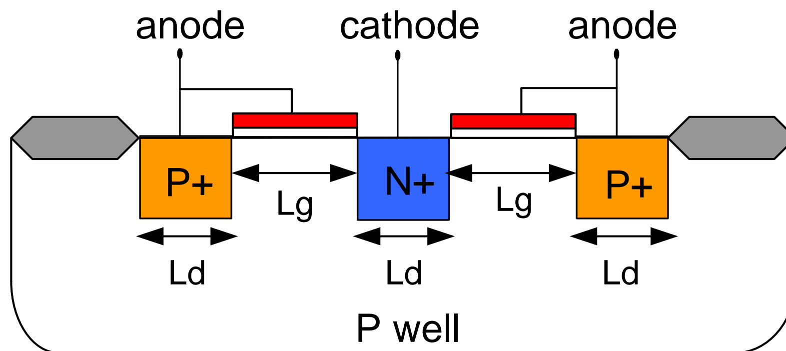
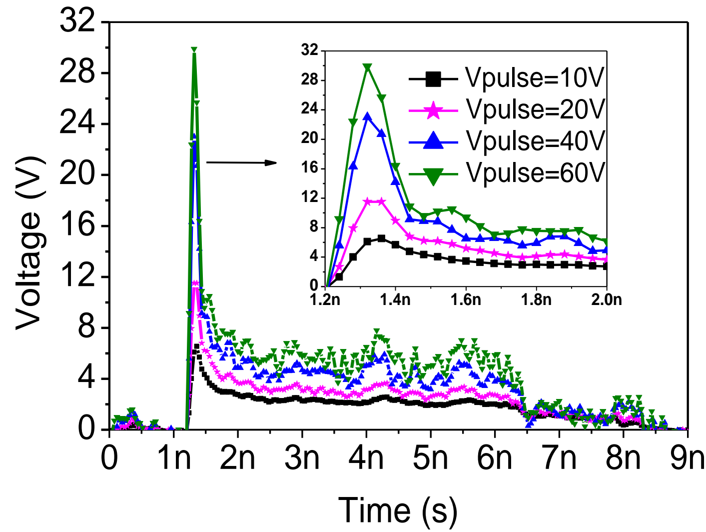


Figure 4.2: Cross-section view of N+/P-well poly-bound diode

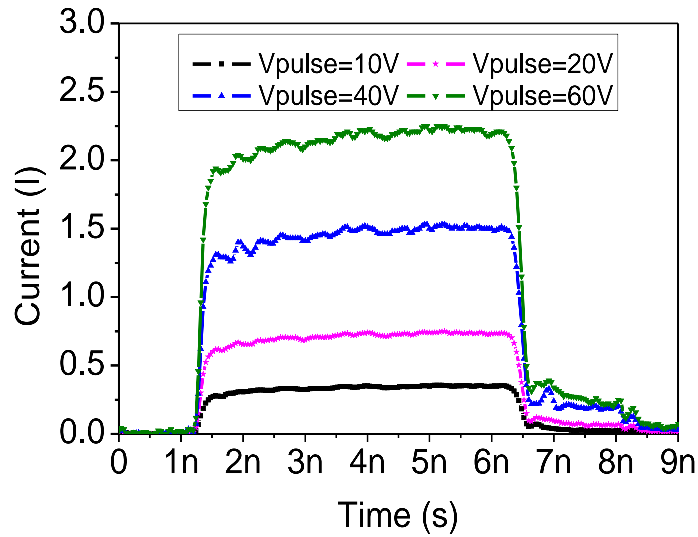
4.3.1 Pulse amplitude

Figure 4.3(a) and (b) shows the voltage and current waveforms, respectively, of an N+/P-well poly-bound diode with Ld = 1.6 μm, Lg = 2 μm, W = 20 μm, and one anode/cathode finger subject to VFTLP voltage pulses with a 5-ns duration, a 100-ps rise time and amplitudes ranging from 10 to 60 V. The corresponding overshoot voltage and turn-on time vs. pulse amplitude (i.e., pulse voltage) of the poly-bound diode are given in Figure 4.4. It can be seen the diode's

overshoot voltage increases roughly linearly with increasing pulse amplitude. On the other hand, the turn-on time is relatively constant versus the pulse voltage, except for a small drop taking place at a voltage of 50 V.



(a)



(b)

Figure 4.3: (a) Voltage waveforms and (b) current waveforms of N+/P-well poly-bound diode stressed with VFTLP pulses having different voltage amplitudes

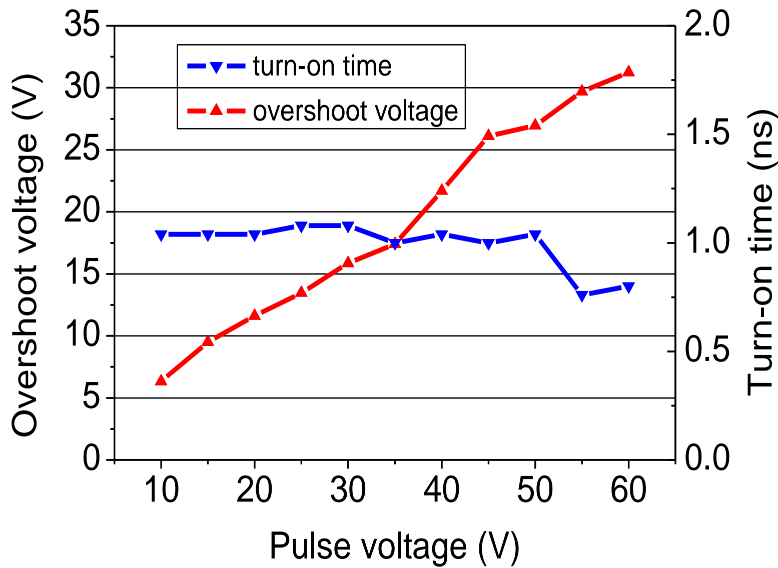


Figure 4.4: Overshoot voltage and turn-on time of N+/P-well poly-bound diode vs. pulse amplitude

4.3.2 Pulse rise time

Figure 4.5 shows the voltage waveforms of the N+/P-well poly-bound diode subject to voltage pulses with a 5-ns duration, a 20-V amplitude, and different pulse rise times of 100, 200, and 400 ps. For the case of a longer rise time, the diode exhibits a lower overshoot voltage but wider overshoot regime. This is because, as the pulse rise time is increased, the minority free-carriers (electrons) have more time to recombine with the majority free-carriers (holes) in the P-well region, thus resulting in a slower conductivity modulation in the diode and the observed transient characteristics [60].

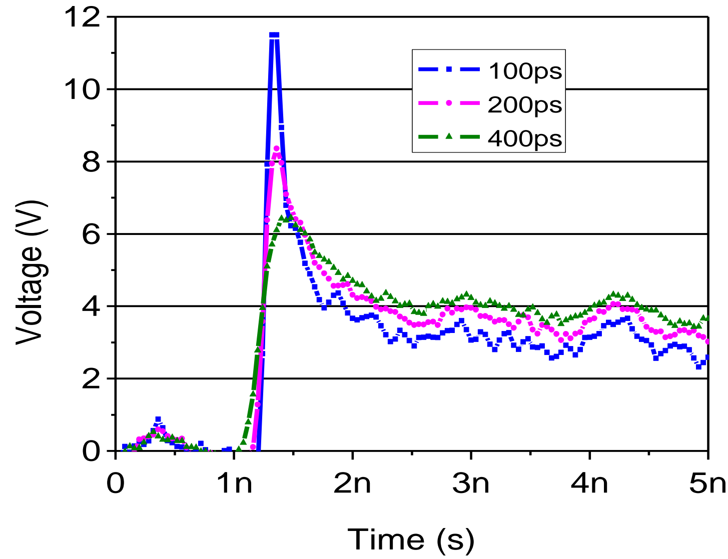
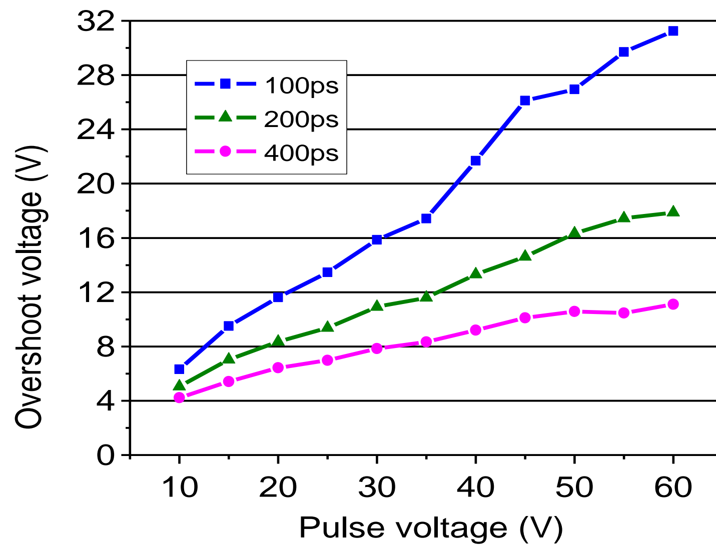
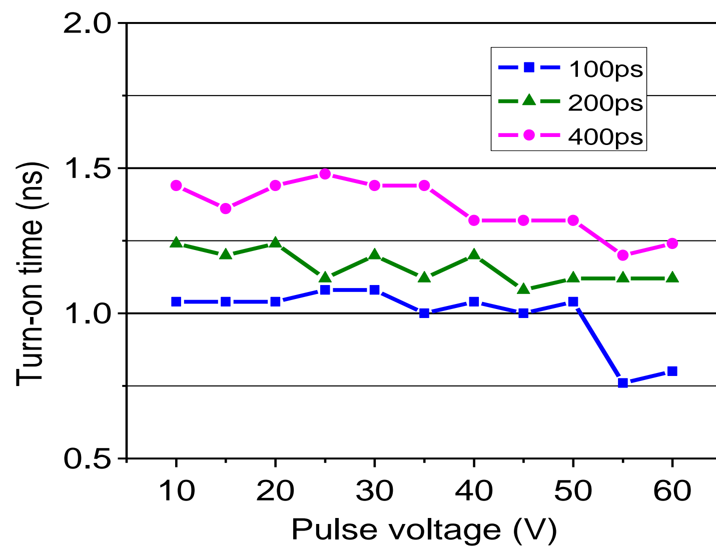


Figure 4.5: Voltage waveforms of N+/P-well poly-bound diode subject to pulses with different rise times

The overshoot voltage and turn-on time of poly-bound diode as functions of the pulse voltage and rise time are given in Figure 4.6(a)-(b). Of all three rise times considered, the overshoot voltage increases monotonically but the turn-on time is relatively insensitive with increasing pulse amplitude. The stress with the smallest rise time gives rise to the highest overshoot voltage but smallest turn-on time.



(a)



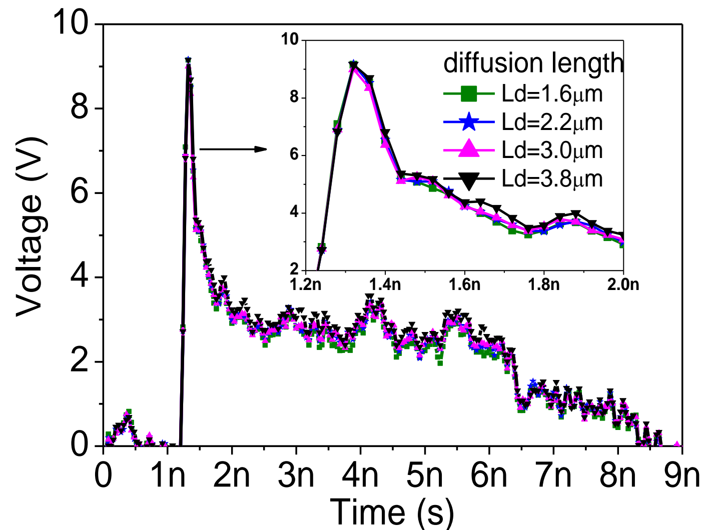
(b)

Figure 4.6: (a) Overshoot voltage and (b) turn-on time of N+/P-well poly-bound diode vs. pulse amplitude for 3 different pulse rise times

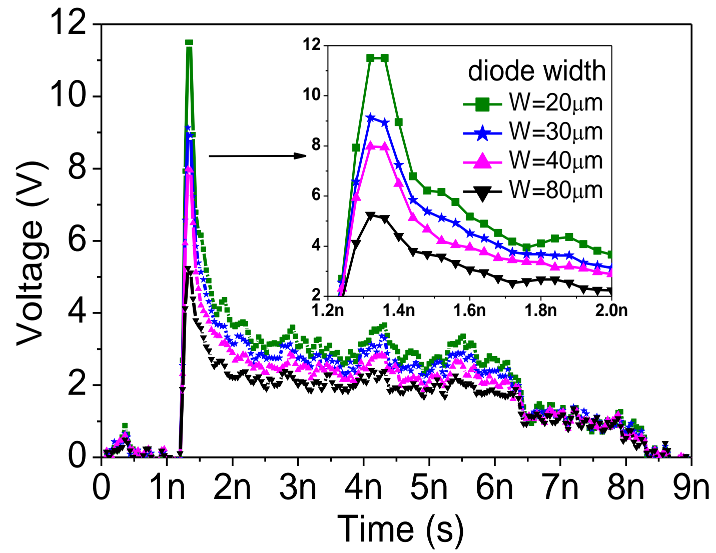
4.4 Effect of dimensions

In this section, we will study the effects of the poly-bound diode's dimensions on the overshoot voltage and turn-on time characteristics. VFTLP pulse having a 5-ns duration, 100-ps rise time, and 20-V magnitude will be used. The norm diode dimensions are Ld = 1.6 μm, Lg = 2 μm, W = 20 μm, and one anode/cathode finger. When changing one parameter, the other three parameters are kept the same.

Figure 4.7(a)-(d) shows the voltage waveforms of poly-bound diodes with different diffusion lengths, diode widths, finger numbers and poly-gate lengths. Clearly, changing Ld impacts minimally the diode's transient behavior under the fast transient event. For two other parameters, diode width W and finger number, a large parameter value yields a lower peak voltage and smaller sustain voltage Vave. But none is as obvious as the effect of Lg on the voltage waveforms, as altering Lg changes both the overshoot voltage and turn-on time considerably (see Figure 4.7(d)).



(a)



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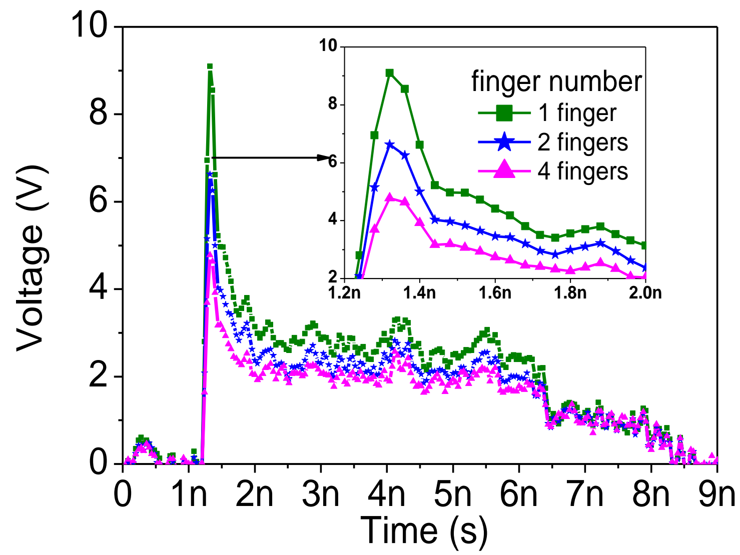
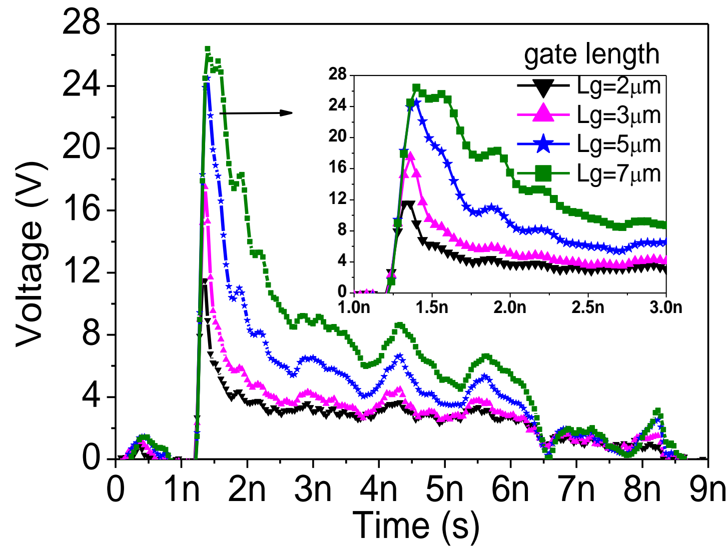


(c)



(d)

Figure 4.7: Voltage waveforms of N+/P-well poly-bound diodes with different (a) diffusion lengths, (b) diode widths, (c) finger numbers, and (d) poly-gate lengths

Based on the results in Figure 4.7(a)-(d), the overshoot voltage and turn-on time vs. different dimension parameters can be extracted and are shown in Figure 4.8. The diffusion length Ld makes almost no impact on both the overshoot voltage and turn-on time. The overshoot voltage decreases and turn-on time remains fairly constant with increasing diode width W and finger number. The effect of poly-gate length Lg is the most prominent, and a smaller poly-gate length gives rise to a lower overshoot voltage as well as a shorter turn-on time.

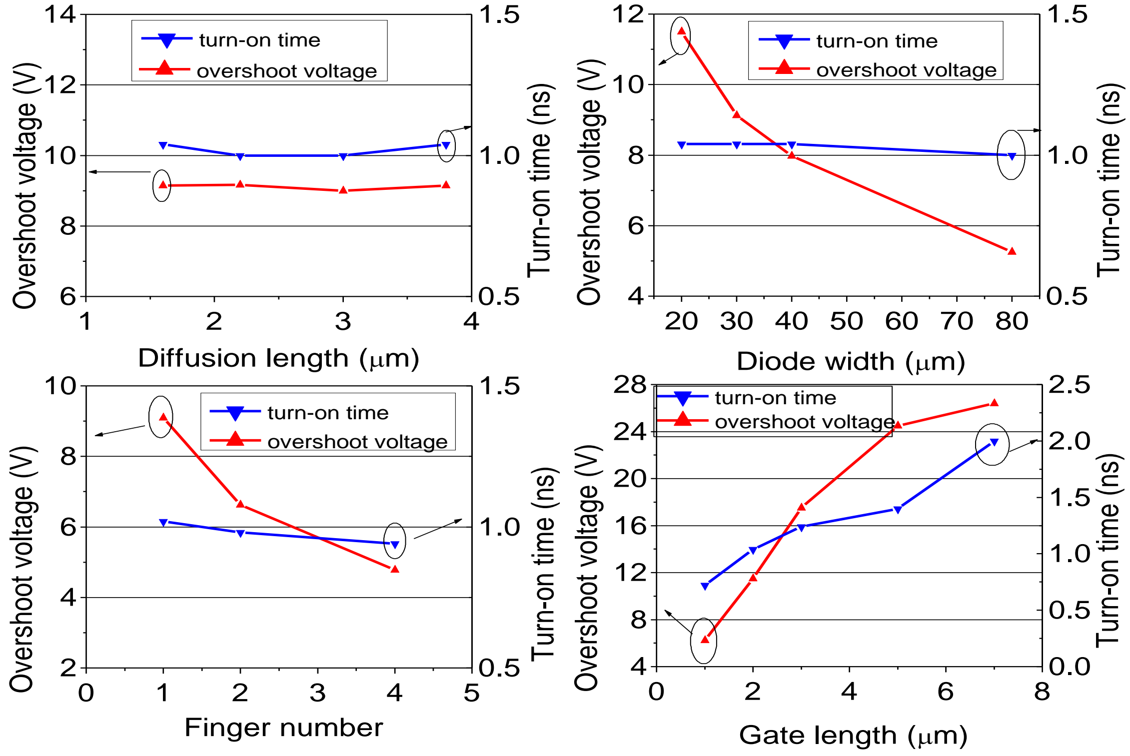


Figure 4.8: Overshoot voltages and turn-on times of N+/P-well poly-bound diodes vs. diffusion length Ld, diode width W, finger numbers and poly-gate length Lg

The reason that the poly-gate length Lg plays such a dominant role in the poly-bound diode's turn-on speed is because it can strongly influence the transit time of the minority free-carriers in the device. Under a fast ESD event, the turn-on time of the N+/P-well poly-bound diode is approximately the transit time of electrons needed to travel across the P-well region. The transit time is defined as [29], [60]:

$$\tau_t = \frac{L_g^2}{4D_n} \tag{4.1}$$

where D_n is the diffusion coefficient of electrons in the P-well region. So the larger is the Lg, the larger is the transit time, and the larger is the turn-on time. As the turn-on time shows no

dependence on the width and finger number of the diode, it does not scale with increasing device size or current, as evidenced by the trends shown in Figure 4.8.

The overshoot voltage is mainly caused by the modulation of the series resistor R_s in the diode's quasi-neutral regions, which is modeled by [72]-[73]:

$$R_s = R_{s0} + \frac{R_{sM}}{1+Q_M/Q_0} \tag{4.2}$$

where R_{s0} is the constant part of the series resistances including the N+/P+ active diffusion region and metal line connection, R_{sM} is the modulated part of the series resistance in the P-well region; Q_0 is the threshold charge for the onset of resistance modulation in the P-well region, and Q_M is the modulated charge for neutralizing the excess electron carriers in the P-well region under high level injection which is dependent of diode's turn-on time τ_t and current I_d [72]:

$$Q_M = \tau_t \cdot I_d \tag{4.3}$$

For times short than τ_t, the modulated charge Q_M will not reach its steady state ($Q_M \ll Q_0$), and as a result, the series resistance becomes $R_{s0} + R_{sM}$ and the overshoot voltage of diode is dependent of this series resistance. The higher is the series resistance, the higher is the overshoot voltage.

Since R_{s0} and R_{sM} are mainly resulted from the resistances in the highly doped N+/P+ diffusion region and lowly doped P-well region, respectively, the series resistance can be further simplified to R_{sM}, which is defined as:

$$R_{sM} = \rho_{pw} \cdot \frac{L_g}{N \cdot W \cdot d_{pw}} \tag{4.4}$$

where ρ_{pw} is the resistivity of the P-well region, and L_g, N, W, d_{pw} are the poly-gate length, finger number, diode width, and depth of P-well region, respectively.

It is clear from equation (4.4) that the series resistance is insensitive to the diffusion length Ld, is proportional to the poly-gate length Lg, and is inversely proportional to the diode width W and finger number N. Such dependencies are consistent with the overshoot voltage trends observed in Figure 4.8.

4.5 Failure mechanisms under fast transient event

In this section, we will investigate in details the correlation between the poly-bound diode failure and the poly-gate configuration, which has been demonstrated in the previous section as the dimension parameter influencing most significantly the diode's transient performance under the VFTLP stress.

Figure 4.9 shows the quasi-static I-V characteristics extracted from the transient waveforms of poly-bound diodes with different gate lengths. The curves in the upper figure are results of diodes stressed by a VFTLP pulse (5-ns duration and 100-ps rise time) to simulate the CDM ESD event, and in lower figure are results stressed by a TLP pulse (100-ns pulse duration and 10-ns rise time) to simulate the HBM ESD event. We define the failure of the poly-bound diodes at the point where the leakage current increases considerably from its normal value. It is interesting to see that under the TLP stress, the on-state resistance of poly-bound diode increases and the failure current remains almost the same with increasing poly-gate length. Under the VFTLP stress, the on-state resistance also increases with the poly-gate length, but the failure current decreases significantly when the poly-gate length becomes longer. This is because the polysilicon gate is connected to the anode region as shown in Figure 4.2, and the voltage pulse that applies to the anode also stresses the gate directly. In addition, unlike the case of TLP stress, the device failure under the very fast transient stress depends less on the energy dissipation but

more on the voltage overshoot [74]-[75]. As the overshoot voltage is directly proportional to the gate length (see Figure 4.8), the gate oxide of poly-bound diode is more likely to be damaged by the VFTLP stress-induced voltage overshoot when Lg is relatively large.

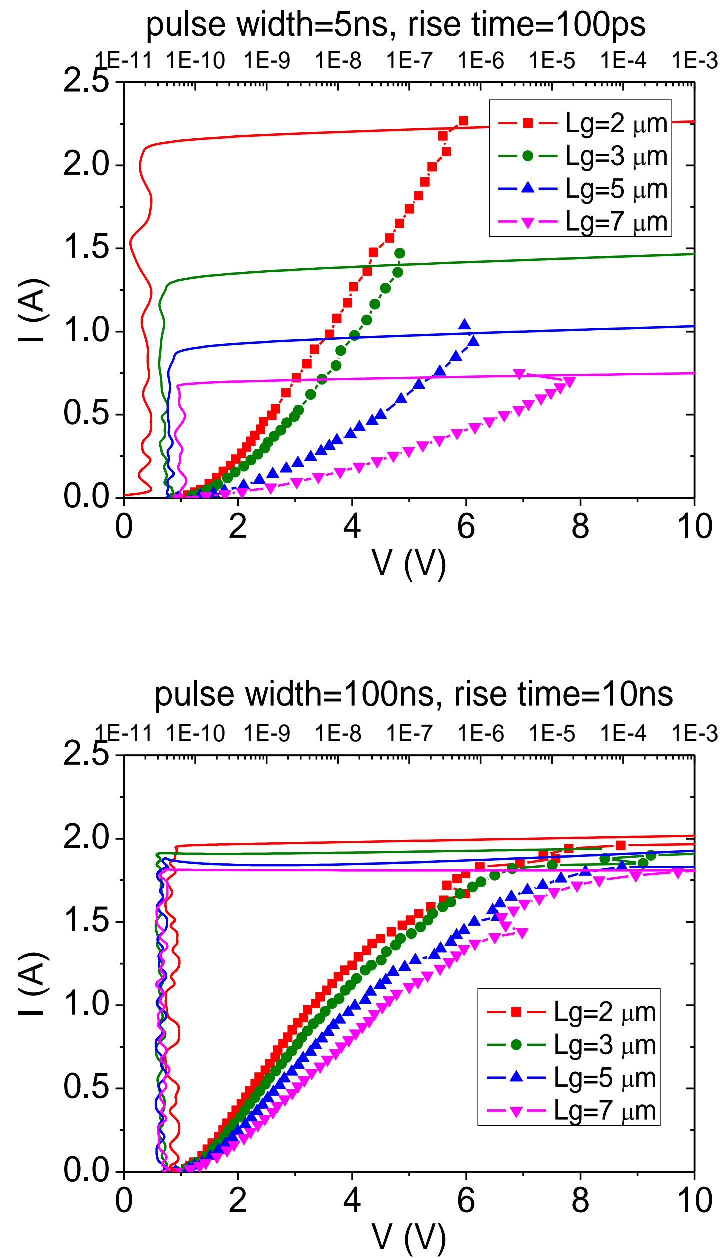


Figure 4.9: Quasi-static I-V characteristics of poly-bound diodes subject to VFTLP (top) and TLP (bottom) stresses

Figure 4.10 shows the voltage waveforms of poly-bound diodes having different poly-gate lengths subject to the VFTLP pulses that cause device failure. It can be seen that the highest voltage the diode can tolerate decreases with increasing gate length. In other words, the diode with the shortest gate length can sustain the largest voltage stress. For example, the diode with a gate length of 2 μm fails at a pulse voltage of 60 V, whereas the diode with a gate length of 7 μm fails at a pulse voltage of 22 V. This is consistent with the finding in Figure 4.9. Note that all the overshoot voltages in Figure 4.10 are about the same (i.e., 30 V) even though the pulse voltages vary. As such, 30 V is the threshold voltage for inducing damage to the 14 nm-thick oxide used in the diodes subject to this particular stress of 100-ps rise time and 5-ns duration.

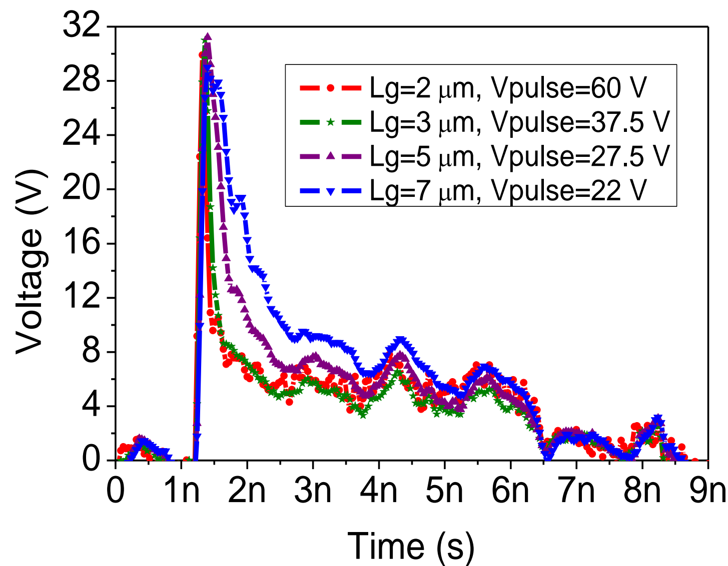


Figure 4.10: Voltage waveforms of poly-bound diodes having different poly-gate lengths subject to the VFTLP voltage pulses that causes device failure

A comparison of quasi-static I-V characteristics extracted from the transient waveforms of poly-bound diodes having the gate floating and the gate tied to anode stressed with VFTLP pulses is shown in Figure 4.11. The results suggest that the diode having the gate floating

configuration has a much higher failure current that its gate tied to anode counterpart. This is due to the fact for the case of gate floating, the pulse does not stress directly to the gate oxide. As such, the failure is related to the damage takes place in the silicon and/or metal, which have a higher ESD tolerance, rather than in the gate oxide.

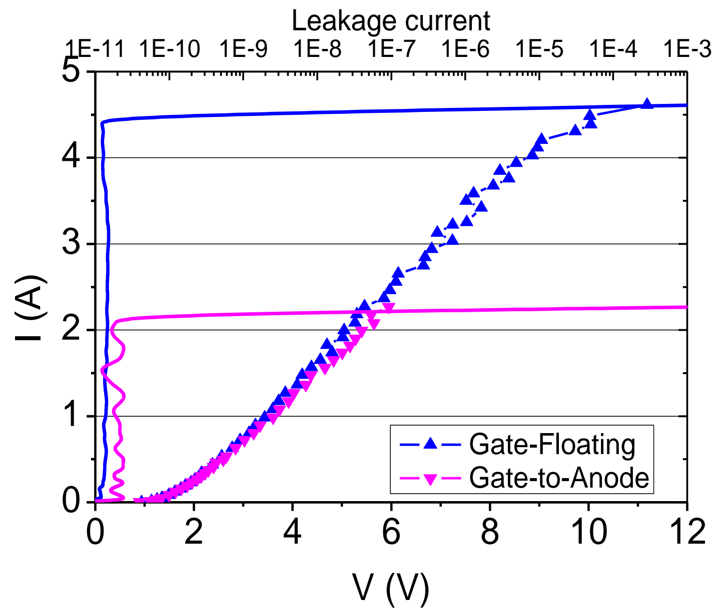


Figure 4.11: Comparison of quasi-static I-V characteristics of poly-bound diodes with gate floating and gate connected to anode

In Figure 4.12, the transient behaviors of the devices with two different poly-gate configurations subject to the VFTLP pulses that cause failure indicate that the gate floating device can tolerate a much higher overshoot voltage than the gate connected to anode diode, a finding in agreement with the results in Figure 4.11. However, the gate potential uncertainty would be a concern for allowing the gate to float.

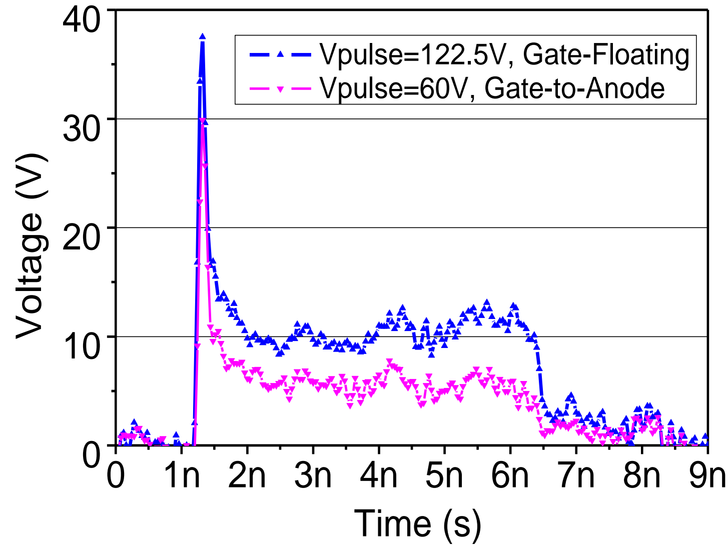


Figure 4.12: Comparison of transient waveforms for poly-bound diodes with gate floating and gate connected to anode subject to the VFTLP pulses that cause failures

Thus, the preceding study has suggested that a poly-bound diode with a normal diffusion length, relatively large width, relatively large number of fingers, relatively small poly-gate length, and gate floating configuration would be an excellent candidate for constructing effective and robust diode-based protection solutions for fast ESD events. However, the gate potential of gate-floating poly-bound diode may be a reliability concern, and a gate-to-anode configuration could be used instead to eliminate such a concern but with the trade-off of a reduced ESD robustness.

4.6 Summary

Transient characteristics of poly-bound diodes under fast ESD events, such as the charged device model (CDM), were investigated using pulses generated from the Barth 4012 very-fast transmission line pulsing tester. In particular, the effects of poly-bound diode's dimension parameters on two ESD figures of merit, namely the overshoot voltage and turn-on time, extracted from the transient waveforms were studied and discussed.

It was found that among the 4 different dimension parameters considered (i.e., diode width, diffusion length, poly-gate length, and finger number), the poly-gate length plays the most dominant role in affecting the diode's fast transient behavior. This is because such a behavior is governed mainly by the minority carrier transport between the anode and cathode regions separated by the polysilicon gate. Specifically, a smaller poly-gate length gives rise to a smaller overshoot voltage and shorter turn-on time, making the diode more suitable for fast ESD protection applications. The correlation between the poly-bound diode failure and poly-gate configuration under the fast transient stress were also addressed, and the results suggested that diodes having the gate floating configuration and a relatively small gate length are less likely to suffer damages induced by fast ESD events.

CHAPTER 5. MULTIPLE-FINGER TURN-ON UNIFORMITY IN SILICON-CONTROLLED RECTIFIERS (SCRs)

5.1 Introduction

Silicon-controlled rectifier (SCR) is a widely used electrostatic discharge (ESD) device for protecting the I/O pins and power supply rails of integrated circuits [39], [76]. Since the SCR operates with snapback characteristic and is triggered under the avalanche breakdown condition of low-doped N-well/P-substrate junction, the trigger voltage is generally greater than the gate-oxide breakdown voltage of input stages and makes it hard to achieve ESD protection for low-voltage applications. The modified lateral SCR (MLSCR) inserts an additional highly doped N+ diffusion region at the boundary of N-well and P-substrate regions and lowers its trigger voltage to the breakdown voltage of N+/P-substrate junction [77]. However, it could be still too high to effectively protect the thin gate oxide of input stages. To further reduce the trigger voltage, the low-voltage triggering SCR (LVTSCR) is invented with the integration of a grounded-gate NMOS to trigger the SCR action and the trigger voltage is equivalent to the lower drain breakdown voltage of short channel NMOS device [78].

To achieve an optimal ESD protection performance, multiple fingers of SCR are often needed. However, the uniformity of finger triggering and current flow is always a concern for multi-finger SCR devices operating under the post-snapback region [79]. Without a proper understanding of the finger turn-on mechanism, design and realization of robust SCRs for ESD protection applications are not possible. The placement of SCR's anode and cathode regions is one of key design factors affecting the turn-on uniformity of SCR devices with multiple fingers, however, few discussion is available in previous literature.

In this work, two two-finger SCRs with different combinations of anode/cathode regions are considered, and their finger turn-on uniformities are analyzed based on the I-V characteristics obtained from the transmission line pulsing (TLP) tester. The effects of different pulse rise times on the finger turn-on behavior of the SCRs are also investigated. The devices were fabricated in a 0.6-μm BiCMOS process with LOCOS (Local Oxidation of Silicon) oxide isolation between the highly doped N+ and P+ diffusion regions. In the ESD testing, the cathode of SCR is grounded and the anode is subject to the ESD stress.

5.2 Device structures

Figure 5.1 shows the cross-section views of two two-finger SCR structures. The first, called the anode-cathode-anode SCR (ACASCR), has one cathode region in the middle and two anode regions on the right-hand and left-hand sides of the cathode region. The other, called the cathode-anode-cathode SCR (CACSCR), has one anode region in the middle and two cathode regions on the right-hand and left-hand sides of the anode region. The ACASCR and CACSCR have the same dimensions, including identical N+, P+, and oxide lengths, layout, and metal connections. But the paths of current flow in the devices are different. Figure 5.2 shows the current paths in each SCR structure. The purple color denotes the level-1 metal placed on top of the N+ and P+ diffusion regions, and the green color denotes the level-2 metal connected to level-1 metal through multiple vias. ACASCR has metal lines 1 and 3 connected to the two anode regions and metal lines 2 and 4 connected to the single cathode region. When subjecting to the ESD stress, the current flows into the ACASCR through metal lines 1 and 3 from the left, enters the two anode regions, transports to the cathode region, and finally flows out of the device

to the right via metal lines 2 and 4. The same description applies to the CACSCR, but the current in the device flows from the right-hand side to the left-hand side.

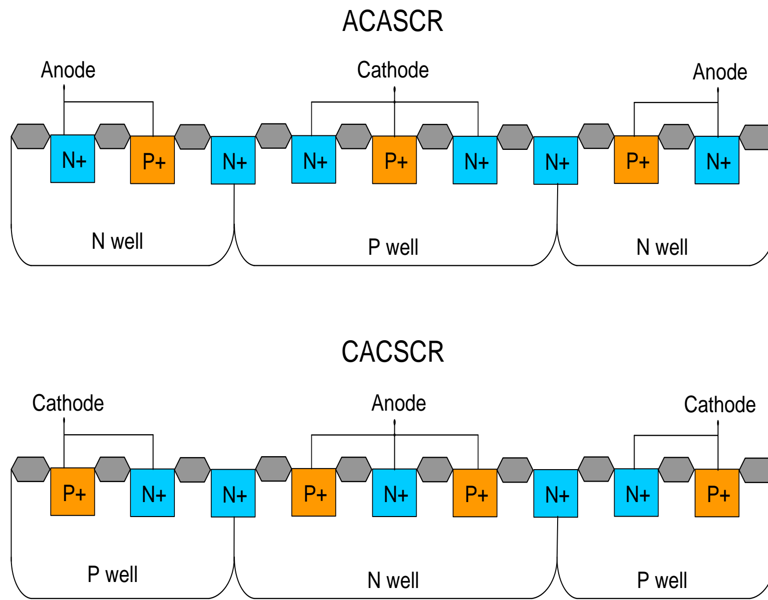


Figure 5.1: Schematics of the cross-section of the ACASCR and CACSCR structures

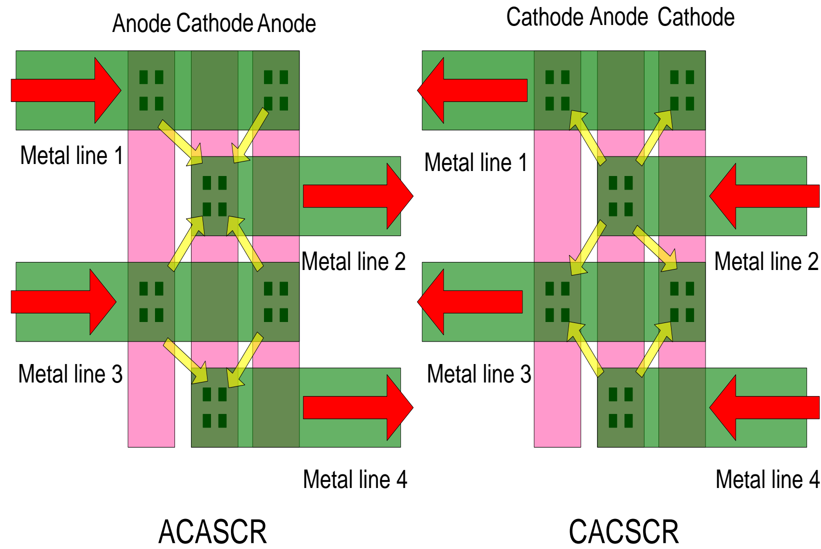


Figure 5.2: Schematics illustrating the current flow paths in the ACASCR and CACSCR

5.3 TLP results and analysis

Figure 5.3 shows the measured current-voltage (I-V) characteristics of the ACASCR and CACSCR stressed with the human body model (HBM) equivalent pulses having a 100 ns width and 10 ns rise time generated from the transmission line pulsing (TLP) tester. Also included in the figure is the TLP I-V curve of an SCR having one finger but otherwise identical structure as the ACASCR and CACSCR (i.e., half of the ACASCR or CACSCR).

Note that the failure current It2 (the current at which the leakage current increases suddenly from its normal value) of the ACASCR is half of that of the CACSCR (2.35 A vs. 4.79 A). As will be discussed below, this stems from the fact that only one of the two fingers in the ACASCR is turned on. Both the ACASCR and CACSCR have the same on-state resistance (3.43 Ω) when the current is lower than 0.8 A. Beyond this current level, the on-state resistance of the CACSCR is cut in half (i.e., 1.79 Ω) and the on-state resistance of the ACASCR remains the same. Figure 5.3 also shows that the ACASCR has almost identical I-V curve as the one-finger SCR, suggesting that only one of the two fingers in the ACASCR is turned on under all the current levels whereas both fingers in the CACSCR are turned on when the current is sufficiently high (i.e., above 0.8 A). Thus, the CACSCR exhibits improved turn-on effectiveness and is more robust than the ACASCR counterpart for ESD protection applications.

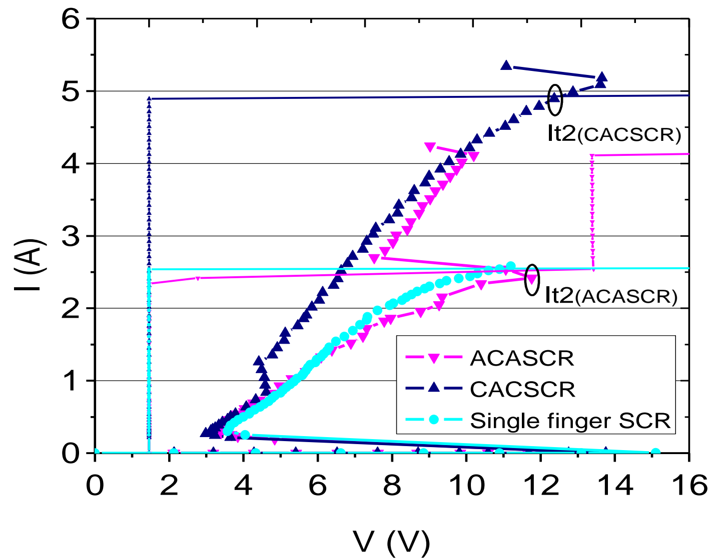


Figure 5.3: I-V characteristics of the ACASCR and CACSCR stressed with 100-ns width and 10-ns rise time pulses generated using the transmission line pulsing tester

The equivalent circuits of the ACASCR and CACSCR structures shown in Figure 5.4 can be used to explain the finger turn-on mechanism in these devices. Let us first focus on the ACASCR, which consists of two separated anode regions and one cathode region sharing the P-well region. In other words, the ACASCR has two parasitic PNP bipolar transistors and two NPN transistors sharing the same P-type base region. Under the ESD stress, the high voltage at the anode first causes avalanche breakdown in one of the two reverse-biased N+/P-well junctions. Holes are generated by impact ionization and flow into the P-well region. Such a hole injection gives rise to a potential increase in the P-well region, which forward biases the P-well/N+ junction and triggers the NPN bipolar transistor. The collect current of NPN transistor flowing in the N-well region reduces the N-well potential, forward biases the P+/N-well junction, and triggers the parasitic PNP bipolar transistor. Subsequently, the finger associated with this PNP bipolar transistor in the ACASCR is turned in the post-snapback mode. As will be explained later,

this process does not trigger the other parasitic PNP bipolar transistor, and the second finger remains off.

On the other hand, the CACSCR has two cathode regions and one anode region sharing the N-well region, or the two parasitic PNP bipolar transistors share the same N-type base region. Similar to the ACASCR, one finger of CACSCR is turned on due to the triggering of a parasitic PNP bipolar transistor at relatively low current levels. However, since the two fingers share the same N-well region, after one of fingers is triggered and carrying the current, a large amount of electrons and holes are generated in the shared N-well region. The holes then flow to the P-well region associated with the other finger because of the increasing electrical field and potential. As such a hole current becomes sufficiently large, it forward biases the P-well/N+ junction, triggers the parasitic NPN bipolar transistor, turns on the second finger in the CACSCR, and reduces the on-resistance to half of its original value when the current is increased beyond 0.8 A (see in Figure 5.3).

Let us revisit the ACASCR. After triggering one of the two fingers in the ACASCR, like the CACSCR, the avalanche generated electrons in the shared P-well can also flow to the N-well region associated with the other finger. However, the parasitic PNP transistor is much harder to turn on than the parasitic NPN transistor due to the fact that the current gain of the PNP transistor is an order of magnitude lower than that of the NPN transistor [32]. As a result, only one finger is turned on in the ACASCR under all the current conditions.

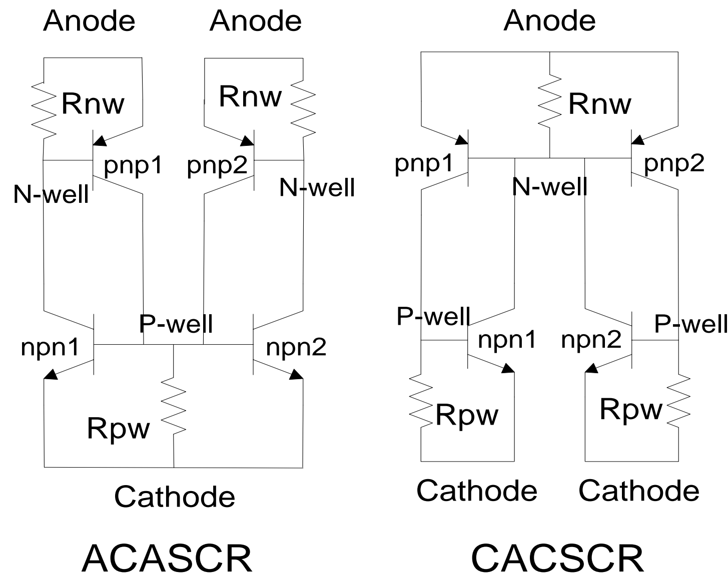
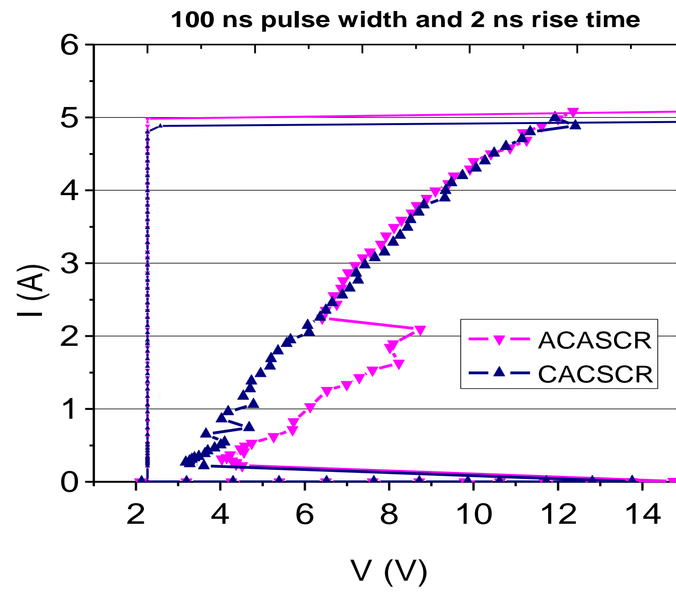


Figure 5.4: Equivalent circuits of the ACASCR and CACSCR structures

5.4 dV/dt effect

Figure 5.5 shows the I-V characteristics of the ACASCR and CACSCR structures stressed with TLP pulses having a 100 ns pulse width and 2 ns rise time (top figure) and 200 ps rise time (bottom figure). These pulses have the same duration but much shorter rise time than the pulses used in Figure 5.3. Unlike the case in Figure 5.3, both fingers in the CACSCR subject to the 2-ns and 200-ps rise time pulses are turned on as soon as the device enters the snapback mode. This is due to the dV/dt effect [80] associated with the fast pulse which generates a substantial displacement current through the depletion capacitance of the N-well/P-well junction and this extra current facilitates the triggering of both parasitic NPN bipolar transistors and thus both fingers as soon as the CACSCR enters the snapback mode. As the effect of dV/dt is less prominent for the slower 2-ns rise time pulse, in this case both fingers in the ACASCR are not turned on until the current reaches 2 A.



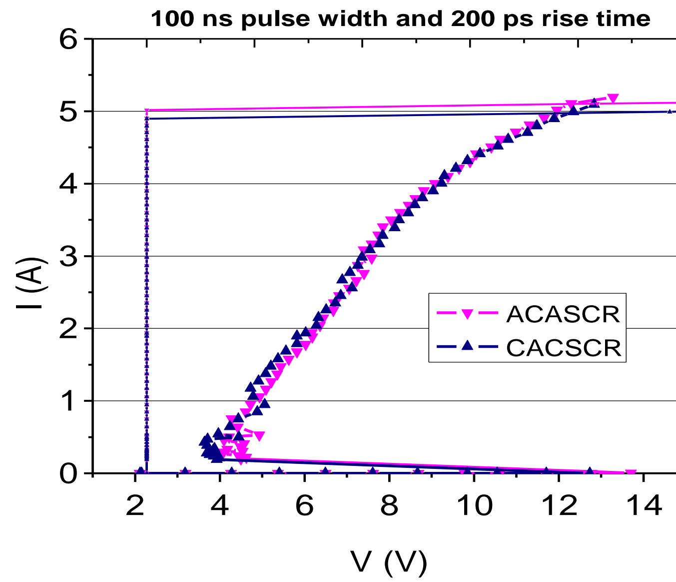


Figure 5.5: I-V characteristics of the ACASCR and CACSCR stressed with 2-ns rise time (top) and 200-ps rise time (bottom) pulses generated by the TLP

5.5 Summary

Multiple-finger turn-on uniformity and mechanism of two different two-finger silicon-controlled rectifier (SCR) structures, CACSCR and ACASCR, were investigated based on the current-voltage characteristics measured using the transmission line pulsing tester. The CACSCR structure having two cathode regions and one anode region showed better finger turn-on effectiveness than the ACASCR structure having two anode regions and one cathode region. The turn-on behavior of the SCR structures was also improved when subjecting to pulses with a faster rise time due to the enhanced displacement current effect.

CHAPTER 6. CONCLUSIONS

ESD related failure is always a major concern for IC reliability and results in a loss of millions dollars to the semiconductor industry each year. To avoid or reduce the IC's failures due to ESD, dedicated on-chip ESD protection structures and schemes are commonly used to discharge the ESD current and clamp overstress voltage under different ESD events. The dissertation starts with the fundamentals of ESD phenomena and existing ESD stress models. The main contributions of this dissertation are having investigated the effect of various design parameters on the overall ESD protection performance of diodes with different anode/cathode isolation technologies and having designed the optimal ESD diode structures achieving both low parasitic capacitance and fast turn-on speed for low-voltage ESD protection applications.

The ESD performance of LOCOS-bound diode with different diffusion layouts, metal connection patterns, dimensions, geometries and junction configurations were first investigated experimentally using pulses generated from the Barth 4002 transmission line pulsing tester. For LOCOS-bound diodes with the parallel metal connection, a smaller diode width and larger number of fingers give rise to higher failure current It2 and lower on-state resistance Ron. On the other hand, diodes with the crossing metal connection would work more effectively when a multiple-finger and/or multiple-metal line structure was used. To account for both the ESD robustness and the parasitic effect, the diode having a stripe structure, crossing metal pattern, large device width, and lowly doped well layer yields the best overall ESD protection performance and lowest parasitic capacitance. The results provide useful insights into optimizing the LOCOS-bound diode for robust HBM ESD protection applications.

Polysilicon-bound diodes were then compared with LOCOS-bound diodes based on TCAD simulation and experimental measurement results. The better performed polysilicon-bound diode was investigated in more details in order to come up with an optimal diode structure for robust ESD protection applications. Specially, the effects of the diode width, cathode length, finger number, polysilicon gate length, terminal connection, and metal topology on the diode's failure current and on-state resistance were considered. Two figures of merit were also developed to better judge the effects of these parameters on the diode's overall ESD performance. Our study suggested that a polysilicon-bound diode with a relatively large cathode length, relatively large diode width, relatively large number of fingers, relatively small polysilicon gate length, poly-to-anode terminal connection, and metal topology having 2 or 3 anode/cathode metal lines would be an excellent candidate for constructing effective HBM ESD protection solutions for low-voltage integrated circuits.

Transient characteristics of polysilicon-bound diodes under fast ESD events, such as the charged device model (CDM), were also investigated using pulses generated from the Barth 4012 very-fast transmission line pulsing tester. In particular, the effects of polysilicon-bound diode's dimension parameters on two ESD figures of merit, namely the overshoot voltage and turn-on time, extracted from the transient waveforms were studied and discussed. It was found that among the 4 different dimension parameters considered (i.e., diode width, diffusion length, poly-gate length, and finger number), the poly-gate length plays the most dominant role in affecting the diode's fast transient behavior. This is because such a behavior is governed mainly by the minority carrier transport between the anode and cathode regions separated by the polysilicon gate. Specifically, a smaller poly-gate length gives rise to a smaller overshoot voltage and shorter turn-on time, making the diode more suitable for fast ESD protection applications.

The correlation between the polysilicon-bound diode failure and poly-gate configuration under the fast transient stress were also addressed, and the results suggested that diodes having the gate floating configuration and a relatively small gate length are less likely to suffer damages induced by fast ESD events.

In the end, the multiple-finger turn-on uniformity and mechanism of two different two-finger silicon-controlled rectifier (SCR) structures, CACSCR and ACASCR, were investigated based on the current-voltage characteristics measured using the transmission line pulsing tester. The CACSCR structure having two cathode regions and one anode region showed better finger turn-on effectiveness than the ACASCR structure having two anode regions and one cathode region. The turn-on behavior of the SCR structures was also improved when subjecting to pulses with a faster rise time due to the enhanced displacement current effect.

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