DESIGN, CHARACTERIZATION AND ANALYSIS OF COMPONENT LEVEL ELECTROSTATIC DISCHARGE (ESD) PROTECTION SOLUTIONS

by

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ABSTRACT

Electrostatic Discharges (ESD) is a significant hazard to electronic components and systems. Based on a specific process technology, a given circuit application requires a customized ESD consideration that meets all the requirements such as the core circuit's operating condition, maximum accepted leakage current, breakdown conditions for the process and overall device sizes. In every several years, there will be a new process technology becomes mature, and most of those new technology requires custom design of effective ESD protection solution. And usually the design window will shrinks due to the evolving of the technology becomes smaller and smaller. The ESD related failure is a major IC reliability concern and results in a loss of millions dollars each year in the semiconductor industry. To emulate the real word stress condition, several ESD stress models and test methods have been developed. The basic ESD models are Human Body model (HBM), Machine Mode (MM), and Charge Device Model (CDM). For the system-level ESD robustness, it is defined by different standards and specifications than component-level ESD requirements. International Electrotechnical Commission (IEC) 61000-4-2 has been used for the product and the Human Metal Model (HMM) has been used for the system at the wafer level.

Increasingly stringent design specifications are forcing original equipment manufacturers (OEMs) to minimize the number of off-chip components. This is the case in emerging multifunction mobile, industrial, automotive and healthcare applications. It requires a high level of ESD robustness and the integrated circuit (IC) level, while finding ways to streamline the ESD characterization during early development cycle. To enable predicting the ESD performance of IC's pins that are directly exposed to a system-level stress condition, a new the human metal

model (HMM) test model has been introduced. In this work, a new testing methodology for product-level HMM characterization is introduced. This testing framework allows for consistently identifying ESD-induced failures in a product, substantially simplifying the testing process, and significantly reducing the product evaluation time during development cycle. It helps eliminates the potential inaccuracy provided by the conventional characterization methodology. For verification purposes, this method has been applied to detect the failures of two different products.

Addition to the exploration of new characterization methodology that provides better accuracy, we also have looked into the protection devices itself. ICs for emerging high performance precision data acquisition and transceivers in industrial, automotive and wireless infrastructure applications require effective and ESD protection solutions. These circuits, with relatively high operating voltages at the Input/Output (I/O) pins, are increasingly being designed in low voltage Complementary Metal-Oxide-Semiconductor (CMOS) technologies to meet the requirements of low cost and large scale integration. A new dual-polarity SCR optimized for high bidirectional blocking voltages, high trigger current and low capacitance is realized in a sub 3-V, 180-nm CMOS process. This ESD device is designed for a specific application where the operating voltage at the I/O is larger than that of the core circuit. For instance, protecting high voltage swing I/Os in CMOS data acquisition system (DAS) applications. In this reference application, an array of thin film resistors voltage divider is directly connected to the interface pin, reducing the maximum voltage that is obtained at the core device input down to ± 1-5 V. Its ESD characteristics, including the trigger voltage and failure current, are compared against those of a typical CMOS-based SCR.

Then, we have looked into the ESD protection designs into more advanced technology, the 28-nm CMOS. An ESD protection design builds on the multiple discharge-paths ESD cell concept and focuses the attention on the detailed design, optimization and realization of the in-situ ESD protection cell for IO pins with variable operation voltages. By introducing different device configurations fabricated in a 28-nm CMOS process, a greater flexibility in the design options and design trade-offs can be obtained in the proposed topology, thus achieving a higher integration and smaller cell size definition for multi-voltage compatibility interface ESD protection applications. This device is optimized for low capacitance and synthesized with the circuit IO components for in-situ ESD protection in communication interface applications developed in a 28-nm, high-k, and metal-gate CMOS technology.

ESD devices have been used in different types of applications and also at different environment conditions, such as high temperature. At the last section of this research work, we have performed an investigation of several different ESD devices' performance under various temperature conditions. And it has been shown that the variations of the device structure can results different ESD performance, and some devices can be used at the high temperature and some cannot. And this investigation also brings up a potential threat to the current ESD protection devices that they might be very vulnerable to the latch-up issue at the higher temperature range.

To my wife Yuan Peng, my parents Jian Luo and Daohua Xiong

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LIST OF ACRONYMS

BCD	Bipolar-CMOS-DMOS
Bi-SCR	Bi-Directional SCR
BJT	Bipolar Junction Transistor
BV	Breakdown Voltage
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DAS	Data Acquisition System
DNW	Deep N-Well
DUT	Device Under Test
EOS	Electrical Overstress
ESD	Electrostatic Discharge
FOM	Figure of Merits
GGNMOS	Gate-Grounded N-type MOSFET
HBM	Human Body Model
HMM	Human Metal Model
IC	Integrated Circuits
IEC	International Electrotechnical Commission
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OEM	Original Equipment Manufacturer

SCR	Silicon Controlled Rectifier
SCS	Semiconductor Characterization System
SEM	Scanning Electron Microscope
STI	Shallow Trench Isolation
TLP	Transmission Line Pulsing
VFTLP	Very Fast Transmission Line Pulsing
WLCSP	wafer-level-chip-scale-package

CHAPTER 1 INTRODUCTION

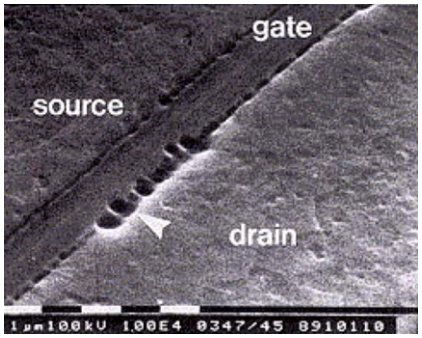
1.1 ESD Event and ESD Failure

Electrostatic Discharge (ESD) event is a common phenomenon in our life, especially in the winter touching a doorknob after walking in a carpeted room. It is an electrical discharge event happens between two object at different potentials. The creation of those static discharge electricity is created by an unbalance of electrons on the surface of a material. Those electric energy can range from a few hundreds volts to a few kilo volts, and discharge a huge amount of energy within a few hundreds nano-second. Those large amount of charge can conducted into a grounded integrated circuit (IC), causing the soft and catastrophic damage of the core circuit. It is also a subset of failure known as electrical overstress (EOS) [1]. In modern ICs, there are a huge amount of the circuit failure are result from the ESD event. Without properly design, the weak robustness in the IC can cause the whole system malfunctioning after an ESD stress. It becomes more and more critical as the technology develops with more and more ICs integrated into the automobile and medical use, it will cause the serious safety issue without proper protection design.

ESD events occurs throughout a product's lifetime, from early wafer-fabrication process to assembly operation, package, wire bonding, and shipping, to the user end applications. Without sufficient ESD protection solutions, the soft and catastrophic damages could happen easily. There are 10% to 90% of the total failure models are result from the ESD event. As microelectronics technology continues shrink to nano-metric dimensions, ESD damage in IC has become one of the major reliability issue [1].

There are various reasons causing the ESD failure, and most common failure mechanism is from three aspect. First is the localized heat regeneration, which is generated from the current going through the metalized connection of internal ICs. When the heat dissipation is not large enough to dissipate enough heat, it will usually causing the metal connection rupture. Another two are from the high electric field intensities and high current densities. For a certain ICs, there are maximum allowance of the highest current density for ESD stresses. The high current density in the device will increase the lattice temperature, which will result a positive feedback increasing the current density at that point future. This usually results the thermal damage in the device structure causing the malfunction of the IC. Figure 1-1 shows the failure analysis results from different devices that suffering catastrophic ESD damages, such as Oxide damage in MOS transistor (a) [1], Drain junction filamentation (b) [1], interconnects damage (c) [2]and ESD diode burnout (d) interconnect damage[1].

(a)



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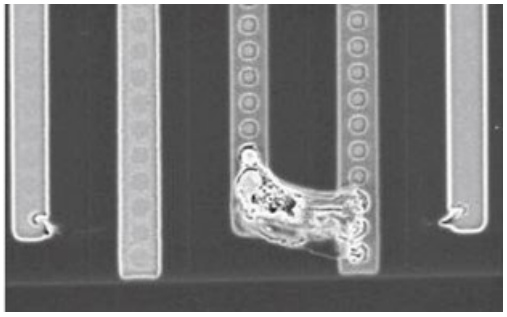

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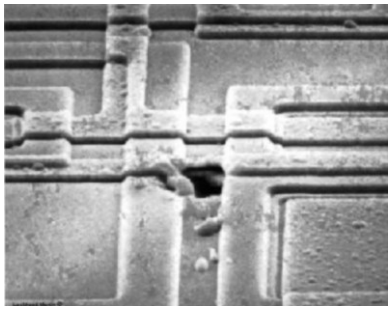


(d)

Figure 1-1 Example of failure analysis photo for catastrophic damage due to the ESD event

1.2 ESD Stress Model and Test Methods

When the ESD events happens at different situation, the characteristics of those events are very different. To quantify and reproduce the real-world ESD event, there are several different catalogs has been used, such as Human Body Model (HBM), Charge Device Model (CDM), Human Metal Model (HMM) and System-level IEC 61000-4-2 model. Based on the different waveform those models specified, the simplified RLC network is used to describe those models with the ideal switches to emulate the ESD events. With additional distributed parasitic elements connected in the ESD test system, they can generate the real world stress to the ICs.

1.2.1 HBM model

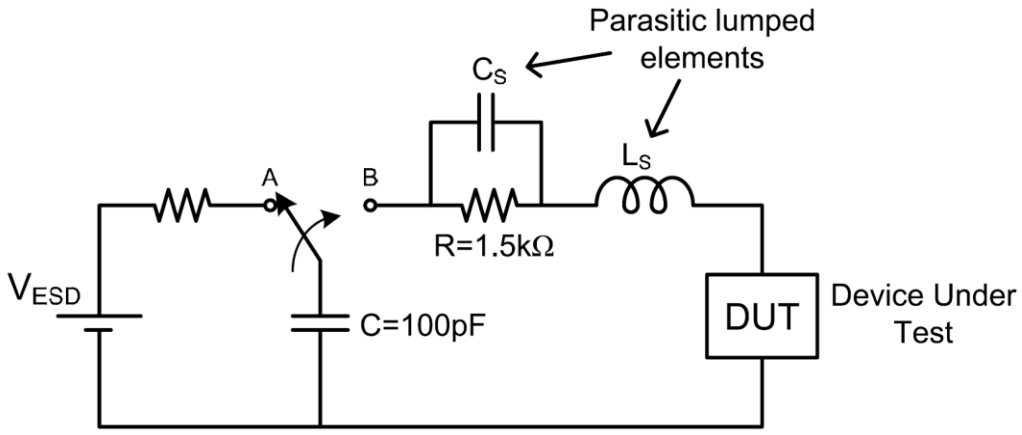


Figure 1-2 A simplified equivalent circuit for HBM ESD model

HBM ESD event represent a charged human body contacts one pin of a grounded semiconductor device or an IC directly, transferring the charge into the device. It is the most commonly used model. During the normal handling and assembly operations, human body can be charged with electrical energy and transfer that charges to a semiconductor under various conditions. HBM ESD testing is performed to evaluate of the effectiveness or robustness of the protection designs in a ICs.

Figure 1-2 shows a simplified equivalent circuit of HBM model, where the value of C_{HBM} = 100pF, R_{HBM} = 1.5kΩ and L_{HBM} = 7500nH are used to replicate a charged human body. Those values are based on the most commonly used HBM standards include JEDEC JESD22-A114-B and ESDA [6] STM5.1-1998 [7].

1.2.2 CDM Model

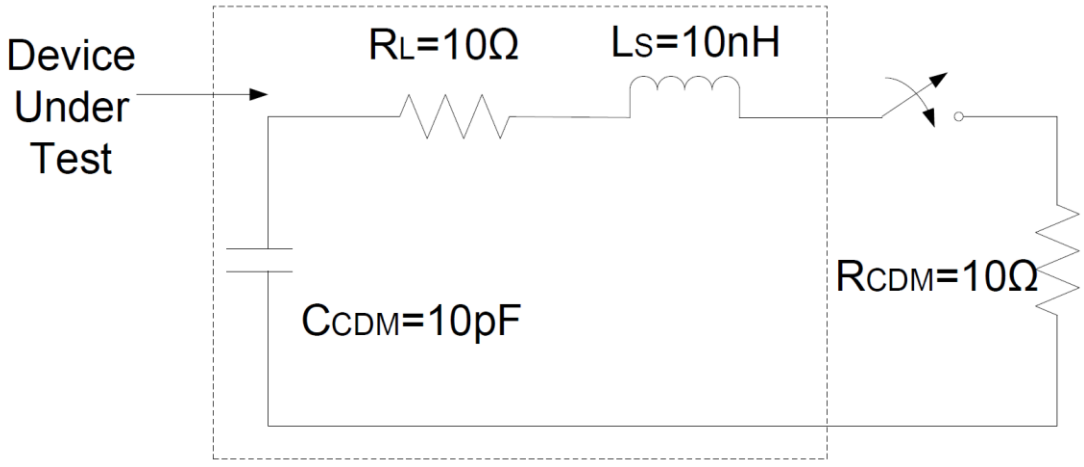


Figure 1-3 An equivalent circuit for CDM ESD stress model

The charge device model (CDM) was developed to replicate the IC self-charging and self-discharging events. A charge IC part discharges when a pin contacts a grounded object or conductive surface. During the manufacturing and field application environments, the IC parts will be pre-charged. It is different to the HBM due to the self-discharging process. However, due to its extremely low discharge resistance and inductance, it will produce more rapid and large ESD current (tens of amperes in 100ps). It is more deadly event for some applications, especially with the thinner oxide from more advanced process technology. Comparing to the previous HBM model, the pick current of CDM ESD stress can reach much higher level, and the CDM stress has smaller stress duration. Thinner dielectric films, such as oxidation, in CMOS technologies are more vulnerable to CDM ESD event. Inside the fully automatic operation in manufacturing lines, the major failure are likely caused by the CDM ESD event [8].

A simplified equivalent circuit for the CDM ESD model is shown in Figure 1-3, where the C_{CDM} = 10pF, R_{CDM} = 10Ω, R_L = 10Ω, and L_S = 10nH. The integrated circuit usually will have small parasitic capacitance, resistance and inductance when self-discharge. The commonly used standard are known as JEDEC JESD22-C1-1-A [9] and ESDA STM5.4.1-1999 [10].

1.2.3 IEC and HMM model

When the ICs integrated with all the components together, the overall better performance is the customer want to achieve. Increasing demand of the overall performance drives the designers not only consider the standalone ESD protection, but also the full chip level ESD protection. Previous model can only guarantee the chip level performance but cannot guarantee system level protection, where both voltage and current waveform from the ESD stress will be completely different. To ensure the system-level ESD robustness, IEC61000-4-2 was developed

for system level ESD testing [11]. An ESD gun, specialized tester, is usually used to produce such ESD stress.

To allow the IC manufacturer to predict the system level ESD performance of their product, the human metal model (HMM) has been introduced. It reproduces the ESD discharge caused by a human touching a pin of a grounded electrical component with a metal tool [12]. Using a novel HMM testing module can reproduce the IEC waveform at wafer-level testing more stable, comparing to the old ESD gun based wafer-level testing [2].

1.2.4 ESD Testing Method

The transmission-line pulse (TLP) system has been used to characterize on-chip electrostatic discharge (ESD) protection structure in the integrated circuit industry. This technique has been introduced by Maloney and Khurana [13] in 1985. The TLP system allows the ESD engineers more accurately measure the conditions that cause IC failures. Different from the HBM, CDM and IEC ESD test methods that only gives the results ESD failure threshold, it is giving an insight information about the current to voltage I-V characteristics of those structures during ESD stress. Those information can be analyzed to provide possible failure mechanisms inside the structure.

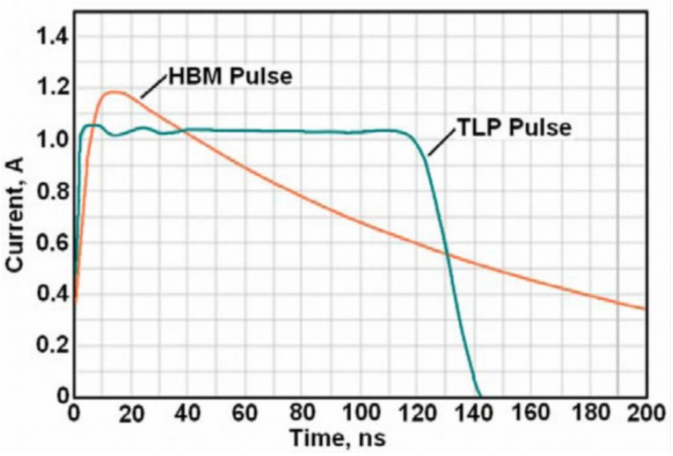


Figure 1-4 HBM pulse vs. TLP ulse.

The TLP uses the rectangular/square-pulse to simulate the energy in an exponential HBM test pulse. Figure 1-4 compares between the HBM pulse and the TLP pulse. The TLP waveform are different to the real world ESD event. However, it is strictly a tool that designers can use to characterize the performance of ESD protection structure and perform circuit analysis and failure analysis. Even though the waveform is different, some researches does showing consistent correlation factors between HBM and TLP for specific types of devices [14]. Compare to the HBM test, the rectangular pulse also provides more accurate pulse shapes. Also eliminate the self-heating effect, which damage the DUT under DC test, so that the ESD stress can reach a much higher level and provides additional information such as trigger voltage, snapback condition (holding voltage and current), soft failure (leakage degradation), and breakdown can be clearly captured. Using the correlation factor, the HBM robustness level can be simply calculated by multiply a factor to the TLP failure current I_{t2} [15].

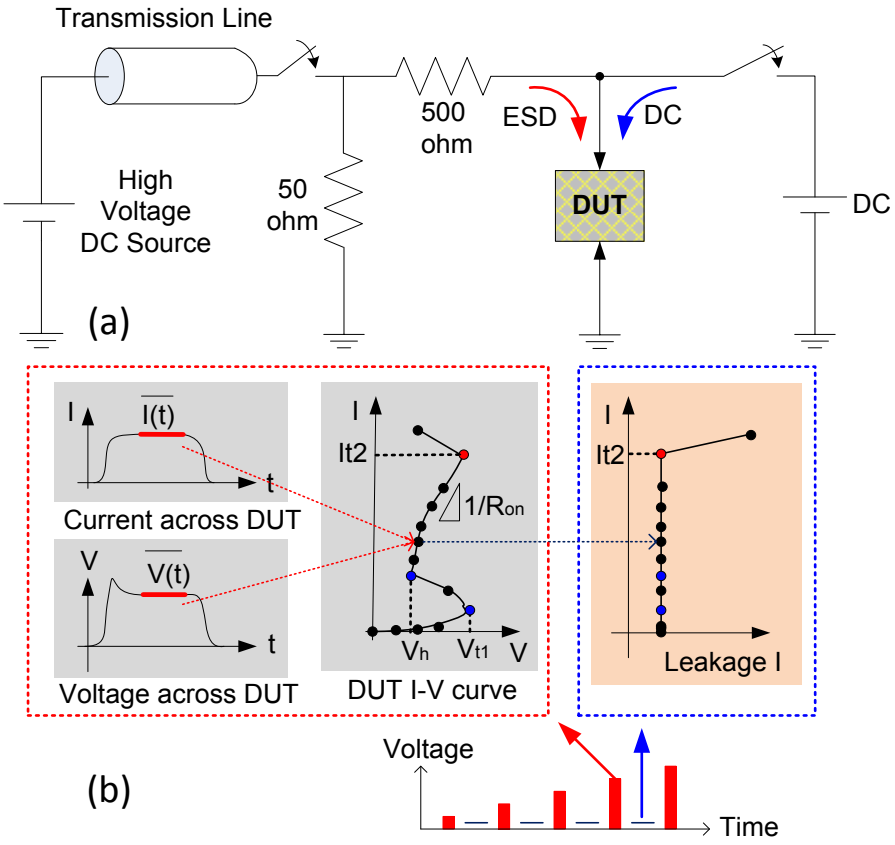


Figure 1-5 (a) TLP test system and (b) TLP waveform

In order to produce a TLP waveform into the DUT, a high-voltage DC source is used inside the TLP tester to charges the transmission line. When the transmission line discharged, after turn on the switch, it will create a current injection to the device under test (DUT). Figure 1-5 (a) shows a schematic of a typical Barth TLP tester system. A 50 Ω resistor is a controlled load for the transmission line. By using the digitized data from the voltage and current analyzer, a TLP tester will build an I-V curve through numerous sets of measurements. The average window is used to make the results more consistent and accurate. Figure 1-5 (b) explains the mechanism inside the TLP tester, like Barth 4002. The default measurement window is between 70%-90% of

the pulse width, and it is called the quasi-static region [16]. The average value are used to plot each point in the I-V curve. To determine the device failure, a post leakage test has been applied between each stress using a DC voltage bias. Typical identification of failure are the significant increase (a few order) of this leakage current. And the small changes in the leakage current may represent a soft failure. The I-V curve can also reveals failure, such as a sudden changes of current in the waveform due to the damage of metal wire or vias, as well as abrupt voltage change due to the internal junction failure. From the TLP measurement, simple extraction from the I-V curve we can get the trigger voltage V_{t1}, holding voltage V_h, failure current I_{t2}, failure voltage V_{t2}, on resistance R_{on}, and leakage current $I_{leakage}$ [18].

The TLP system is only valid to simulate the HBM ESD event. For the CDM event, a very fast TLP (VFTLP) system will be used [19]. The VFTLP system is the same setup as compare to the TLP system. But it is capable of generating a rectangular pulse between 1ns to 10ns pulse width with a rise time of 100ps. It can also provide the VFTLP I-V curve and the waveforms, which can be used to analysis the turn-on speed and the voltage overshoot. In our research work, most of the characterization is using the Barth 4002 TLP system and Barth 4012 VFTLP testers.

1.3 ESD Protection and Design Window

ESD event can happens between any of the two pins of an integrated circuit. Ideally, we will need a low resistive ESD protection device or a circuit bypasses the stress in any of these situations to prevent the core circuit from damage. But such protection devices need to stay in off condition while the chip in the normal operation condition. In order to keep the IC full functioning, it requires low parasitic effect, such as low leakage current, low capacitance, low

resistance low power consumption. Also it will be able to conduct enough ESD current during the ESD event.

Figure 1-6 shows an ESD protection blocks that provide protections between the I/O to VDD, VDD to VSS and I/O to VSS for a whole chip protection method. There are several modes that bypass the stress under the ESD event: 1) PD mode: positive ESD stress between the input pin and VDD, when VDD is grounded. Assuming all the protection devices are bi-directional, through the ESD protection I and Power clamp, there are two current conduction path (solid and doted blue line) can bypass the ESD current in this mode; 2) PS mode: positive ESD stress between the input pin and VSS, when VSS is grounded. In this case, the I/O protection II and the Power clamp also offers two current conduction path (solid and doted red line) to bypass the ESD current; 3) ND mode: negative ESD stress between the input and the VDD, when the VDD is grounded. The I/O ESD protection I and the power clamp can provide two current conduction path (dash green line and doted green line) to bypass the ESD current; 4) NS mode: negative ESD stress between the input and the VSS, when the VSS is grounded. The I/O ESD protection and the power clamp provides two current conduction path (solid and doted purple line) to bypass the ESD current. For the output pin protection, it will be the similar case compare to the input. The I/O protection III and IV works with the power clamp providing different current path to different ESD event.

Both I/O pads and the VSS/VDD power lines need to have effective ESD discharging path in submicron CMOS ICs. And it becomes more important for nanometer CMOS circuit, especially when there are higher parasitic resistances and capacitances resulting from the larger chip size and longer VDD and VSS power rails [20].

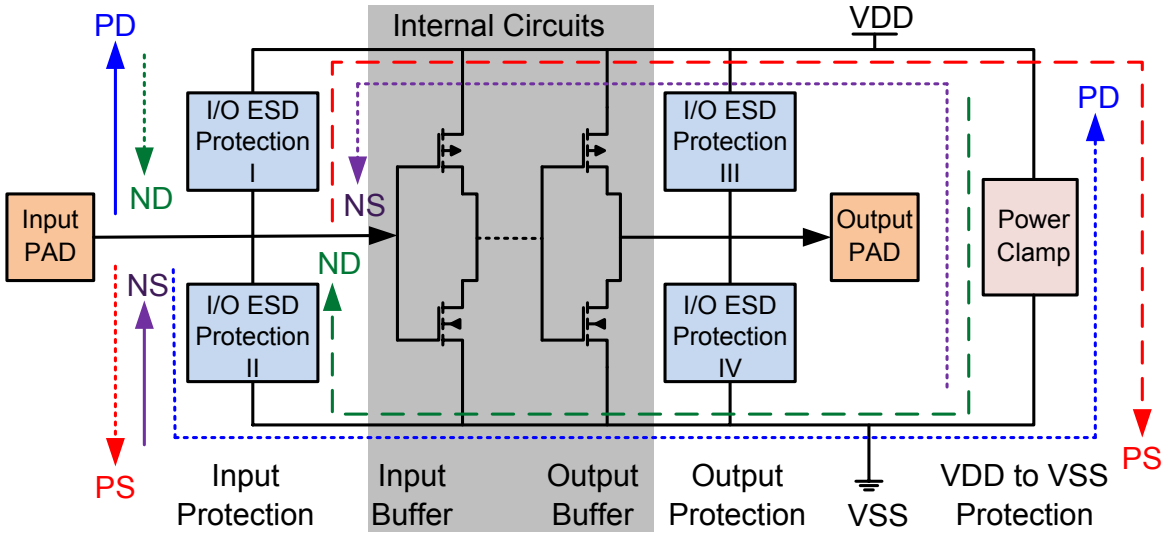


Figure 1-6 Whole chip ESD protection and conducting modes

Figure 1-6 shows a whole chip ESD protection stratagem, which protect every possible ESD discharge paths. The protection devices can varies from a single device to a protection circuit, and they need to be in off-state during the normal circuit operation. Then when the ESD event happens, turns on providing a low impedance path to conduct excess current. ESD device need to be able to detect the ESD events in a very short window.

In order to meet those requirements, the characteristics of the ESD protection devices need to stay within a certain design window. Many different aspects need to be taken into account for the design and optimization of the ESD protection solutions in advanced CMOS technologies. Figure 1-7 shows a typical ESD design window and I-V characteristics of a basic ESD protection device.

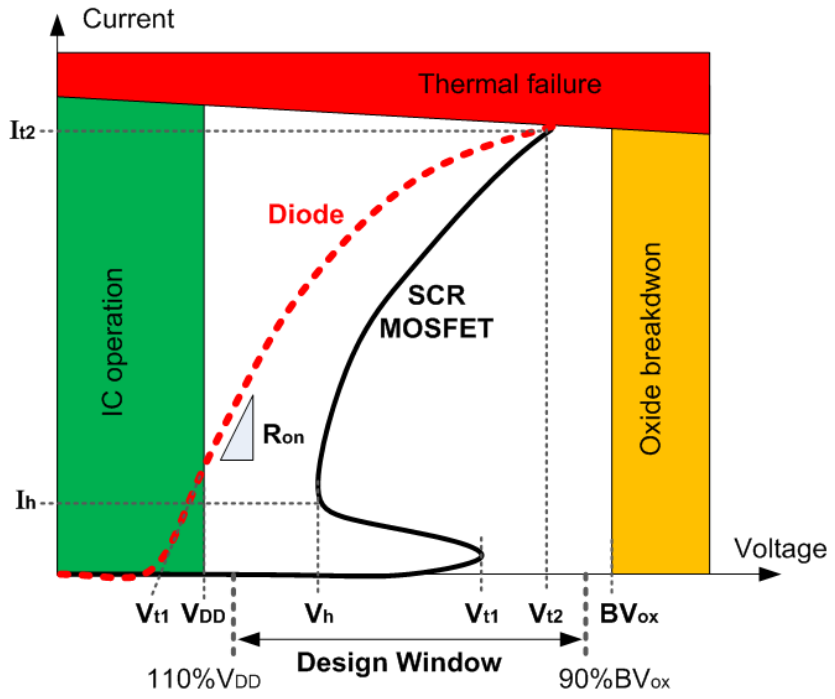


Figure 1-7 ESD design window and TLP characteristic of basic ESD protection device

The protection device should not affect the normal IC operation, so its triggering voltage (V_{t1}) must be higher than that, plus the signal range and some noise margin. Additionally, the voltage drop across the protection element during an ESD event should be limited to a certain range. In that case, even though the protection devices is not dead, but the high voltage drop could damage the gate oxide of the input/output driver and also the transistors of the core circuit. A 10% safety margin is usually needed to make ESD protection designs more robustness.

For a snap-back type of devices, like silicon control rectifier (SCR), they should have a trigger voltage (V_{t1}) smaller than the BVox but larger than VDD. So that they can turns on during the ESD event and not damaging the gate oxide, and also keeps in off-state during normal operation. The holding voltage V_h needs to be higher than the V_{DD} to avoid latch-up issue,

otherwise there will be a chance letting the ESD protection device turns on and short the core circuit. The holding voltage is depending on the process technology and the device structure, by increasing to a high holding current I_h devices or use the guard ring can reduce the risk and providing a latch-up free design. For a non-snapback device, like diode, can be used by stacking them at the supply pin. A higher trigger voltage can be achieved by connecting them in series.

The key parameter for a ESD protection device include: trigger voltage V_{t1}, holding voltage V_h, holding current I_h, failure current I_{t2}, on resistance R_{on}, leakage current $I_{leakage}$, parasitic resistance R, capacitance C, voltage overshot, turn-on speed, turn on time and size. The designer should take all the parameters into consideration, and choose the one that provides best protection efficiency and minimum interference introduced to the core circuit [21].

1.4 Basic ESD protection devices

1.4.1 Diode

Diode are the most commonly used ESD protection devices due to its structural simplicity, and it also provides high current conductivity under forward bias and low leakage under reverse biasing condition [22]. Figure 1-8 illustrate the cross-section of junction diodes using different structures: (a) diode junction formed between P+ and N-well; (b) P-substrate and N+; (c) poly-silicon diode; (d) poly-bound diode.

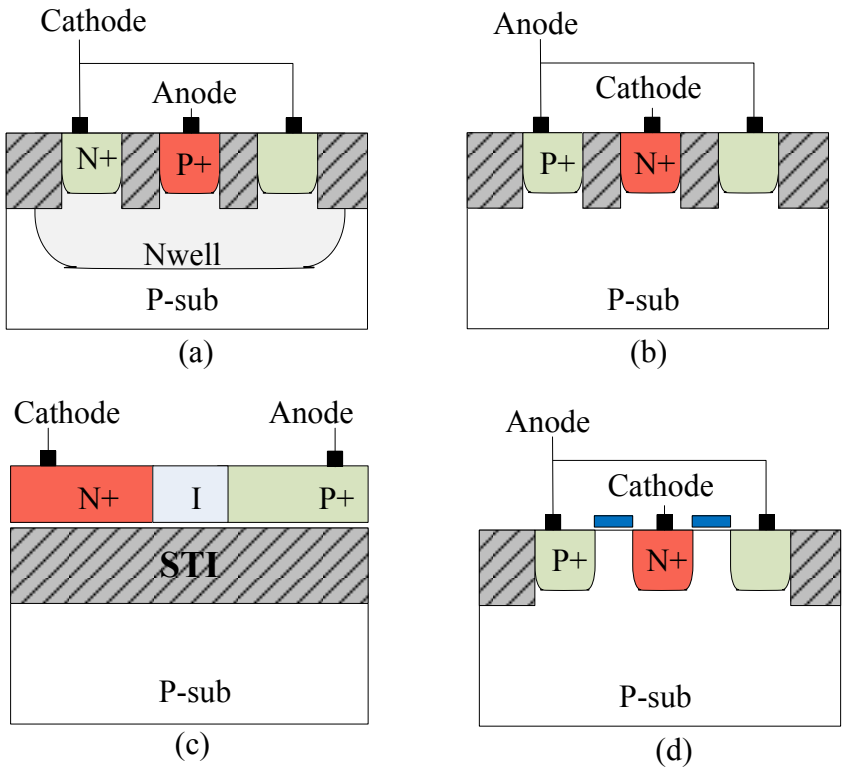


Figure 1-8 Cross-section of diodes that use different types of junctions.

Zener diode is another option, which can also be used in the ESD protection circuits. The trigger voltage of a zener diode will be lower comparing to PN diode. Also a lower on-voltage. This required a process in the manufacturing process called silicide block. In addition to the Tungsten or Cobalt interface to the semiconductor material, silicidation has becomes a standard CMOS process step in submicron technologies. Figure 1-9 shows the cross section of this zener diode.

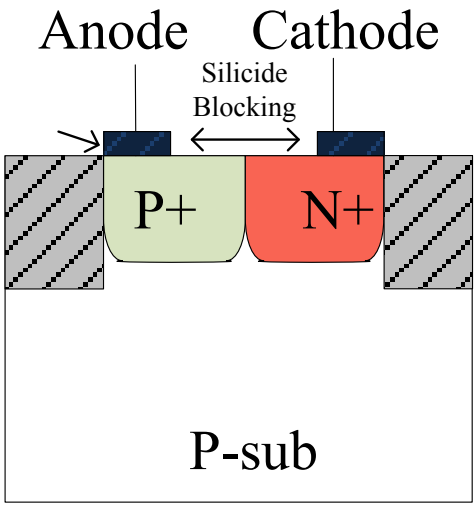


Figure 1-9 Zener diode

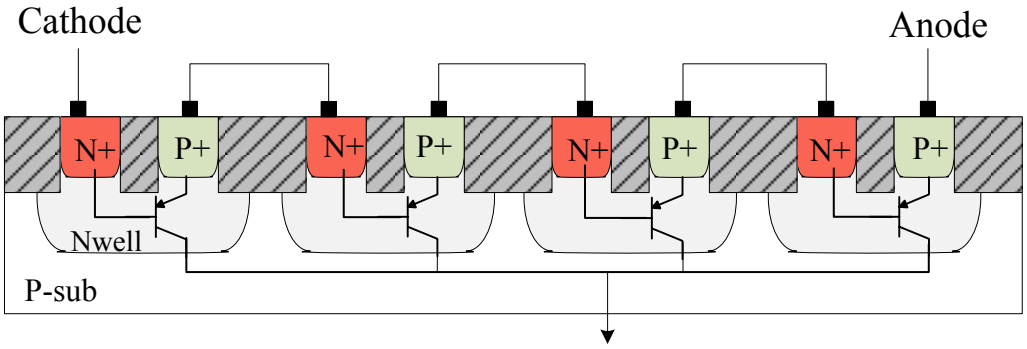


Figure 1-10 Four diode string with parasitic BJT

In order to adjust the turn-on voltage, diode string can be used with forward biased junction diode in series. It offers the flexibility to control its turn-on voltage by adjusting the number of the diode [24].

Another advantage of the diode string is the reduction of parasitic capacitance. When the number of stacked diode reaches three, they usually will saturated. Due to the increasing of the junction capacitance, which will increase with the number of the diode. And this junction

capacitance wont be in series as the parasitic capacitance. This configuration is a better choice for the high frequency applications. On the other hand, higher parasitic resistance and larger area are the major limitations of this method [25]. Also the self-heating effect, higher capacitance, and leakage induced power dissipation need to be considered as well.

1.4.2 MOSFET

MOSFET is commonly used in the CMOS process technology. The simplest for of a MOSFET used in the ESD protection applications is the grounded gate NMOS (GGNMOS). They are one types of snapback devices. Similar to the reverse biased diode, it will go into the breakdown region wile the voltage across them is increased. After the breakdown point, the voltage across the device will drops and the device will move from the breakdown region into the saturation region.

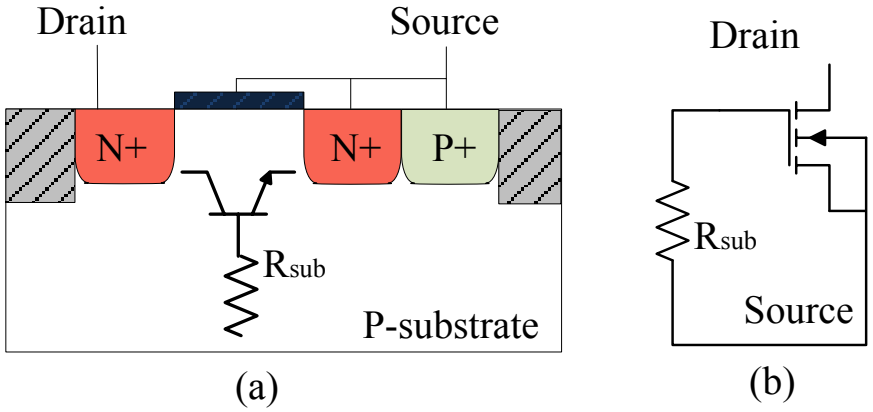


Figure 1-11 (a) cross section and (b) equivalent circuit of GGMOS

Figure 1-11 shows a cross section of gate grounded N-type MOSFET. The gate and the source are shortened to ensure the off-state of the NMOS during the normal operation of the core

circuit. When ESD event happens, the ESD pulse stresses on the drain of the GGMOS. Avalanche breakdown takes place as the stress level goes higher and holes and electrons are generated by impact ionization. With the parasitic NPN bipolar transistor formed by the N+ drain, P-substrate and N+ source, the potential at the P-substrate will reaches a level to forward bias the base-emitter junction of this BJT, it turns on to sink the ESD current under a certain voltage and current. After triggering, The higher drain current will rise due to the electrons channeling from emitter (source) to collector (drain). As a result, the GGMOS goes into snapback operation region with a negative resistance characteristics. The post snapback region requires higher voltage to maintain the BJT action due to the reduced body resistance after conductivity modulation.

The multi-finger layout and silicidation process is resulting the major challenges of ESD protection design using GGNMOS in modern technologies. By increasing the area efficiency, give rise to the risk of non-uniform turn-on on the multi-fingers. Many literatures have been published to solving those issues. For example, silicidation is used to add to process to helping drain, source and gate region [26]. Alternatively, the N well, segmentation and back-end poly resistors are also been proposed to address those issue [28],

1.4.3 SCR

Another type of commonly used snapback ESD protection device is silicon controlled rectifier (SCR). It offers better ESD robustness and least capacitance comparing to diode and GGMOS at same layout size. But it is not widely available due to the high current and breakdown regions in the operation of SCR for ESD application. Figure 1-12 has shown its cross section and the equivalent circuit. The lateral NPN and PNP transistor are formed by Nwell/P-

sub/N+ and P+/Nwell/P-sub. When the terminal is exposed to the ESD stress, the junction between Nwell and P-sub is reverse biased, while the ESD stress is reaching a certain limit, this junction initiates avalanche breakdown. High ESD current increases the junction voltage drop that turns on both PNP (Q1) and NPN (Q2) transistor. Due to the higher gain and then pulls down the potential of the collector of NPN, the NPN will usually turns on first. And it is also the base of the PNP, then PNP turns on and inject more current to the base of NPN. The positive feedback between PNP and NPN keeps the SCR to maintain the on-state while does not need high voltage biasing [1]. The avalanche breakdown voltage of the Nwell and P-sub determins the trigger voltage of the devices itself. Different device structure is needed to modify the trigger voltage.

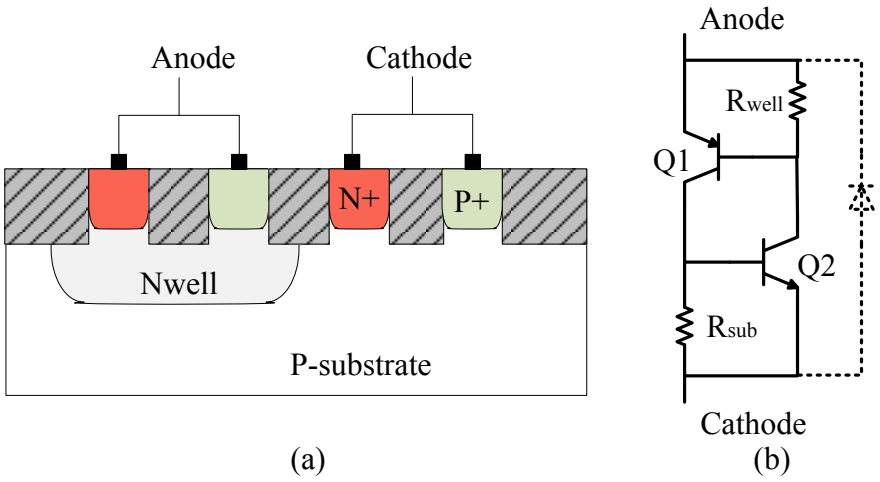


Figure 1-12 Cross-section and simplified equivalent circuit of SCR

SCR usually has higher failure level and layout area efficiency in CMOS ICs. But the SCR device still has a higher trigger voltage (as much as 22V) in the 90nm CMOS technology, where the oxide breakdown voltage is around 10V. And it will be future decreased with the

shrinkage of CMOS technologies. Thus it is imperative to reduce the trigger voltage and to enhance the turn on speed of SCR for effectively protection the ultrathin gate oxide from latent damage or rupture, especially against the fast charged-device-model (CDM) ESD events [32].

For more effective ESD protection, the SCR based ESD devices were designed with low enough triggering voltage. But the transient induced latch-up issue still need to be solved. Special technique is needed to increasing the holding current, such as modifying layout dimensions can be used to improve holding voltage. Also a segmentation layout, extra resistance, stacking of several SCRs, and additional diode are the potential options to avoid the latch-up issue [33]. And latch-up immunity can be achieved by increasing the holding current as well [36].

1.5 Dissertation outline

Different technologies and applications require customized ESD consideration at the early stage of design and development. The goal of this research is to develop novel, effective solutions for the system-level ESD requirements, and develop more robust and ESD protection solutions for advanced CMOS technologies. This dissertation is summarized as following:

Chapter 1 presents some of related the background information, from the ESD event and failure model as well as the major ESD protection device and concept. And also briefly mentioned about the system-level ESD requirement. Chapter 2 covers a comprehensive study of the system-level ESD characterization methodology. Discuss the drawback of the conventional testing method. Providing a novel way for HMM characterization to be more accurate and more efficient. Chapter 3 developed a dual polarity conduction and high blocking voltage ESD protection devices realized in an 180nm CMOS technology. This ESD device is designed for a specific application where the operating voltage at the I/O is larger than that of the core circuit.

Chapter 4 reports the design of monolithic ESD Protection Structure for variable operating voltage interface applications in 28-nm CMOS Process. This ESD structure is capable of providing multiple discharge-paths and multiple operating voltages for in-situ IO protection. Chapter 5 will discuss the performance variation of ESD protection devices under different temperature. The chapter 6 will covers the summary of the dissertation and outlook for the future research.

CHAPTER 2 A NOVEL PRODUCT-LEVEL HUMAN METAL MODEL CHARACTERIZATION METHODOLOGY

2.1 Introduction

Increasingly stringent design specifications are forcing original equipment manufacturers (OEMs) to minimize the number of off-chip components. This is the case in emerging multifunctional mobile, industrial, automotive and healthcare applications. It requires a high level of electrostatic discharge (ESD) robustness at the integrated circuit (IC) level [11], while finding ways to streamline the ESD characterization during the early development cycle.

To enable predicting the ESD performance of IC's pins that are directly exposed to a system-level stress condition, the human metal model (HMM) test method was introduced [37]. The HMM testing at the wafer-level has been proven to provide valuable insight into the stand-alone protection devices robustness [37], and the transmission line pulsing (TLP) versus HMM correlation has also been studied [38]. But extending the wafer-level testing to the IC-level (or product-level) characterization imposes additional complications. As will be shown later, the conventional approach of observing the post-stress leakage current change is no longer suitable for failure detection at the IC-level.

In this chapter, a new testing methodology for product-level HMM characterization is introduced. This testing framework allows for consistently identifying ESD-induced failures in a product, substantially simplifying the testing process, and significantly reducing the product evaluation time during development cycle. For verification purposes, this method has been applied to detect the failures of two different products. It is worth mentioning that a previous work has reported a new methodology for the failure detection under the HBM stress [39].

2.2 Conventional methodology

The integrated circuit industry has been using transmission-line pulse (TLP) testing to characterize on-chip electrostatic discharge (ESD) protection structures since 1985. This TLP ESD testing technique was introduced by Maloney and Khurana as a new electrical analysis tool to test the many single elements used as ESD protection structures. IC designers now use TLP testing in increasing numbers, because it provides a reliable, repeatable, and constant amplitude waveform. The TLP testing lets ESD engineers more accurately measure the conditions that cause IC failures. TLP uses the rectangular-pulse testing or square-pulse testing to simulate the energy in an exponential HBM test pulse.

The square pulsing ESD test techniques, such as TLP and VFTLP, are the standard analysis tools for characterizing the protection devices behavior during the ESD event. Those includes the trigger voltage, holding voltage, failure current and leakage current particularly. It is the only technique to study the internal ESD behavior in integrated circuits. TLP testing provides detailed knowledge about the actual ESD current paths, which is not available from traditional ESD test on ICs. [1]

During the ESD test, a very important characteristics is the failure current, which determines the robustness of the ESD protection devices or the passing level of the combined ICs. The system and devices engineer is depending on the characteristics of all the parameters to achieving the device with the best performance without sacrificing the overall performance. To determine the failure current, the TLP system is using the leakage evaluation between each pulse to determine the highest passing level. And the leakage test point is usually selected between 10-20% below the breakdown voltage. Figure 2-1 demonstrate the conventional leakage evaluation

that TLP system uses. Each point of the I-V curve from the TLP was taken from the average window from transient waveform, then there will be a DC leakage test before next pulse coming in (blue region). When the leakage is showing the consistency after each pulse, it means devices passed the stress level that is given to the DUT. If the leakage showing there is drastic changes after the pulse, such as the one after red dot on the blue region, it means devices fails at that level. And the highest current this device or IC can reach is the failure current (I_{t2}).

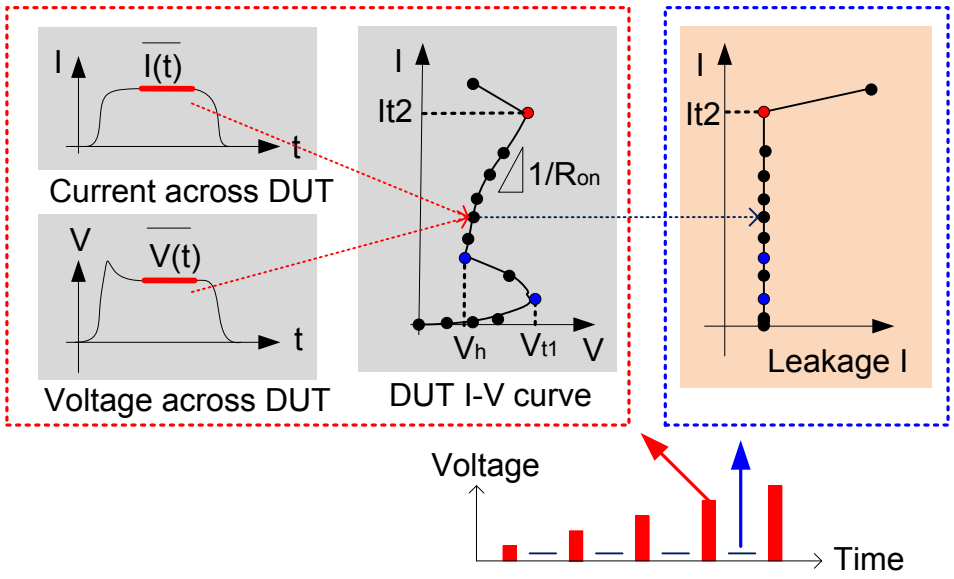


Figure 2-1 Conventional leakage evaluation of the TLP test system

Characterization methods for system-level and component-level ESD stresses exist in parallel. To represent the system level ESD event at the component level, human metal model (HMM) alternative has been proposed using IEC 61000-4-2 basic. To allow the IC manufacturer to predict the ESD performance of their products under system level stress conditions at early stage of the design. [2]

HMM reproduces the ESD discharge caused by a human holding a metal tool touching a pin of a grounded electrical components. It simulates a system-level type of ESD stress at the component level. Providing an inside of the system level performance at the early stage of the design flow. Help reduce the production time of the designer to achieve the ESD requirement more efficiently. Using the ESD gun is the initial stage when there are not specific HMM testers available. To capture the waveform using an oscilloscope for the ESD gun and ESD system level pulses is extremely difficult. And sometimes the results is not stable and accurate when captured, this is mainly due to the high electrical magnetic fields generated by the ESD gun. Also the connection cable can also cause a false readings on the oscilloscope. Usually it require to disconnect the DUT from the TLP setup and perform the ESD gun test. Then after the test, it was using the same method as the TLP to detect the failure [40].

More recently, the test setup has been improved using the specific HMM/HBM testers, such as Hanwa, HPPI system. Figure 2-2 shows an improved HMM testing module setup. Using this module, which can be mounted on a standard wafer prober, delivers a stress waveform according to the IEC 61000-4-2 standard. By using this module, the electromagnetic disturbances caused by the traditional ESD gun can be eliminated during the discharge. It provides more consistent stress and more accurate waveform. And the stress module are changeable according to the specific waveform standard. In Hanwa system, you can switch the stress module between HBM and HMM stress. And the failure detection are still be monitored by the leakage current between each stress.

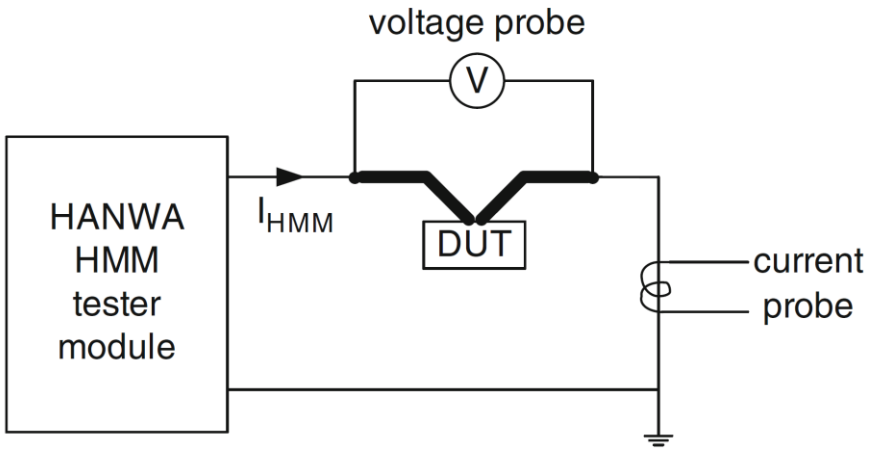


Figure 2-2 wafer level HMM measurements setup for HANWA system.

2.3 Limitations of conventional methodology

For all the traditional ESD testing methodology, the leakage evaluation are used as a standard failure detection method. It was assumed to faile when snapback was observed in the voltage wave and when a subsequent leakage increase was measured. However, when the traditional ESD testing methodology was used more and more for evaluating all kinds of devices and ICs, in some cases, the leakage does not change even when the device failed [39]. Especially after the system-level evaluation was introduced, the more and more complex current path in those component resulting the inaccuracy of conventional leakage evaluation. In this section, two product at the wafer level has been evaluated to demonstrate the limitation of the conventional leakage evaluation.

The first product is a transceiver for industrial applications. This product has four transceiver interface pins and a ground (Vss) connection directly exposed to the environment at the system-level. Figure 2-3 shows a simplified schematic of the transceiver interface pin

connected to a voltage divider of the core circuit. The transceiver pins have independent ESD protection between the pin and the Vss ground. Due to signal conditioning design constraints, no protection can be included in this application from the transceiver pins to the power supply.

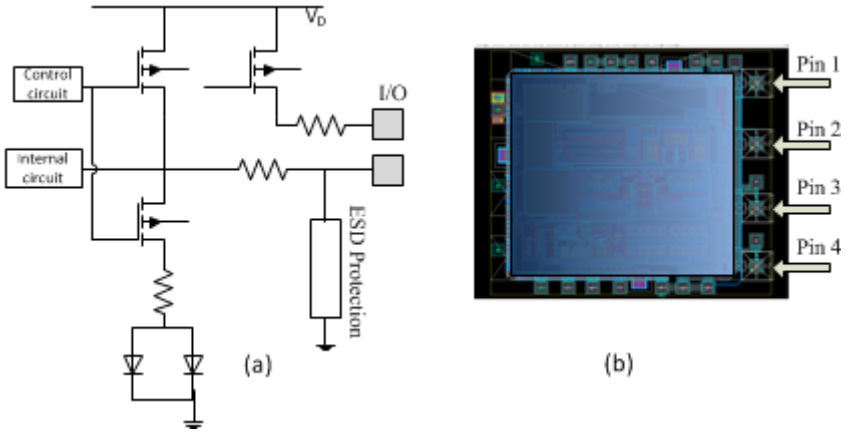


Figure 2-3 (a) Simplified schematics of industrial transceiver interface circuit (Product 1) and (b) Top-level layout view

To evaluate this product's ESD performance, we have performed standard TLP test first. Figure 2-4 shows the TLP measurement for one pin of the product I. It is obtained using the Barth model 4002 TLP tester generating pulse with 100-ns width and 2-ns rise time. The blue curve is the first TLP test, it shows the leakage changes at the -6A. Initially, we that leakage increase will be an identification for the failure current of this tested pin of product I. However, after some other test results from the product line using functional testing confirmed that this product actually will survives after the +/-20A TLP current. This discrepancy shows indicates that there might be something turns on during the TLP testing and stays on during the following test.

In order to eliminate the charge stored inside the device, we applied the small positive or negative pulse at that pin and also letting the product rest for some time. The red curve in Figure

2-4 shows the TLP test at the same device, the leakage has been restored to the fresh condition. At this point, we believe the product is survived at -6A TLP. For a standalone device, the current path are identical and the leakage change can be an indication of the failure. However in this product, due to the complexity of the current path inside the chip, there might be some charge stored inside the capacitor inside the product during the test and stays on after that point. But the leakage increase due to this reason is not an identification of the failure. This is one example that the leakage evaluation is inaccurate during the wafer-level products ESD characterization. And the summary of the characterization accurate data is shown in Table 2-1.

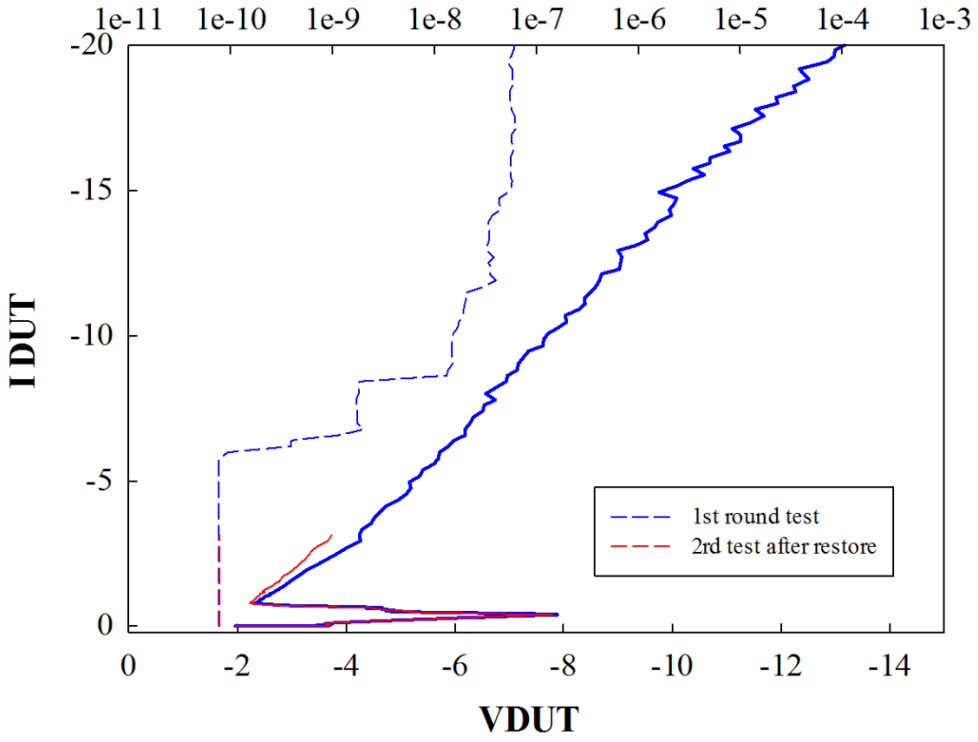


Figure 2-4 TLP results from one pin of the product I

Table 2-1 TLP HMM and HBM results for product I

	Stress mode	V_h (V)	R_{on} (Ω)	I_{TLP} (A)	HMM passing voltage (kV)	HBM passing voltage (kV)
Pin_1	Positive	2.86	0.88	20	8	8
Pin_2	Positive	2.6	0.78	20	8	8
Pin_3	Positive	2.85	0.61	20	8	8
Pin_4	Positive	2.5	0.61	19	8	8
Pin_1	Negative	-2.5	-0.8	-20	-8	-8
Pin_2	Negative	-2.3	-0.72	-20	-8	-8
Pin_3	Negative	-2.3	-0.58	-20	-8	-8
Pin_4	Negative	-2.4	-0.56	-16.8	-8	-8

The second product is a signal conditioning amplifier for infotainment automotive applications. This product has four amplifier input pins (1-4) and two ground pins (Vss) directly connecting to the car cable harness. Figure 2-5 shows the schematic representation of the amplifier input circuit. The amplifier inputs would be seeing the high stress in this case and the protection is connected between the input pin and the Vss.

In this product, we also performed the TLP ESD characterization first. During the test, we have noticed that there are abrupt holding voltage change during the 4.5A current level. Around that current level, the leakage did not changes. By only look at the leakage current, this

pin of the product II has reaches the 20A, the system limit, without any changes in the leakage current. However, the results from the separate product team has showing much lower failure current, besides from the results of the product I indicates that the leakage is not a reliable source to identify the failure. We have decided to run multiple times of the TLP on this pin of product II to check other parameters such as the trigger voltage and holding voltage instead of the leakage current.

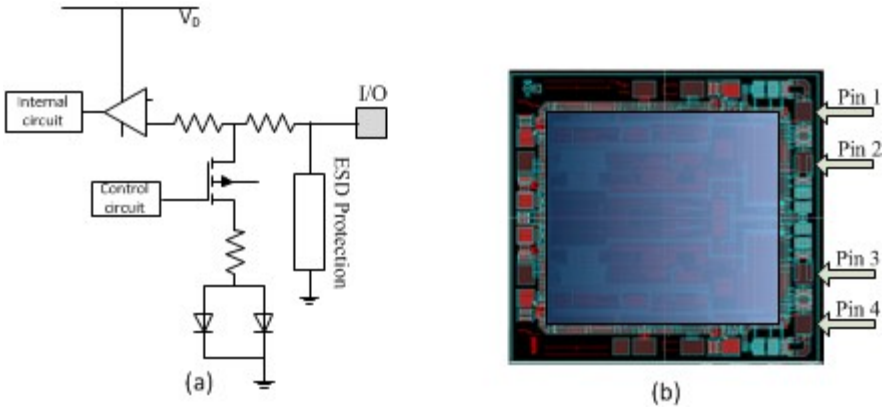


Figure 2-5 (a) Simplified schematics of input interface of an automotive amplifier (Product 2) and (b) Top-level layout view

Figure 2-6 shows an example of multi-times TLP test before 4.5A current level and after. The first TLP test has been stopped at the 4.5A before the abrupt changes in the I-V curve; then the second test showing the consistency of the trigger voltage, holding voltage and on resistance indicates that this pin of the product II does not fail. Then we have keeps the tress increasing until we have saw that abrupt I-V changes around 5A current level. After that we have performed the third test on the same pin of this product II. The I-V curve of the third time TLP test showing

the changes of the trigger voltage and also the holding voltage (green curve). With the 3 set of TLP test, we can confirms that the failure current of this pin of product 2 is at 4.5A. However, the leakage does not show any changes. And the summary of the characterization accurate data is shown in Table 2-2.

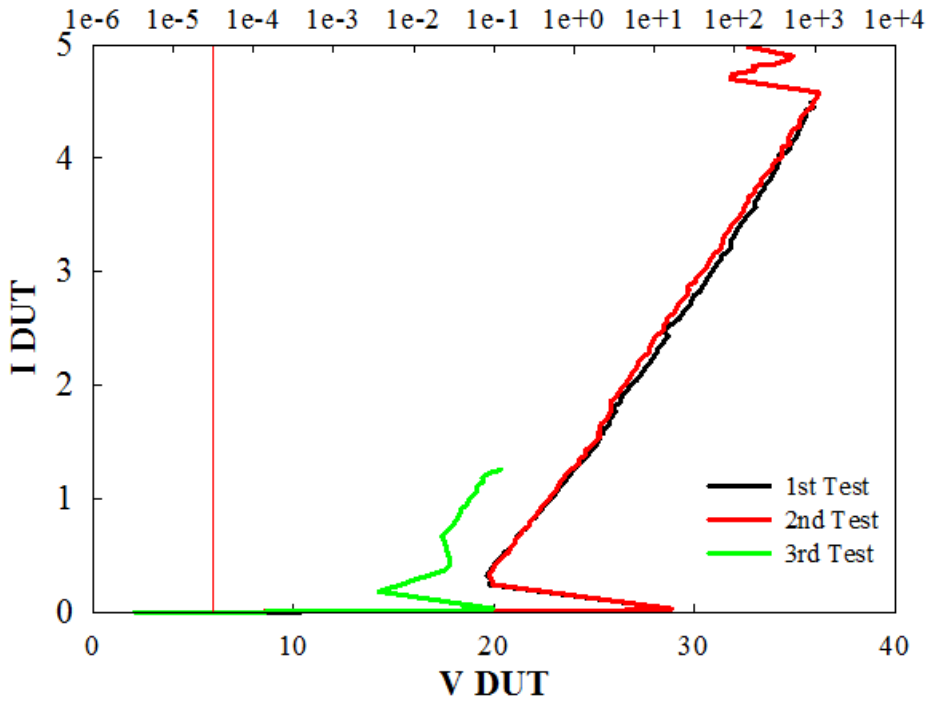


Figure 2-6 TLP result from on Pin of Product II

Due to the complexity of the current path inside the product, the leakage can be changed by the potential charge storage at some part of the product, such as a capacitor, turns-on during the test. It also can be very large in some cases. Without the functional testing after the product packaging, it brings more difficulties to evaluate the ESD performance of a product at wafer level.

Table 2-2 TLP HMM and HBM results for product II

	Stress mode	V_h (V)	R_{on} (Ω)	I_{TLP} (A)	HMM passing voltage (kV)	HBM passing voltage (kV)
Pin_1	Positive	20	3.5	4.3	2.8	8
Pin_2	Positive	20	3.9	4.3	2.8	8
Pin_3	Positive	19.7	3.9	4.3	2.8	8
Pin_4	Positive	19.8	3.5	4.3	2.8	8
Pin_1	Negative	-11.4	-1.82	-5.5	-2.8	-8
Pin_2	Negative	-11.6	-1.8	-5.5	-2.8	-8
Pin_3	Negative	-11.5	-1.84	-5.5	-2.8	-8
Pin_4	Negative	-11.5	-1.94	-5.5	-2.8	-8

2.4 New methodology to overcome the conventional limitation

Monitoring the trigger voltage and holding voltage by running TLP multi-times at different current level can be used to identify the failure for a product at the wafer level. However, in a product at the wafer level, designers are more interested in the system-level ESD performance, which is the HMM passing level. Currently, none of the test module has been offer the other failure detection methodologies other than the leakage evaluation. We have performed the HBM/HMM characterizations on the Hanwa system, however during the standard testing procedure it offers in the system, all of them are failed to identify the correct passing level. Due

to the complexity of the product design, certain level of ESD stress can turns on some part of the product and stays in that way during the characterization, especially for the power-off ESD characterization, and some of them might have too large leakage current, and cannot shown any leakage changes after the failure. Two product from the previous section has demonstrated that the only using the leakage evaluation can brings some inaccuracy to the characterization results.

In order to address the above-mentioned issues of failure identification in products subject to the HMM stress at the wafer-level, this work introduces a new method in which a reference transient voltage waveform is first selected as the initial benchmark, and the post-stress transient waveforms are then measured under the same reference stress condition and compared against the reference waveform. Figure 2-7 shows the flowchart of this testing method. The first step is to measure and capture the voltage waveform at an IC pin subject to a reference stress level, for instance 200 V HMM. Second, increasing in steps the HMM test voltage starting from the reference stress. In line with the description in the IEC 61000-4-2 ESD standard, 15 zaps are used at each stress level. After each stress step, the IC pin is tested at the reference stress level again, and the resulting transient waveform is compared against the original benchmark waveform to determine whether a failure has occurred. Note that this reference waveform is obtained when stressing the I/O pin of a product (standalone protection device together with core circuit). Even though the voltage waveform taken from a standalone ESD protection clamp can be considered as a reference waveform, it would not be practical in the following three aspects: 1) It would require the fabrication of standalone ESD protection devices in addition to the products, which is highly dependent on the development stage and it is not always viable with the product reticle mask set; 2) it would add extra testing time and would not necessarily be the same as the

reference waveform obtained at the I/O pin; 3) it does not account for the loading effect and effective device plus core circuit reaction to the HMM stress.

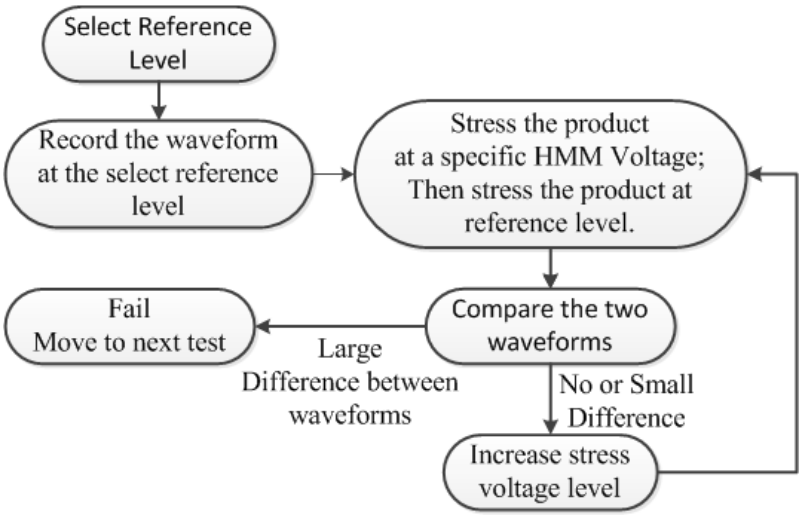


Figure 2-7 Flowchart of the new HMM testing method.

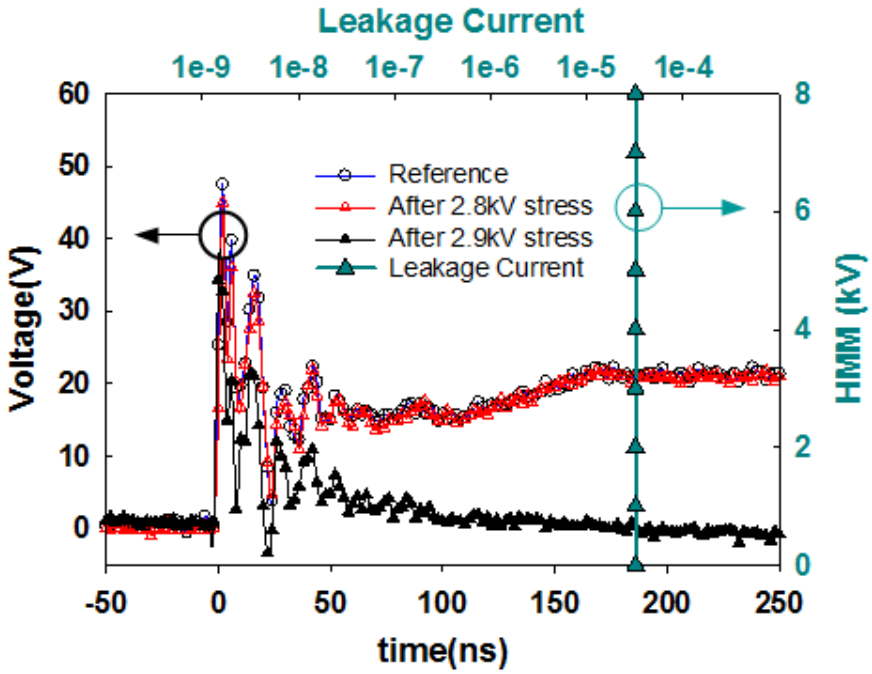
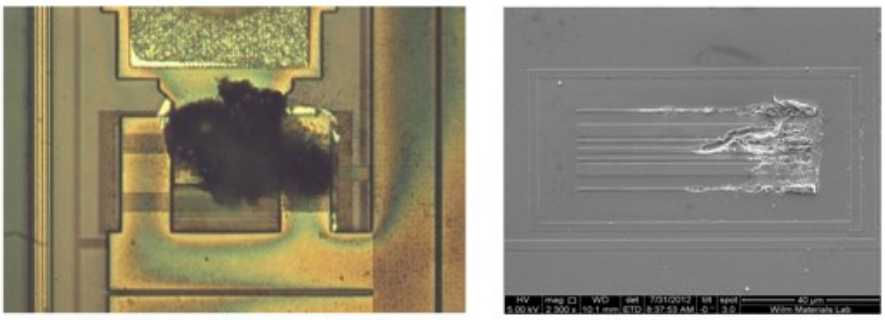


Figure 2-8 Voltage waveforms of Product 2 measured at the reference stress level of 200 V without additional stress (reference), with 2.8 kV stress (pass), and with 2.9 kV stress (fail). Post-stress leakage currents obtained from the conventional leakage current method are also included.

Figure 2-8 shows the voltage waveforms at the input pins of Product 2 (see Figure 2-5) measured at the reference HMM voltage of 200 V without additional stress and measured at the reference HMM voltage of 200 V after subjecting to two HMM stress voltages of 2.8 and 2.9 kV. The blue curve is the waveform resulting from the reference stress level of 200 V, and the red curve is the waveform measured at the reference level of 200 V after 2.8 kV HMM stress. No change over the reference waveform is found and the product is undamaged after the 2.8 kV stress. As the stress level is increased to 2.9 kV, however, a drastic drop in the voltage waveform (black line) at the reference stress level compared to the reference waveform is observed, suggesting that the product has failed. The post-stress leakage currents are also shown in the figure, and such a current does not change after the product has failed at 2.9 kV and beyond. This indicates that the conventional leakage current approach is invalid for the detection of product failure. To prevent possible charge accumulation effect, each pin was grounded before and after the testing. Furthermore, 1 sec was used as the interval time between zaps and 10 sec bet

ween stress levels. A failure analysis was also conducted, and the optical and Scanning Electron Microscope (SEM) images shown in Figure 2-9 confirm that a hard failure took place at a stress level of 2.9 kV.



Optical image of damage point

A SEM image of damage point

Figure 2-9 Images obtained from failure analysis of Product 2 subject to a HMM stress of 2.9 kV

Figure 2-10 compares the reference and post-stress voltage waveforms measured at the interface pin of Product 1 (see Figure 2-3). The post-stress leakage currents measured are also included in the figure. The product is stressed with a maximum HMM voltage of 8 kV. Comparing the resulting waveform with the benchmark (reference) waveform it maybe concluded that the product does not fail at such a stress condition. On the other hand, the conventional leakage current method suggests a drastic change in the leakage current, which can be erroneously interpreted as a product failure at 2 kV.

To further verify the impact of ESD stress on the core circuit, we have tested the same products using the conventional IEC table/gun setup and measured the products' post-stress functionality on an automatic tester to determine the HMM failure voltages. Before reaching the passing levels (i.e., 2.9kV for Product II), there was no product-level degradation or malfunction. In addition, our failure analysis has indicated that the failure took place in the junction, not the oxide. Based on these observations, we can rule out secondary effects, such as the charged device model (CDM) like damages resulting from voltage overshoot. The data is summarized in

Table 2-3. It can be seen that the failure voltages obtained from the new method and the IEC gun testing agree to each other, but the data obtained from the conventional leakage current method show a large discrepancy.

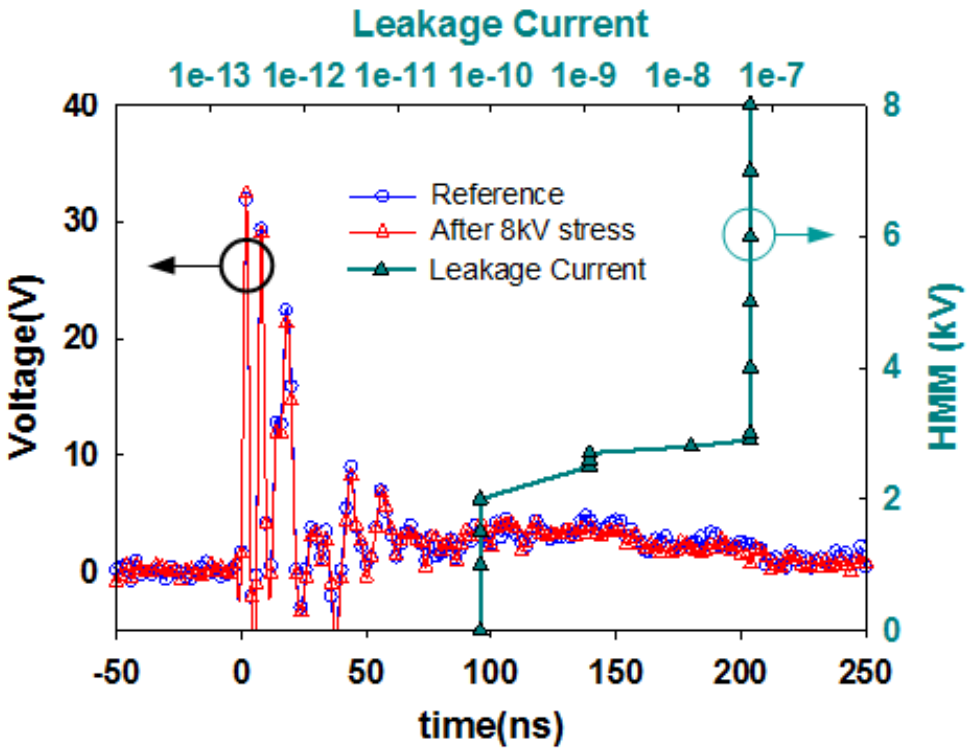


Figure 2-10 Voltage waveforms of Product 1 measured at the reference stress level of 200 V without additional stress (reference) and with 8 kV stress (pass). Post-stress leakage currents obtained from the conventional leakage current method are also included.

There are a few intrinsic assumptions in the methodology presented. They include: 1) the waveforms generated under each stress must be identical; 2) the testing setup should allow for capturing the waveforms under the stresses and 3) the reference stress selection criterion were developed based on two products under study illustrating common interfaces in IC applications. HMM characterization of IC applications departing from the discussed schemes may require

defining different reference stresses. There are a few intrinsic assumptions in the methodology presented. They include: 1) the waveforms generated under each stress must be identical; 2) the testing setup should allow for capturing the waveforms under the stresses and 3) the reference stress selection criterion were developed based on the two products under study illustrating common interfaces in IC applications. HMM characterization of IC applications departing from the discussed schemes may require defining different reference stresses.

Table 2-3 HMM passing levels obtained from different characterization methods

	Leakage current method (kV)	New voltage waveform method (kV)	ESD gun with functionality testing (kV)
Product 1, Pin 1	2	8	8
Product 1, Pin 2	2	8	8
Product 2, Pin 1	8	2.8	3
Product 2, Pin 2	8	2.8	3

From the preceding analysis, it becomes obvious that the selection of a suitable reference stress level is very critical for the newly developed methodology. Such a reference stress can neither be too large to damage the IC nor too small to hinder the observation of the device's normal functionality. The criteria of selecting the correct reference stress level are as follows. First, it must be significantly below the targeted ESD protection level and does not trigger the parasitic path. Second, it must be able to turn the device on so that its full response to this reference stress can be clearly observed. Third, it should generate a distinct and detectable

difference between the reference and failure waveforms. Summarizing the above requirements, we have concluded that the lowest stress level that can fully turn on the device and be captured by the instrument is the suitable reference stress level.

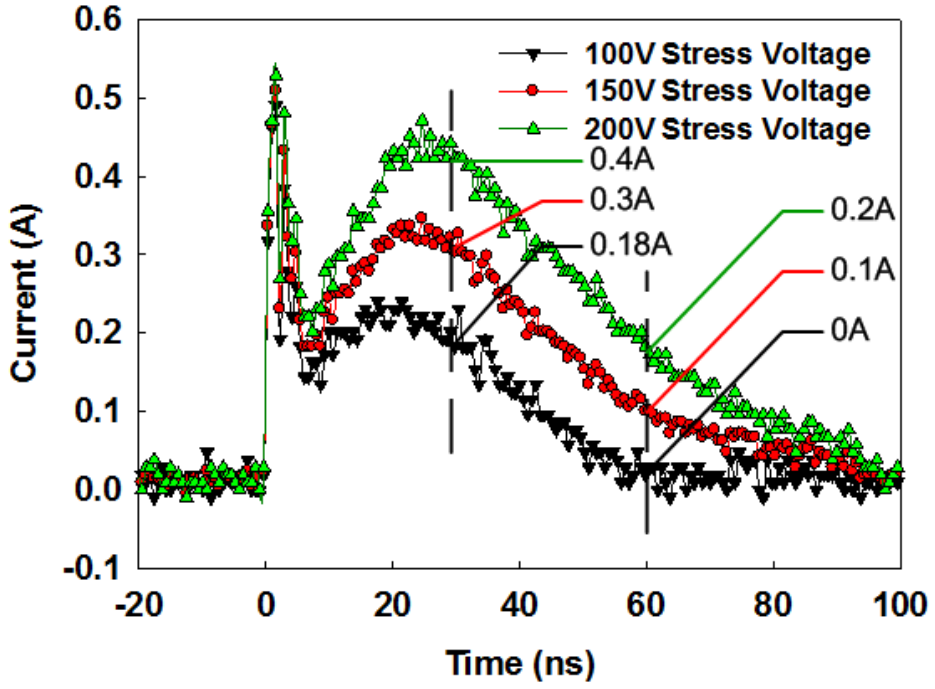


Figure 2-11 Current waveforms of Product 1 subject to HMM stressing voltages of 100, 150 and 200 V

Shown in Figure 2-11 are the current waveforms of Product 1 subject to 100, 150 and 200 V HMM stresses. According to the IEC61000-4-2 standard, a typical way to determine the device's turn-on is to see if the current at 60ns is at least half of the current at 30ns. Such a condition is not satisfied under the 100 and 150 V stresses, as can be seen from the results in Figure 2-11, suggesting that these two stress voltages are unable to fully show clamping characteristics at the product I/O pin. On the other hand, the device is fully operational under the

200 V stress, and such a stress voltage can be used as the reference stress level. Note that the 200 V reference stress level is specific to Products 1 and 2 under test. The reference selection criteria were developed based on the two products under study, and its wide applications to a large number of different products require further verifications. The new methodology does offer an effective way to characterize the HMM ESD performance at the product-level when the conventional evaluation based on the observation of leakage current is not viable.

This method has also been verified using the standalone device and compare to conventional DC leakage measurement to see whether the results is matching with using normal DC as a identification. The Figure 2-12 shows the results from the characterization that the DC leakage changes after failure and at the same time, the voltage waveform changes also at different time window. It also being verified at different devices and this method can match the DC leakage measurement results without any problem.

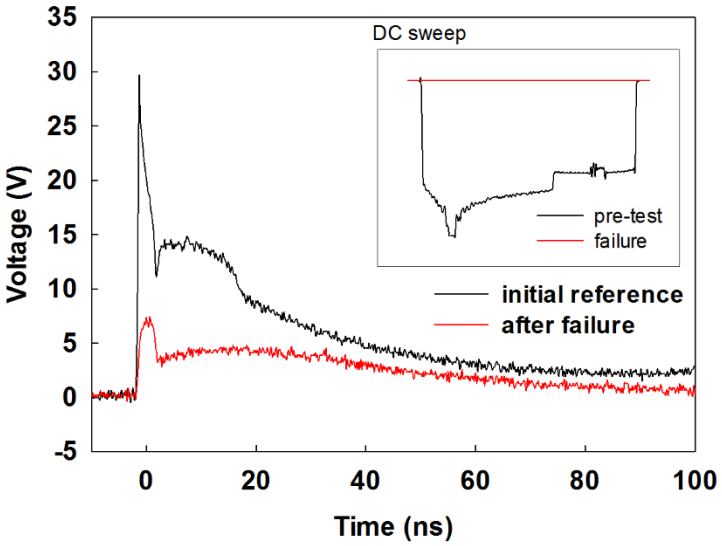


Figure 2-12 Accuracy against DC leakage method

2.5 Reference stress level

For a high holding voltage device, the 200V to 500V reference level can be used as the reference stress level. But the accuracy for them will be different, especially for the device that has low holding voltage (<10V). The voltage waveform of those devices will have a very flat and low level after 30ns in of the Figure 2-13. And the error rate maybe varies for different reference level at different time window. So an investigation of the best stress reference stress level between 300V to 600V has been done.

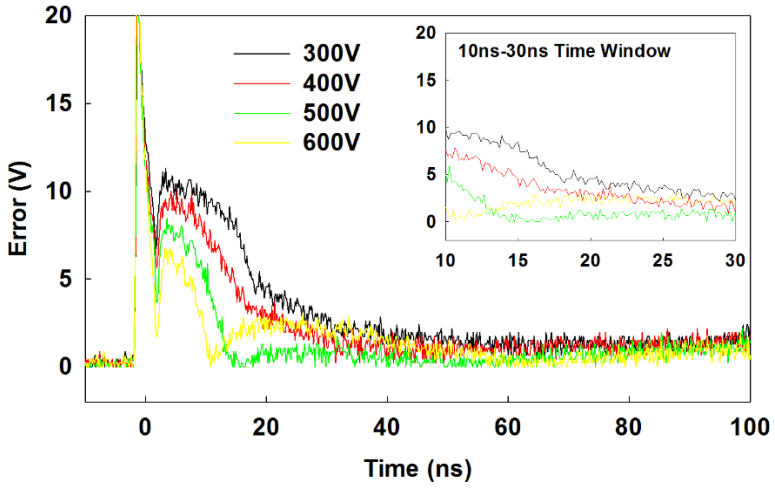


Figure 2-13 : Error for different reference stress level

In this case, we are using a low holding voltage device, which will be more difficult to detect the failure because of the lower holding voltage at 30ns to 100ns window. And in that time period, due to the system noise and it will give a lower error rate. As we can see from Figure 5, the error at the time window between 30ns to 100ns is low when the device has low holding

voltage. From 0ns to 30ns, it has larger error rate. But between 0-10ns window, the noise is large and different across different instrument, that region may varies between different stress. For this situation, we need look into the more stable time window, between 10ns to 30ns. And 300V during that window it shows the largest error rate and also can gives cleaning waveform for identifying the failure. Overall, the selected 300V reference level is the optimal across this research work.

2.6 Conclusion

A new and improved testing framework has been introduced for assessing the HMM robustness of a product at the wafer-level. By using a suitable HMM reference stress voltage, a benchmark voltage waveform was first generated. HMM post-stress voltage waveforms were then measured and compared against this benchmark waveform. The product was considered damaged when there was a notable difference between the post-stress and benchmark waveforms. The guideline for selecting a suitable reference stress level was also developed and discussed. Two different products were tested using the new testing method and the conventional leakage current method, and the results were verified against those obtained from the IEC standard testing. It was found that the new method and IEC testing yielded consistent failure voltages, whereas the conventional leakage current method produced erroneous failure detection.

CHAPTER 3 DESIGN OF HIGH VOLTAGE DEVICE IN LOW VOLTAGE PROCESS

3.1 Introduction

Integrated circuits (ICs) for emerging high performance precision data acquisition and transceivers in industrial, automotive and wireless infrastructure applications require effective and robust electrostatic discharge (ESD) protection solutions. These circuits, with relatively high operating voltages at the I/O pins, are increasingly being designed in low voltage CMOS technologies to meet the requirements of low cost and large scale integration. For example, a CMOS simultaneous sampling analog-to-digital data acquisition system (DAS) is required to have interfaces operating at a high bipolar voltage in the range of ± 20 V. ESD protection structures for these circuit applications must also be integrated on-chip and fabricated using the same technology. An attractive ESD protection device for input/output (IO) interface applications is the silicon controlled rectifier (SCR) because of its high robustness and flexibility [41]. But the trigger voltage or blocking voltage, of an SCR is governed by the breakdown voltage of the reverse biased p/n junction between the terminals of the SCR. Such a blocking voltage is constrained to a relatively low level when the SCR is fabricated in a low voltage CMOS technology. This shortcoming has traditionally made it unfeasible to integrate a high-voltage I/O ESD protection in low voltage CMOS-based ICs.

In this chapter, a new dual-polarity SCR optimized for high bidirectional blocking voltages, high trigger current and low capacitance is realized in a sub 3-V, 180-nm CMOS process. This ESD device is designed for a specific application where the operating voltage at the

I/O is larger than that of the core circuit. For instance, protecting high voltage swing IOs in CMOS DAS applications. In this reference application, an array of thin film resistors voltage divider is directly connected to the interface pin, reducing the maximum voltage that is obtained at the core device input down to ± 1-5 V. Its ESD characteristics, including the trigger voltage and failure current, are compared against those of a typical CMOS-based SCR.

3.2 Design and layout

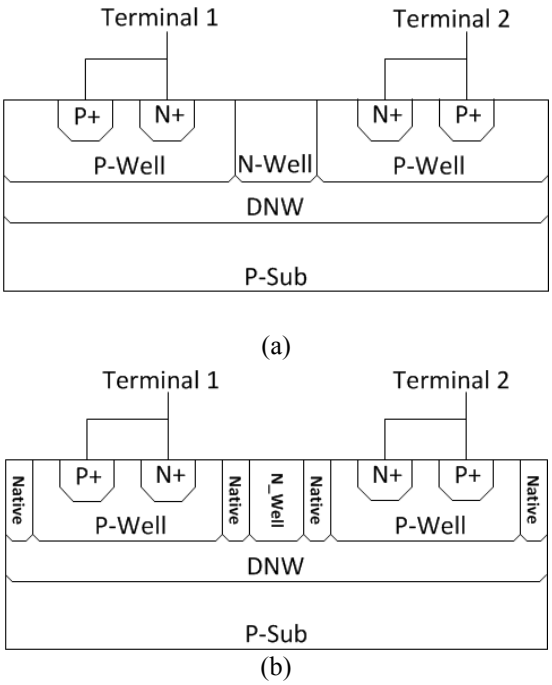


Figure 3-1 (a) Conventional bidirectional SCR (Device 1) and (b) proposed bidirectional SCR (Device 2) fabricated in a 180-nm CMOS technology.

Figure 3-1(a) shows the cross-sectional view of a typical bidirectional SCR device fabricated in a 180-nm CMOS process. There are two interacting SCRs embedded in the structure in Figure 3-1(a). When terminal 1 is subject to a positive-polarity ESD stress, the p-n-p-n structure turns-on and a conducting path is created from terminal 1 to terminal 2. On the other

hand, when terminal 2 is subject to a positive-polarity ESD stress, the p-n-p-n structure turns-on and another current path is created from terminal 2 to terminal 1 [41]. In both cases, the reverse biased P-Well/N-Well junction serves as the blocking junction, and the breakdown voltage of such a junction determines the trigger voltage of the SCR. Due to the relatively high doping concentration in the P-Well and N-Well regions for low voltage CMOS applications, P-Well and N-Well regions peak doping concentration at the surface are ~ 3-8 x 1017cm-3 and junction depth ~ 0.5-1 μm, the P-Well/N-Well junction breakdown voltage is relatively low, in the range below 15 V. As a result, high blocking voltage SCR ESD devices are traditionally implemented using high voltage CMOS or BCD (Bipolar-CMOS-DMOS) processes, in which lightly doped regions are available to realize relatively large voltage blocking junctions [41].

To enable high-voltage tolerant IOs in low voltage CMOS processes, Figure 3-1(b) shows a new SCR-type protection device with a high dual-polarity blocking voltage. The new SCR incorporates an additional logic operation step in masking generation to create the native buffer regions without incurring in extra cost. The native buffer region is commonly used in the metal-oxide-semiconductor field-effect transistor (MOSFET) to control the transition between the enhancement and depletion modes. This native buffer region is introduced as part of the N-Well and P-Well mask logic operation, to allow blocking of both, the N-Well and P-Well, where this native buffer layer is defined. Thereby, if the native layer is drawn inside the deep N-Well (DNW), it is possible to obtain a native lightly doped N-type buffer region, and if this is drawn outside the DNW, a native lightly doped P-type buffer region is obtained. The native substrate doping is ~ 0.8-3x$10^{14}$$cm^{-3}$ and the native DNW region is ~ 4-9 x$10^{14}$$cm^{-3}$ at the surface, with the peak doping concentration of ~ 0.8-2 x$10^{17}$$cm^{-3}$ located ~ 1.2-2 μm away from the surface. Upon

introduction of the native region, the net doping concentration at the metallurgical junction drops by over an order of magnitude.

The native buffer region (Native in Figure 3-1 (b)) is a lightly doped N-type region defined by the background DNW doping. Adding this region creates a higher blocking voltage for ESD protection purposes. Similarly, a high isolation blocking voltage from the DNW to substrate is achieved by introducing an extra native region in the periphery of the device in Figure 3-1(b). The length of the native regions is 1 um, which is the minimal layout design rule for reliable manufacturing. The P-Well/native-buffer junctions allow the creation of high voltage blocking junctions in the SCR structure; hence a relatively large dual trigger voltage in excess of ±20 V is achieved.

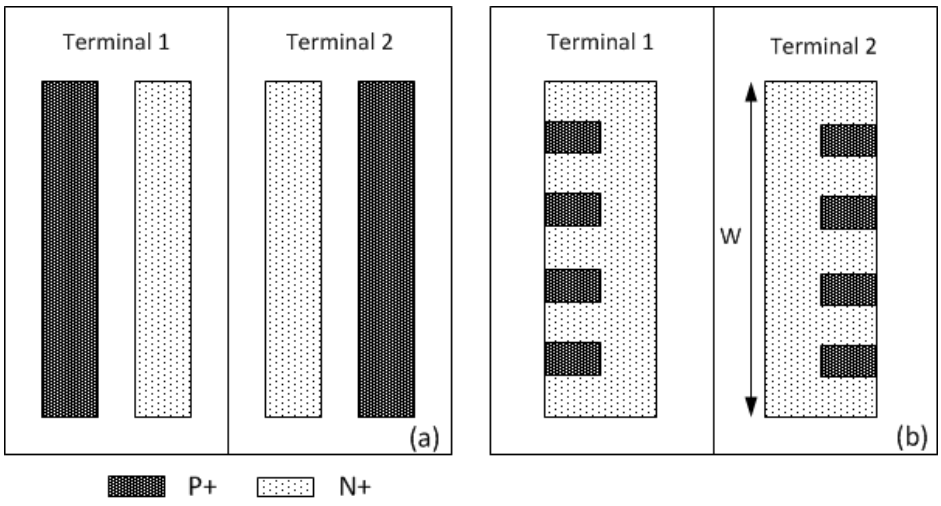


Figure 3-2 Bi-directional new SCR with (a) traditional p+/n+ stripe topology (Device 1 and 2) and (b) p+/n+ T-island topology (Device 3).

Besides the introduction of the native buffer region, additional optimization in the SCR's trigger current and capacitance is achieved by engineering the active region definitions [44]. The

n+ and p+ active regions of the SCR are typically drawn in a rectangular stripe array, as shown in Figure 3-2(a). An n+/p+ T-island topology was proposed to better control the SCR I-V characteristics and turn-on speed, in particular for ESD protection of automotive IC's [44]. This modification in the active regions does not affect the DC breakdown of the device. Such an approach is implemented in the proposed SCR with the native buffer regions in Figure 3-2(b), thereafter denoted as Device 3.When Device 3 is triggered, the active T-island topology leads to a lower emitter injection efficiency, longer base transient time, and lower hole mobility, thus resulting in a lower PNP current gain to better control the device turn-on characteristics [44].

3.3 Results and discussion

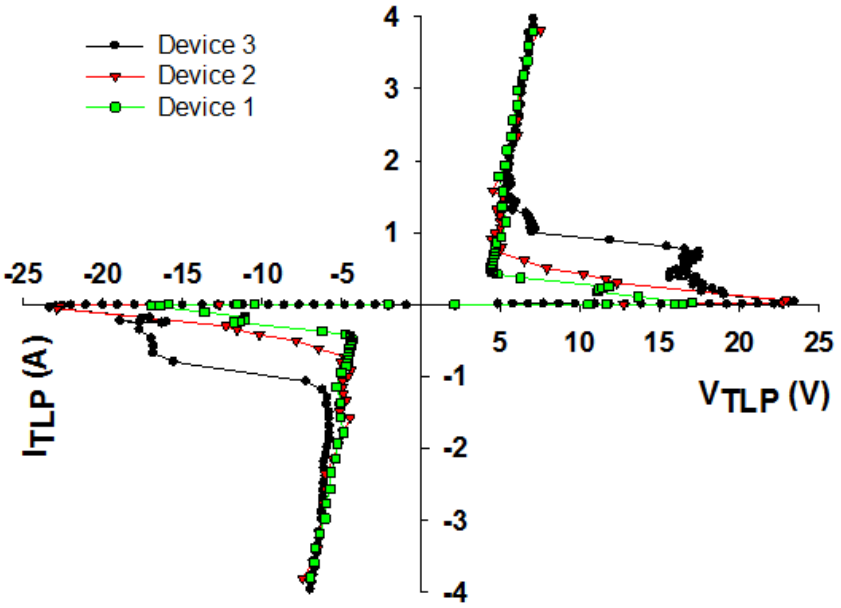


Figure 3-3 TLP I-V characteristics of conventional SCR (Device1) and new SCRs having the conventional stripe topology (Device 2) and T-island topology (Device 3).

The measured TLP I-V characteristics of the traditional (Device 1) and new (Devices 2 and 3) SCRs are shown in Figure 3-3. The new SCRs can offer 21V DC breakdown voltage (BV) compare 15V BV for the Device 1. In line with the DC BV difference, a high trigger voltage of about 24 V, compared to about 16 V of its traditional counterpart. The lightly doped native buffer regions inserted between the P-Well and N-Well regions (see Figure 3-1(b)) substantially increase the range at which this device can operate.

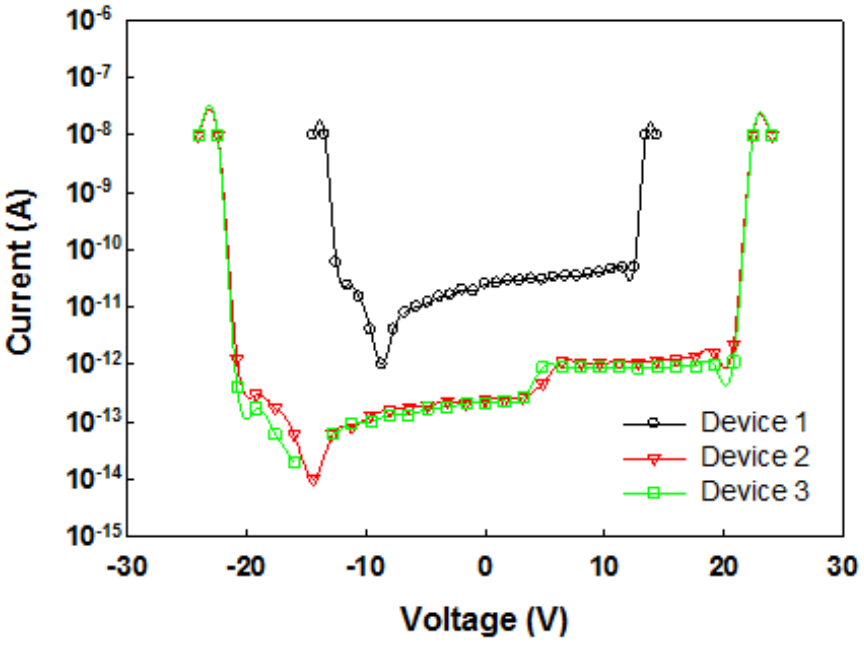


Figure 3-4 DC characteristics for Devices 1, 2 and 3.

The TLP I-V curve of the new SCR (Device 3) with the T-island topology is also included in Figure 3-3. The trigger voltages of Devices 2 and 3 are very similar, but Device 3 shows two NPN-enhanced trigger points, with the second triggering condition taking place at a much higher trigger current. Notice that the high trigger current of 1A aids avoiding an unintended latch condition in the worst case of a miss-triggering condition in the protection

clamp, as the interface pin operating current applications such as DAS are typically less than 100 mA. The ESD current handling capability trade-off of Device 3 is lower than Device 2, about a 40% drop in TLP current to failure (It2), due to the reduction in the SCR action by lowering the PNP current conduction capability. For cases in which an even higher holding voltage is required; this is achieved in this device by inverting the definition of the n+ and p+ T-island active regions in Figure 3-2.

Table 3-1 ESD Performances of Three Different SCR's

	V_T (V)	I_T (A)	V_H (V)	It2 (A)	W (um)	$I_{leakage}$ (A) @25°C	$I_{leakage}$ (A) @125°C
Device 1	16	0.1	4.5	8.5	85	5e-11 @10V BV=14V	1e-8@10V BV=16V
Device 2	24	0.2	5	7	85	1e-12 @10V BV=21V	5e-9@10V BV=22V
Device 3	24	1	5.5	4	85	9e-13 @10V BV=21V	3e-9@10V BV=22V

Table 1 summarizes the characteristics of Devices 1, 2 and 3. Notice that the native buffer regions in combination with the active T-island topology allows for the most optimized structure and lower standing leakage current. The DC characterization is performed using 1ms rise time voltage waveform, the results is shown in Figure 3-4. The SCRs were stressed with a relatively large rise time of 1 ms square-shape voltage waveform, emulating conventional power-up conditions. The devices exhibit relatively small conduction current, except when the stress

voltages are beyond the breakdown voltage. During the normal circuit operation, the interface signal voltage swing remains within ±20 V. Under this condition, the Device 3 with a trigger voltage of 22V has been confirmed not prone to false triggering. Notice that the ~ 1 A holding current is higher than the interface circuit driving current (~100 mA), further preventing the device from entering a latch-up condition in a worst case miss-triggering condition.

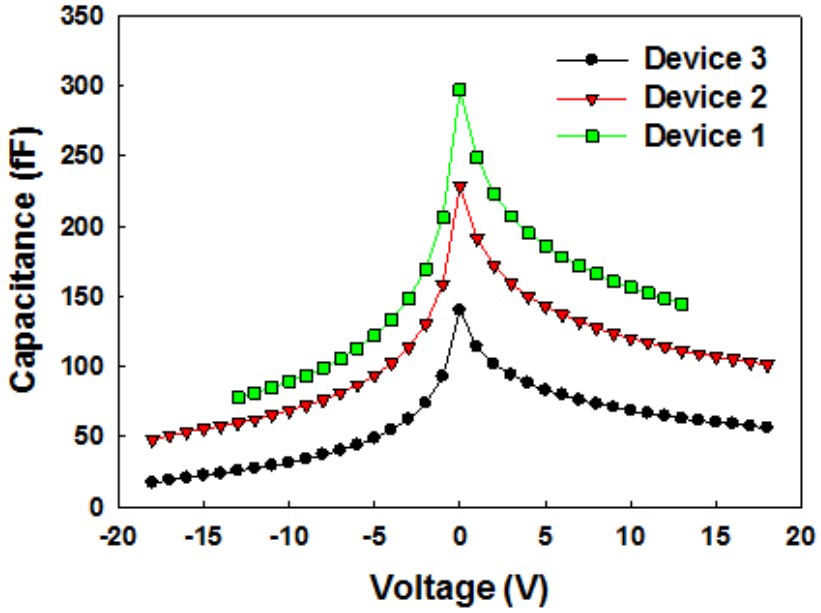


Figure 3-5 Capacitance-voltage characteristics for Devices 1, 2 and 3.

Another consideration in the optimization of the ESD protection design for communication interface applications is the minimization of capacitance associated with the SCR. Reducing the ESD parasitic capacitance is required for the development of an effective ESD protection solution is higher speed and low noise communication interface in mixed-signal IC's [23]. Figure 3-5 shows the C-V capacitance characteristics of Devices 1, 2 and 3. The data demonstrates in one hand that the native buffer regions added in the SCR reduces the SCR's

capacitance by about 23% (300 fF vs. 230 fF). This is because the presence of the native buffer regions widens the space charge region associated with the blocking junction. Furthermore, the T-island topology decreases to a larger extent the forward-biased capacitance and increases to a less extent the reverse-biased capacitance, consequently making the overall junction capacitance smaller. On the other hand, comparing Device 2 to Device 3, the capacitance is further reduced by about 40% with the use of the T-island topology, making it an optimum structure for enabling robust high voltage-tolerant precision communication interfaces in emerging data communication CMOS applications.

Since a trade-off was identified between the parasitic capacitance and the ESD performance, Table 3-2 shows the ratio between capacitance and the maximum It2, Cn=C/It2. Notice that the Cn ratio is comparable in the three devices, confirming minimum impact of the Device 3 optimization on this ratio.

Table 3-2 Figure-of-merit (FOM) of three different SCR's

	Device 1	Device 2	Device 3
Cn (fF/A)	35.3	32.9	35

3.4 Conclusion

A silicon controlled rectifier (SCR) can often be designed for high voltage interface ESD protection applications fabricated in high voltage processes, such as high voltage CMOS or BCD processes. In a standard low-voltage CMOS technology, however, integration of ESD devices to protect high-voltage tolerant communication interfaces is challenging because of the

fundamental junction breakdown voltage limitations. A new bidirectional SCR fabricated in a low-voltage, 180-nm CMOS process was developed for enabling the ESD protection of high-voltage-tolerant communication interface pins. The SCR high trigger voltage was successfully achieved by selectively defining and adding native-buffer regions in the device. The new SCR offered a high trigger voltage up to 24 V. When a T-island active-region topology was implemented, the proposed SCR, in addition to the high trigger voltage, yielded a highly desirable high trigger current of over 1 A and the low parasitic capacitance.

CHAPTER 4 DESIGN OF IN-SITU ESD PROTECTION STRUCTURE FOR VARIABLE OPERATING VOLTAGE INTERFACE APPLICATIONS IN 28-NM CMOS PROCESS

A multiple discharge-paths electrostatic discharge (ESD) cell for protecting input/output (IO) pins with a variable operating voltage (0.5 to 3.5 V) is presented. This device is optimized for low capacitance and synthesized with the circuit IO components for in-situ ESD protection in communication interface applications developed in a 28-nm, high-k, metal-gate CMOS technology.

4.1 Introduction

With the advancement of high-speed and low-cost mixed-signal CMOS circuits, the viable implementation of multi-gigabit communication systems-on-a-chips are getting closer in sight [46]. Among the challenges for enabling such high performance and multifunctional CMOS systems, achieving very low noise [48] and robust on-chip ESD protection [49] without compromising core performance are particularly urgent and critical [50].

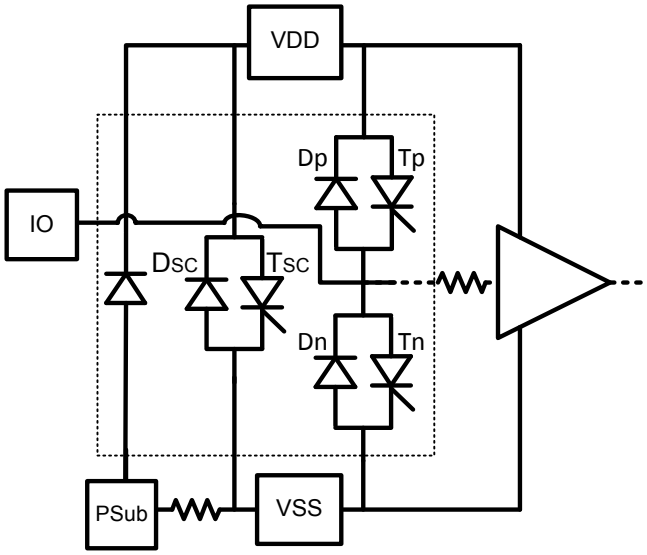


Figure 4-1 Schematic of monolithic Input/Output (IO) ESD protection structure with a built-in supply clamp.

On-chip protection schemes typically follow the conventional approach of using separated components to provide specific discharge paths under an ESD stress [51]. However, relying on this approach to provide robust protection solutions is increasingly difficult in high data rate distributed communication systems [50]. Driven by circuit design optimization factors [46], packaging, proximity between functional blocks and impedance matching constraints, emerging converter applications require more complex layout and routing [50]. Consequently, this restricts the placement of ESD protection components and hence creates a roadblock on the commercialization of these emerging high-speed integrated circuits.

To address the above-mentioned challenge, Figure 4-1 shows a proposed monolithic multiple discharge-paths schematic for ESD protection [50]. It includes an optimized p/n junction structure for providing complementary protection for stress conditions at each of the external pins: VDD, IO and VSS. For example, when the IO pin is subject to a positive/negative ESD stress and VSS is grounded, the Tn/Dn clamps are turned on to discharge the ESD current. As the stress voltage increases, at some point the Dp/Tp clamping components, together with the supply clamp devices DSC/TSC, are also activated to provide a parallel secondary current discharge path. Such an integrated design reduces the spacing between each protection component and minimizes the metal series resistance, thus allowing for a more efficiency and self-contained protection scheme and less proximity restrictions between IO pins and main supply clamps.

The above-mentioned multiple discharge-paths protection cell allows for flexible implementation on various inputs/outputs (IOs), such as those defined in a fan-out wafer-level-

chip-scale-package (WLCSP) [56], and can be adopted for enabling plurality of IO bumps distributed throughout the die surface. This also minimizes the parasitic interconnect associated with the different circuit blocks by relaxing the proximity constrain between the IOs and supply clamps. While the design concept was introduced in, the details and specifics pertinent to its integration and implementation tailored to variable operating conditions in an advanced CMOS technology were not addressed.

This paper builds on the concept described in Figure 4-1 and focuses the attention on the detailed design, optimization and realization of the in-situ ESD protection cell for IO pins with variable operation voltages. By introducing different device configurations fabricated in a 28-nm CMOS process, a greater flexibility in the design options and design trade-offs can be obtained in the proposed topology, thus achieving a higher integration and smaller cell size definition for multi-voltage compatibility interface ESD protection applications.

4.2 Protection cell structure

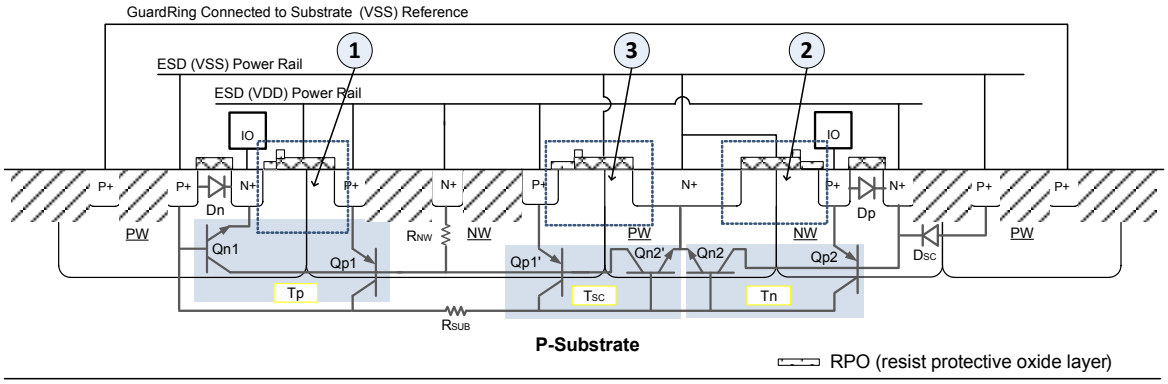


Figure 4-2 Annotated cross-sectional view showing equivalent schematic of the monolithic high-k metal-gate CMOS protection cell

Figure 4-2 shows an annotated cross-section of the IO ESD protection device based on the concept of monolithic in-situ protection shown in Figure 4-1. The corresponding layout footprint of this cell is 12x36 μm^2. Figure 4-3 depicts the layout of three such ESD cells connected in parallel within a common substrate guard ring. The protection cell needs to be segmented in an advanced process such as the 28-nm CMOS technology due to the manufacturing constraints on the maximum metal-gate area. Figure 4-3 shows an example layout top-view of a three segments metal gate device. For characterization of this device topology, a 4-pad configuration is used. The IO and VDD pads are placed on the left side of the layout, while the corresponding VSS pads are shorted and placed at the right side of the layout (see Figure 4-3). This configuration facilitates characterization of the device for the different stress conditions.

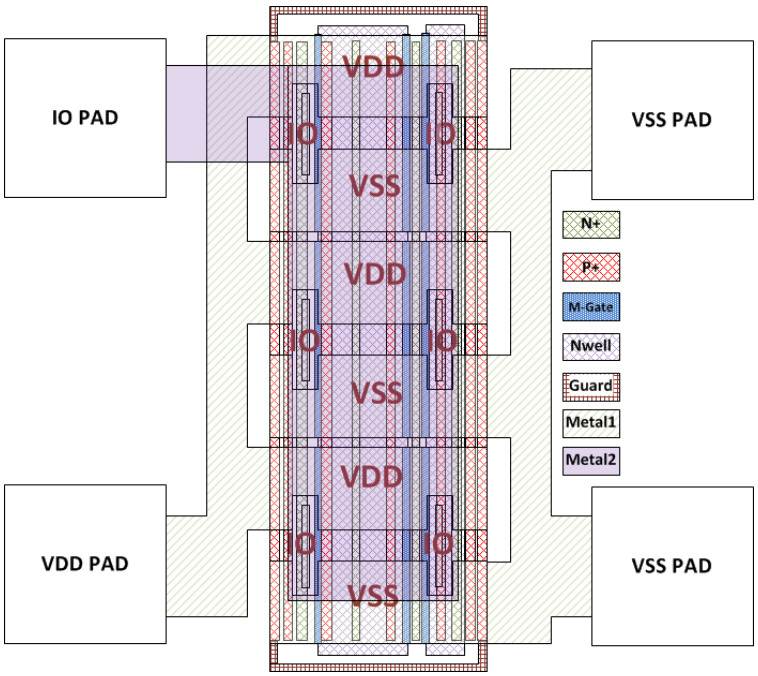


Figure 4-3 Layout view of the monolithic protection device

The cell includes the IO and connectivity to the different power references within the IO domain. A metal gate n-diode (Dn) is formed between the IO and the VSS terminals. A metal gate p-diode (Dp) is formed between the VDD and the IO terminals. The VDD to IO protection path (Tp: Qn1 and Qp1) is formed between the N-well (NW) and P-well (PW) on the left-hand side, the VDD to VSS protection path (Tsc: Qn2' and Qp1') is formed between the left-hand side NW and the center PW. The IO to VSS protection path (Tn: Qn2 and Qp2) is formed between the center PW and the right-hand side NW. This allows for activation of parallel and complementary discharge paths under different ESD stresses from the IO to the power rails. The junctions that control the ESD conduction from VDD to IO and from IO to VSS were labeled as 1 and 2, respectively, and the VDD to VSS ESD protection junction was labeled as 3. Notice that the VDD to VSS (Tsc) structure formation is similar to the one obtained between VDD and IO (Tp). It results in equivalent electrical characteristics and optimization criteria for both of them, Tsc and Tp. By analogy, the following discussion focus on the variations in the structures used for the VDD to IO (Tp) and IO to VSS (Tn) protections.

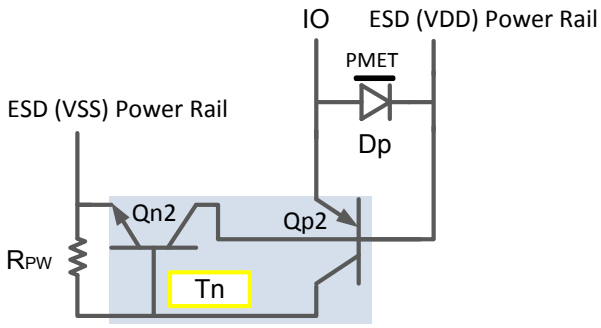


Figure 4-4 Schematic of IO-VSS ESD protection.

Figure 4-4 shows the schematic of the IO to VSS protection. In this case, an SCR exists, with the base of Qp2 connected to the VDD, which is floating during the ESD testing. For the

positive stress from IO to VSS, the voltage drop on the resistance Rpw turns on the bipolar transistor Qn2.

Figure 5 shows four different junction combinations for the IO to VSS protection device, which corresponds to the region labeled as 2 in Figure 4-2. These four blocking junctions allow for different interface operating voltage levels. Figure 4-5(a) depicts the junction formed between the NW and the PW, with the spacing between N+ and P+ region around 0.28 μm. Figure 4-5(b) shows a metal over the NW and PW junctions, with the un-doped/un-silicided regions at one side of the metal gate and a floating N+ inserted to mitigate the standing leakage of the NMOS parasitic formation.

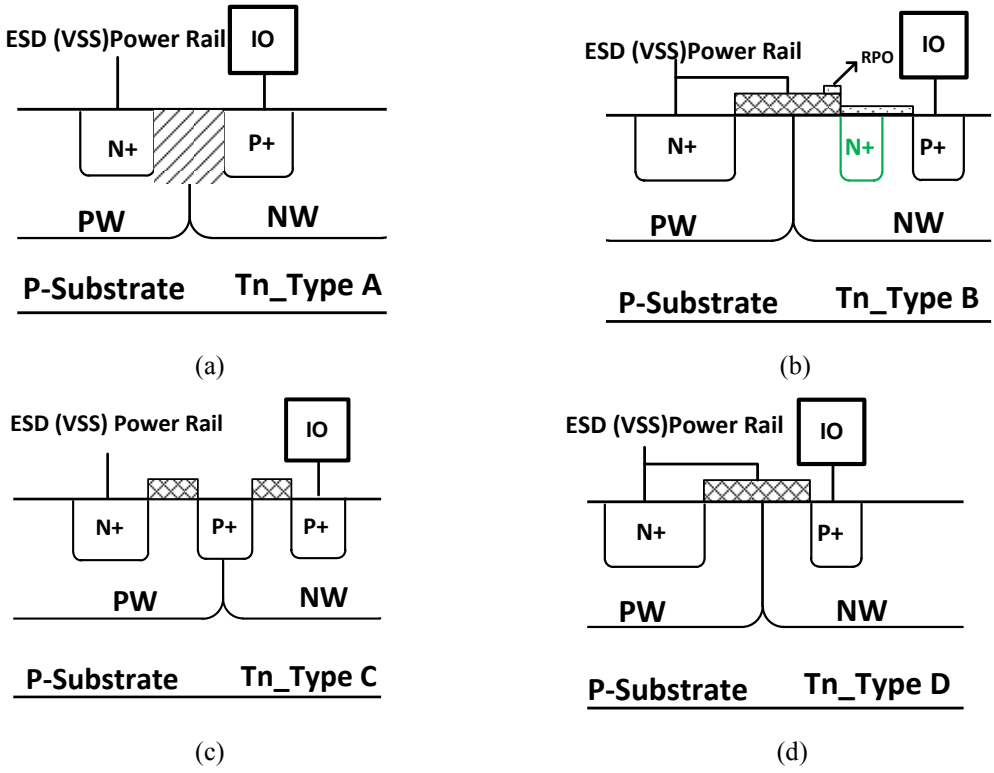


Figure 4-5 Schematic of alternation Tn junction configurations (corresponding to the region labeled 2 in Figure 4-2).

To expedite the protection cell turn-on during an ESD stress, low blocking voltage and high leakage current issues have been reported in 28-nm CMOS-based discrete ESD protection components [52]. This is due to the early MOS-induced conduction between the regions separated by the metal gates. MOS-induced standing leakage is mitigated in this cell by creating un-doped/un-silicided regions (RPO) at one side of the metal gate and selectively defining the metal gate work function.

Figure 4-5(c) has a P+ insert between the NW and PW regions, which gives rise to a lower trigger voltage and faster turn-on compared to the structure in Figure 4-5(a). Figure 4-5(d) has a metal over the junction, aimed for low operation voltage applications. The embedded MOS provides a very low trigger voltage and very fast turn-on speed under a 0.5 V operating voltage condition.

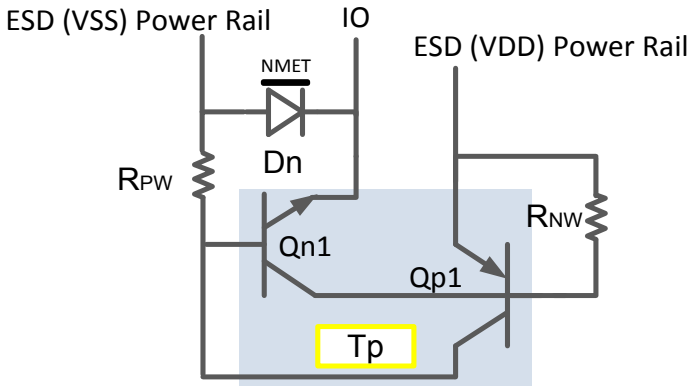


Figure 4-6 Schematic of VDD-IO ESD protection.

Figure 4-6 shows the simplified schematic of the components providing the VDD to IO protection. Different from the protection scheme in Figure 4-4, in this case the base of the Qn1 is connected to the VSS and the base of the Qp1 is connected to the VDD. As a result, when ESD is

coming from the VDD to IO, the base of the Qn1 (Rpw) is floating, which aids in the device turn-on speed during stress conditions.

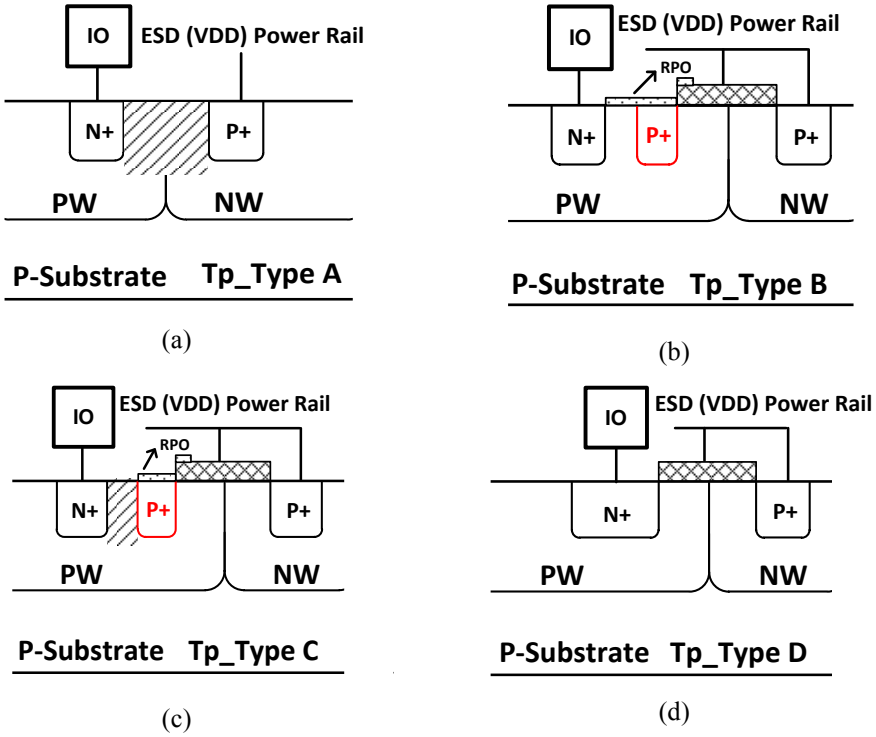


Figure 4-7 Schematic of alternation Tp junction configurations (corresponding to the regionlabeled 1 in Figure 4-2).

Figure 4-7 shows four different junction combinations for the VDD to IO protection device, which corresponds to the region labeled as 1 in Figure 4-2. Figure 4-7(a) shows a high blocking junction formed between the NW and PW regions. Figure 4-7(b) shows a metal over the NW/PW junction with the un-doped/un-silicided regions on one side of the metal gate used to reduce the trigger voltage and also reduce the leakage current. Figure 4-7(c) shows a STI added between the floating P+ insert and the N+ region connected to the IO to further reduce the

leakage current. Figure 4-7(d) shows a metal gate covering the junction to provide a very low trigger voltage and very fast MOS-induced turn-on speed.

4.3 Results and discussion

4.3.1 IO to VSS protection

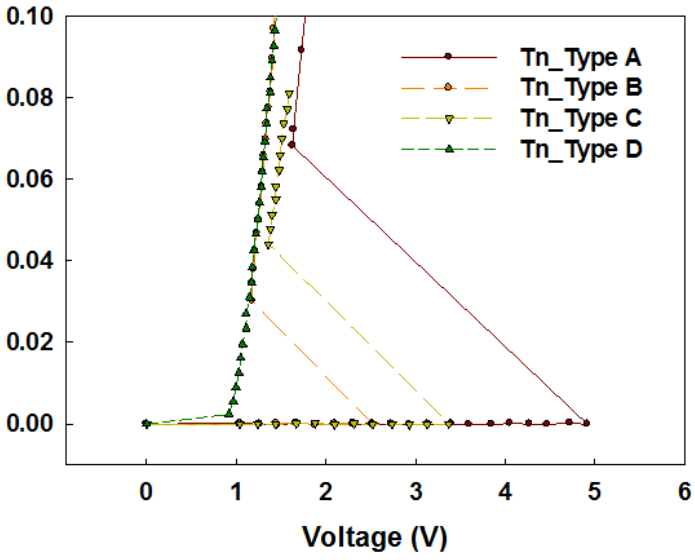


Figure 4-8 TLP performance of different junction configurations for IO- VSS protection

Figure 4-8 shows the TLP measurement results for different formations of the 'Tn' SCR configurations listed in Figure 4-5 (label 2 in Figure 4-1). The 'Tn_Type D' shows the lowest trigger voltage, but the highest leakage current at 0.9 V. For more detailed comparison, Figure 4-9 shows the DC characterization for the different junction formations between -1V and 3V at 25 C. When there is a stress coming from the IO port, the metal gate will form a depletion region on the NW side of the junction. As the stress increases, a channel connecting the P+ and PW regions

will form, thus resulting in a large current flow into the PW region. Further, the large base resistance of the PW region helps turning on the Qn2 and induces the full conduction of the Tn SCR very quickly. The "Tn_Type B" is optimized over the "Tn_Type D" using the un-doped/un-silicided regions on one side of the metal gate and an N+ insert on the other side of the metal gate. A floating N+ region is also added to reduce the NMOS effect by increasing the required stress potential to turn on the embedded MOS. In this case, the trigger voltage is increased and the leakage current is reduced. With the modification of base resistance in configurations B and C using the inserts and the STI, the trigger voltage can further increase. Table 4-1 shows the summarized characterization results for the different device configurations.

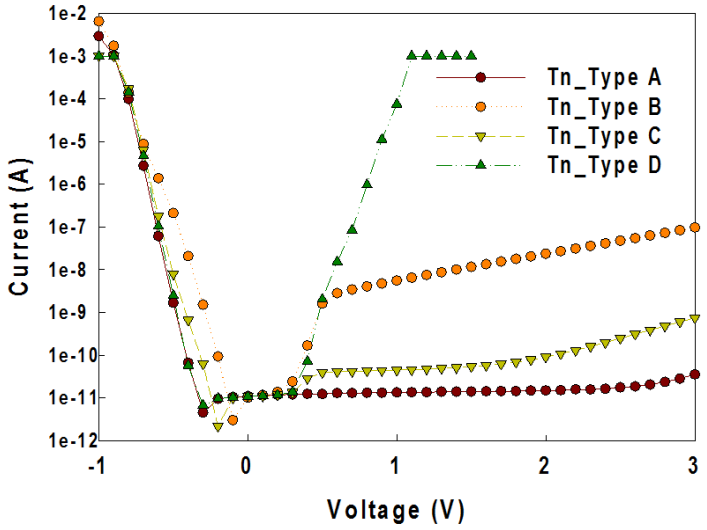


Figure 4-9 DC characteristics of different cells for IO-VSS protection at 25C.

Figure 4-10 shows the DC measurement results for three different temperatures for the "Tn_Type B" IO to VSS protection. The breakdown voltage (BV) decreases with increasing

temperature, and such a behavior is dominated by the embedded bipolar transistor. The same situations were observed in other types of junction configuration. The BV values for different temperatures are summarized in Table 4-2. Note that the BV is defined as the voltage at which the leakage current reached a level of the 10 μA.

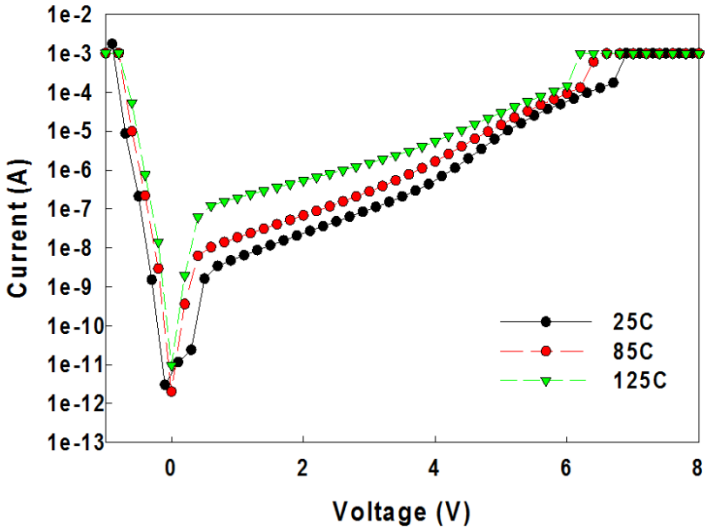


Figure 4-10 DC characterization of type B structure for IO-VSS protection at different temperatures

Table 4-1 Summary TLP results for different Tn types of junction

Junction Type	V_T (V)	V_H (V)	It2 (A)	Cap @0.9V (fF/kV HBM)	$I_{leakage}$ (A) @ 0.9V
Tn_Type A	5	1.6	1	115	1e-11
Tn_Type B	2.5	1.2	1	120	4.7e-9
Tn_Type C	3.4	1.4	1	115	4e-11
Tn_Type D	1	1	1	NA	1e-5

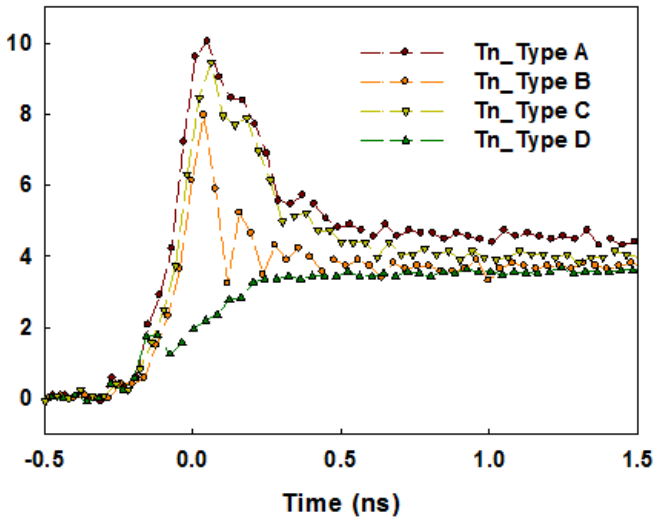


Figure 4-11 VFTLP voltage waveforms measured at 1-A current level for different junction configurations

Table 4-2 Summary of DC breakdown voltages for different Tn types of junction

Junction Type	BV @25C	BV @85C	BV @125C
Tn_Type A	7.1	7.1	7.1
Tn_Type B	5	4.9	4.4
Tn_Type C	6.7	6.7	6.7
Tn_Type D	0.92	0.86	0.8

Figure 4-11 depicts the transient response of the ESD protection cell subject to the CDM (Charged Device Model)-like very fast transmission line pulsing for the IO to VSS stressing, under which the shallow junctions and gate oxide are phone to failure. In line with the transient response obtained for the different stress modes, at a current level of 1 A, the response time is in

the sub 100 ps, which is in a range suitable for protecting the shallow junctions and thin gate oxide [56].

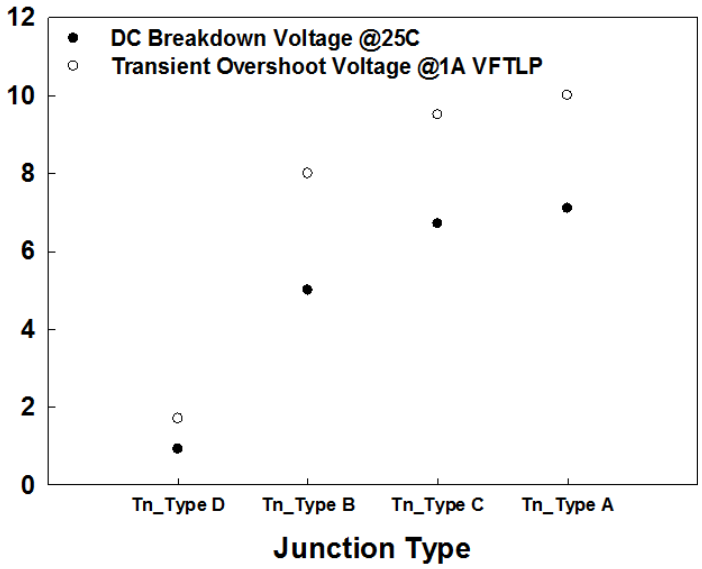


Figure 4-12 Overshoot voltage and trigger voltage for different junction configurations.

Figure 4-12 also depicts the overshoot voltages and the DC breakdown voltages at 25 °C for each junction type. “Tn_Type D” junction offers the lowest overshoot voltage. When there is a metal covering the junction, the embedded MOS can conduct a significant amount of current at a low stress and result in the turn-on of the Qn2 and eventually the turn-n of the Tn SCR. By adding the un-doped/un-silicided regions on one side of the metal gate and a floating N+ region in the “Tn_Type B” configuration, the MOS conduction effect can be reduced, thereby increasing the trigger voltage and also increasing the overshoot voltage. Depending on the different types of specifications, different protection cell types can be selected. The junction between the NW and PW regions gives rise to the highest overshot voltage and BV in the

"Tn_Type A" configuration. Followed by the "Tn_Type C" configuration implemented a P+ insert between the NW and PW junctions.

4.3.2 VDD to IO protection

The protection schematic for the VDD to IO protection is shown in Figure 4-6 Considering the different Tn junction combinations specified in Figure 4-7, their TLP measurement results are shown in Figure 4-13. Similar to the case of the Tn SCR, the "Tp Type A" configuration with the PW/NW junction offers the highest trigger voltage, and the "Tp Type A" configuration having a metal over the junction yields the lowest trigger voltage. As for the other two configurations, using the RPO with P+ insert provides a higher trigger voltage compare to the Tn SCR where the un-doped/un-silicided regions are included.

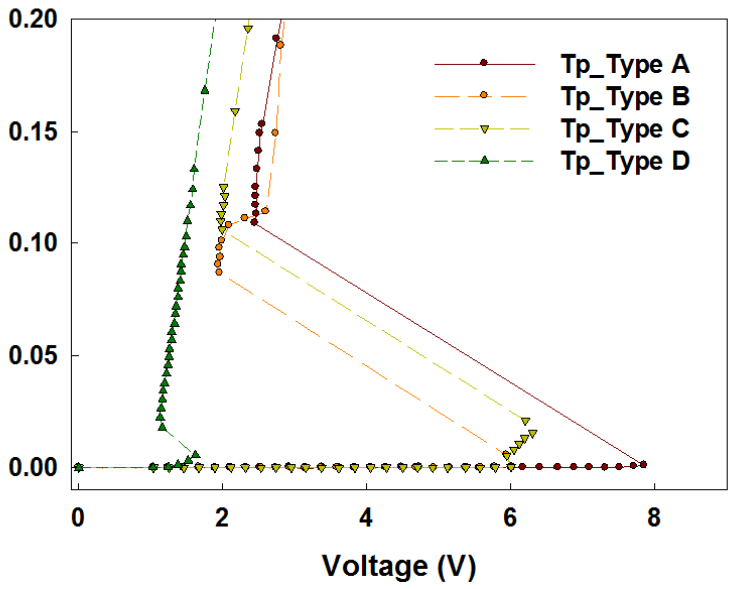


Figure 4-13 TLP performances of different junction configurations for VDD-IO protection

In the VDD to IO stressing condition, the base resistance (Rpw) of Qn1 is connected to the VSS, which is floating. The turn-on of this SCR will depend on the turn-on of the Qp1. The base resistance (Rnw) of Qp1 is relatively small in this case, making the trigger voltage higher than that of the Tn SCR. By optimizing the Rnw, for instance, by increasing the spacing between the N+ and P+ regions from 1 to 1.5 μm for the "Tp_Type B" configuration, the turn-on speed of the Qp1 is improved and the overshoot voltage can be reduced (i.e., from 7.4 to 6.9V @0.9A). Table 4-3 summarizes the TLP results for the four Tp junction types.

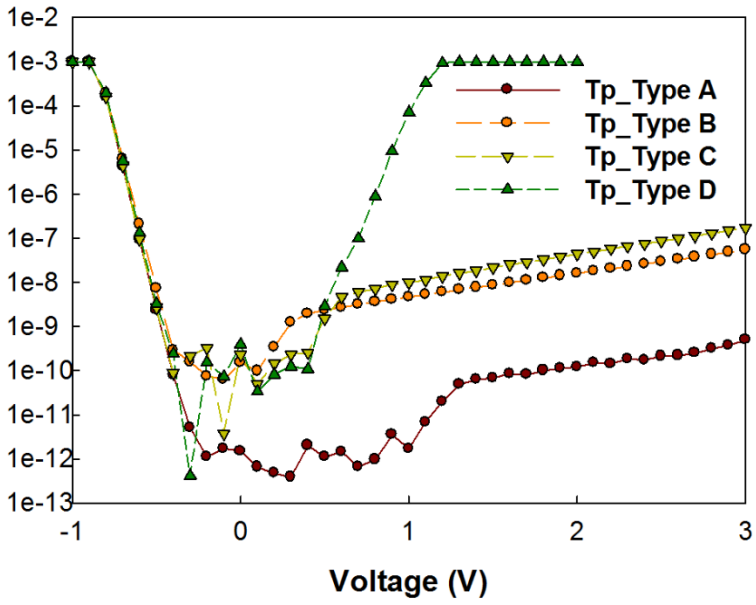


Figure 4-14 DC characteristics of different cells for VDD-IO protection at 25C

Figure 4-14 shows the DC characterization results measured between -1 to 3 V. Table 4-4 lists the DC BV values for different temperatures. The DC characterization also included subjecting the devices to a square-shape voltage waveform with a relatively large rise time of ~

1ms to emulate conventional power-up conditions. Under the voltage transition, the device exhibits relatively small displacement current without and the leakage is immediately reduced without showing signatures of miss-triggering or latch-up.

Table 4-3 Summary of TLP results for different Tp types of junction

Junction Type	V_T (V)	V_H (V)	It2 (A)	$I_{leakage}$ (A)
Tp_Type A	7.9	2.5	1	3.5e-12@ 0.9V
Tp_Type B	6	1.9	1	4e-9@ 0.9V
Tp_Type C	6.3	1.9	1	8.9e-9@ 0.9V
Tp_Type D	1.6	1.1	0.9	9e-6@ 0.9V

Table 4-4 Summary of DC breakdown voltages for different Tp types of junction

Junction Type	BV @25C	BV @85C	BV @125C
Tp_Type A	6.7	6.7	6.7
Tp_Type B	5.6	5.1	4.5
Tp_Type C	5.3	4.3	3.3
Tp_Type D	0.9	0.85	0.75

4.3.3 Capacitance results and discussion

The linearity (change in capacitance with respect to voltage) is an important design metric for large-signal, high-frequency converter applications. Linearity optimization is critical to the IO design as it directly impacts data distortion [47][59]. The monolithic IO ESD protection configurations are characterized using the C-V measurement setup shown in Figure 4-15. In this diagram, the protection cell is powered at the operating voltage. The C-V meter and power

supply ground references are commonly defined to capture the capacitance variation over voltage while the cell is biased. This measurement setup allows for the capacitance characterization in alignment with the protection cell design intend. The labels VHF/VHS and VLF/VLS in Figure 4-15 correspond to the high-end and low-end bias terminals, respectively, of the C-V meter Kelvin measurement setup.

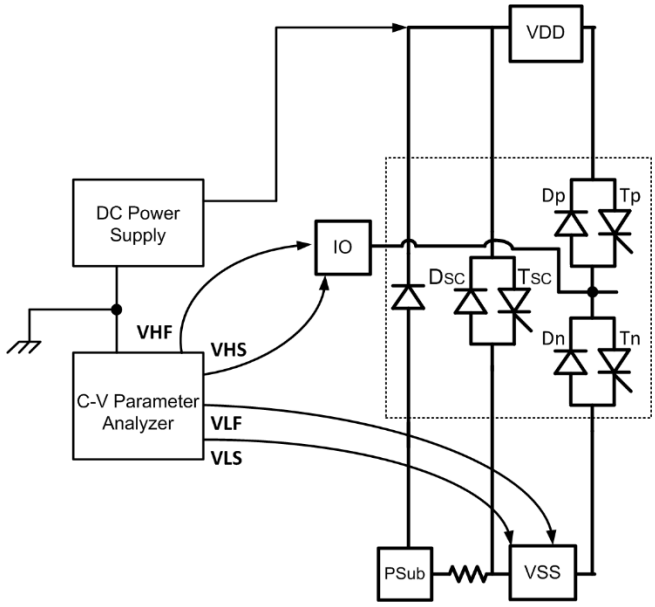


Figure 4-15 Schematic of capacitance vs. voltage (C-V) characterization setup.

Figure 4-16 shows the C-V results for the in-situ protection structures using the building blocks “Tn_Type B” and “Tp_Type B”. It is measured at 25 C and normalized to 1 kV HBM. Notice that this measurement provides the net capacitance looking into the IO connected to the in-situ protection cell. A separate metal array including the bond-pads and equivalent metallization to the one used in the in-situ protection device was used to de-embedding the effect of interconnectivity above metal 4. As a result, the capacitance measurement captures the effect

of the different junction capacitances and below metal 3 interconnectivity capacitance contribution. A capacitance of less than 150 fF is a common requirement in the distributed data conversion applications.

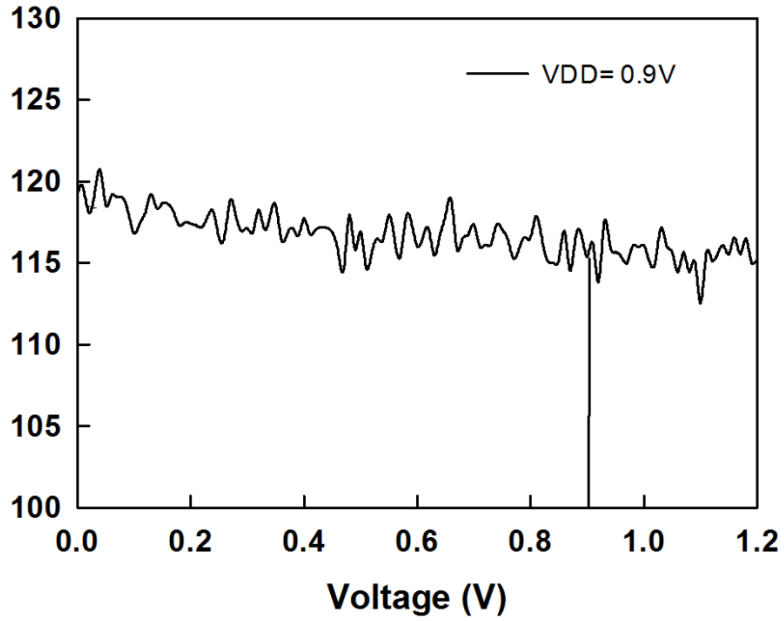


Figure 4-16 IO Capacitance vs. voltage normalized to 1 kV HBM (Human Body Model) for the proposed protection cell

For the case of VDD = 0.9V operating condition, the C-V data is measured with the IO pin biased from 0 to 1.2V. Note that the Dp diode is turned-on when the IO voltage exceeds 1.5V. The same C-V trend was found for the cases of larger VDD. Notice the low and relatively constant capacitance under the operating voltages, varying within 3 fF for the operating voltages ranging from 0 to 0.9 V. This demonstrates the capacitance linearity witin the operating voltage range.

4.4 Suggested ESD protection structure

Table 4-5 Protection structure suggestions for different voltage operations

Applications	IO to VSS	VDD to IO
1V protection	Tn_Type B	Tp_Type D
1.8V protection	Tn_Type B	Tp_Type B
3.5V protection	Tn_Type C	Tp_Type B

Based on preceding design and analysis, one can use the proposed monolithic design that is implemented with a specific junction combination or can use those junction configurations independently. A summary of design building block combinations for different reference interface operating voltage conditions is given in Table V. It includes cells for the 1.0, 1.8, and up to 3.5 V applications. For the IO to VSS protection, considering the leakage current requirement, the "Tn_Type B" configuration is a suitable choice for the 1.0 and 1.8 V ESD protection. When the voltage is increased to 3.5 V, the "Tn_Type C" configuration can meet the requirements of high DC BV and trigger voltage. On the other hand, for the protection of VDD to IO, the "Tp_Type D" configuration can be selected for the 1.0 V voltage applications, whereas the "Tp_Type B" is more suitable for the 1.8 and 3.5 V applications. Besides, the "Tn_type D" and "Tp_type D" can also be combined to offer the best overall performance in the low operation condition down to around 0.5 V.

4.5 Conclusion

An electrostatic discharge (ESD) structure capable of providing multiple discharge-paths and multiple operating voltages (0.5-3.5 V) for in-situ IO protection in distributed CMOS communication applications has been proposed and demonstrated in a 28-nm CMOS process. The optimization criteria for the VDD to IO and the IO to VSS protection schemes were presented and discussed. TLP, very-fast TLP, and C-V measurements were conducted to characterize and verify the performances of the new protection cell, and excellent ESD performances were obtained and illustrated in this study. Based on the experimental results shown in this paper, optimized and effective protection solutions can be realized using different junction configurations in advanced CMOS metal-gate processes. The proposed building blocks components of the protection cell can also be used independently to build single-power-reference standalone IO protection structure with variable operating voltage.

CHAPTER 5 INVESTIGATION OF ESD PROTECTION DEVICE PERFORMANCE UNDER DIFFERENT TEMPERATURE

5.1 Introduction

Electrostatic static has been considered to be a major threat to the semiconductor industry, resulting up to 70% of failures in the IC industry [61]. Providing adequate ESD protection solution is becoming more difficult and challenging, especially with the scaling of the device dimensions and also more complexity design of the integrated circuit. The typical ESD requirement in the IC products are 2 KV in human body model, 200V machine model [62]. With the variety of ESD protection devices, such as diode, gate-grounded MOS (GGMOS) and silicon controlled rectifier, this level of protection can be easily achieved. And the MOS protection structure usually have an area gain factor related to the ESD performance. SCR has very low holding voltage (below 5V) even though it has relatively high triggering Voltage (about 20V depending on the process). It might results the latch-up issue. However due to the benefit of its area efficiency, some other SCR-based devices (LVTSCR, GGSCR, etc) have been proposed to lower triggering voltage [63]. To reduce the affect of transient-induced latch-up problem due to lower holding voltage, increasing the holding current or holding voltage is a better solution to this issue.

In the industries, more and more electronics are needed to operate reliably in harsh environment, which includes high temperature. The high temperature can cause the shift of electronics performance. Designer must account for the changes of the performance at different temperature. In the semiconductor industry, to build the devices that able to worked at high temperature usually use the wild bandgap devices, such as GaN and SiC. At the ESD point of

view, we also need to use a specific design for that high temperature application. In addition to this high temperature constraint, ESD requirements from the integrated circuit to the system are particularly severe: for example, in automotive applications, 2-8kV in contact according to the IEC 61000-4-2 standard is often required [63].

Pervious works has been shown that the increasing of the ambient temperature can result the holding voltage and holding current drops, which brings a potential latch-up issue [64]. Depending on the different device types, the performance of the ESD device can changes differently. In this chapter, we will focus on discussing the ESD performance of the several different SCR devices, which is used extensively in the ESD protection solutions nowadays, under various temperature conditions.

5.2 Device structure

In this research, we have used four different types of SCRs which is specialized in the ESD protection. The first set of the device we are using is the bi-directional SCR (Bi-SCR) structure shown in Figure 5-1. A bidirectional SCR device has been introduced [67]. The advantage of this type of device is the dual-polarity protection. For both positive direction and negative direction, it can provides trigger voltage up to 15V at regular CMOS process for both sides. However, sometimes it is too high for the protection for the CMOS devices. To enable this Bi-SCR design, a lot of technique has been adopted and optimized to reduce the trigger voltage.

There are three structures has been selected in this Bi-SCR design for this research work, first one is a conventional Bi-SCR1 (Figure5-1(a)). The other two are modified versions from the conventional design, Bi-SCR2 (Figure5-1(b)) and Bi-SCR3 (Figure5-1(b)). With the extra

P+/N+ inserts in the Bi-SCR2 and Bi-SCR3, they can helps reduce the trigger voltage but also increasing holding voltage. With a proper dimension design, previous report high leakage issue can be greatly reduced [68].

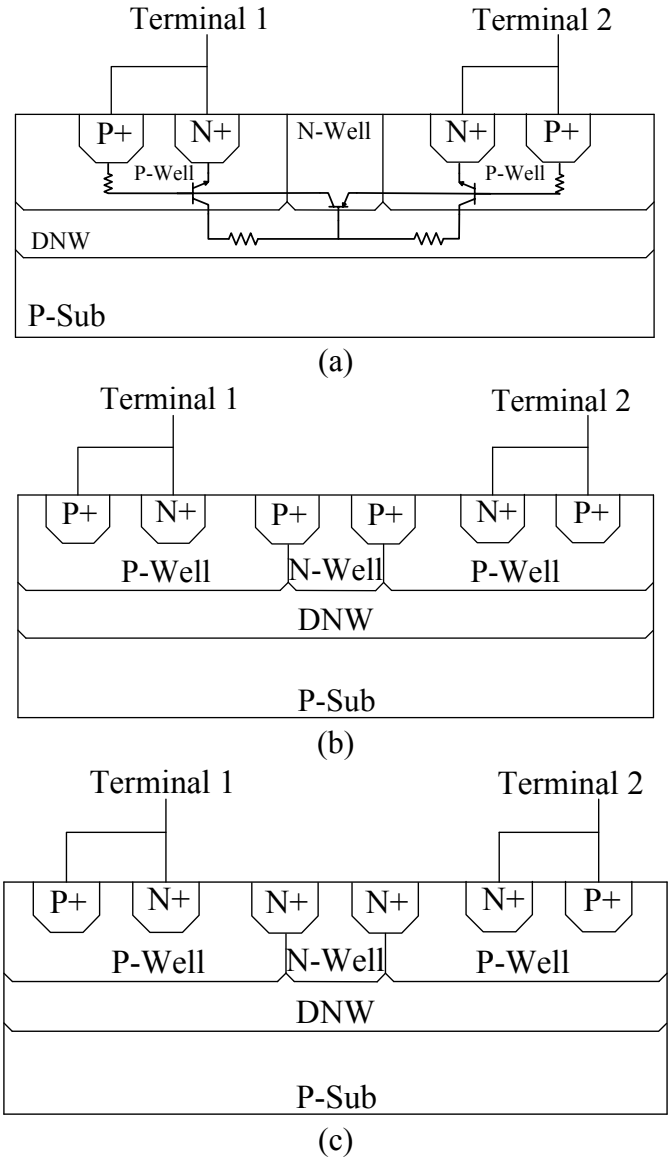


Figure 5-1 Bi-directional SCR structure

Inside the Bi-SCR there are three SCR structure imbedded between N+/PW/NW/PW/N+ in the devices which provides the dual conduction path. Three bipolar transistors have formed in this device: left N+/PW/NW formed a NPN bipolar transistor, the middle PW/NW/PW formed a PNP bipolar transistor, and another NPN bipolar transistor formed from the right NW/PW/N+ [69]. For the case of Bi-SCR2 and Bi-SCR3, the N+/P+ inserts at two side of the center NW is intended to reduce the trigger voltage and increasing the holding voltage. As a result, the β of the parasitic bipolar transistors increases, resulting better current shunting ability for the ESD conduction. The NWs is also placed around the device providing the isolation to the other devices.

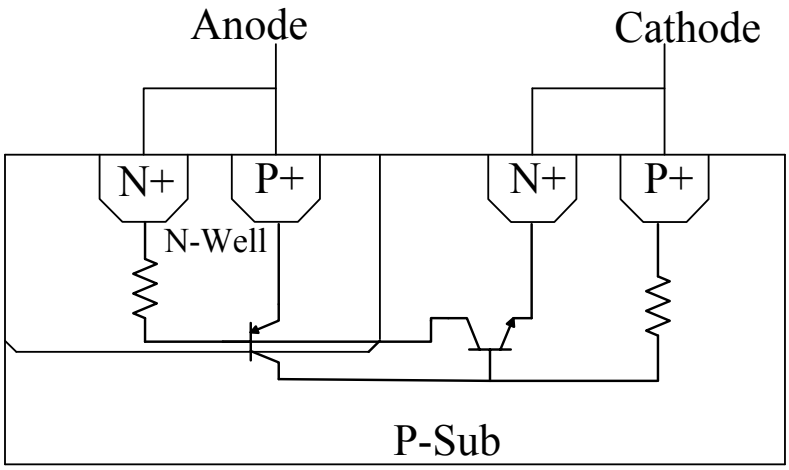


Figure 5-2 Conventional single directional SCR structure

Another structure we are using to doing the comparison is a single directional SCR (Sd-SCR). The cross-section of this device is shown in Figure 5-2. This Sd-SCR is a typical standard design of a SCR for ESD protection using a PNPN structure. Inside the N-well, the P+ diffusion and N+ diffusion connected together as an anode. And the N+ diffusion P+ diffusion at P-

Substrate (P-Sub) forms the cathode of the SCR. This connectivity allows the ESD protection using this structure. The schematic of the SCR structure has been shown in the cross-section.

All the structure we have used are using the layout stratagem shown in Figure 5-3. The size of three Bi-SCRs we are 97um*60um and the size of the Sd-SCR is around 100um*80um. All of them has used the two figure structure design to achieve a better performance of those ESD protection devices.

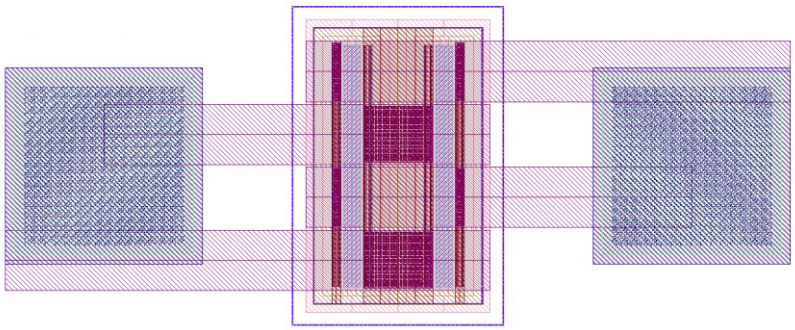


Figure 5-3 Layout view of the tested structure.

5.3 Results and discussion

To characterize the ESD performance of all four devices, we have using the Barth TLP system with the temperature controlled chunk. We have selected five different temperature, 25°C, 85°C, 125°C, 200°C and 300°C. The major factors that determine the ESD performance are trigger voltage, holding voltage, holding current, failure current and leakage current. In this section, we will compare how those four different devices performs under those five different temperature condition.

5.3.1 Trigger voltage

The first performance factor we are looking at is the trigger voltage. In previous chapter 1 when we discuss the safe operation area of the ESD devices in Figure 1-7, triggering voltage (V_{t1}) must be larger than the operation voltage plus some noise margin. It is a key parameter to determine whether the device can be used or not. Figure 5-4 has shown the trigger voltage variations of those four devices under five different types of temperature conditions. Three Bi-SCR has shown very steady trigger voltage from 25°C up to 300°C. However, the Sd-SCR is more vulnerable to the temperature variations, especially when the temperature exceeds 200°C, a huge decrease in the trigger current are observed in 300°C.

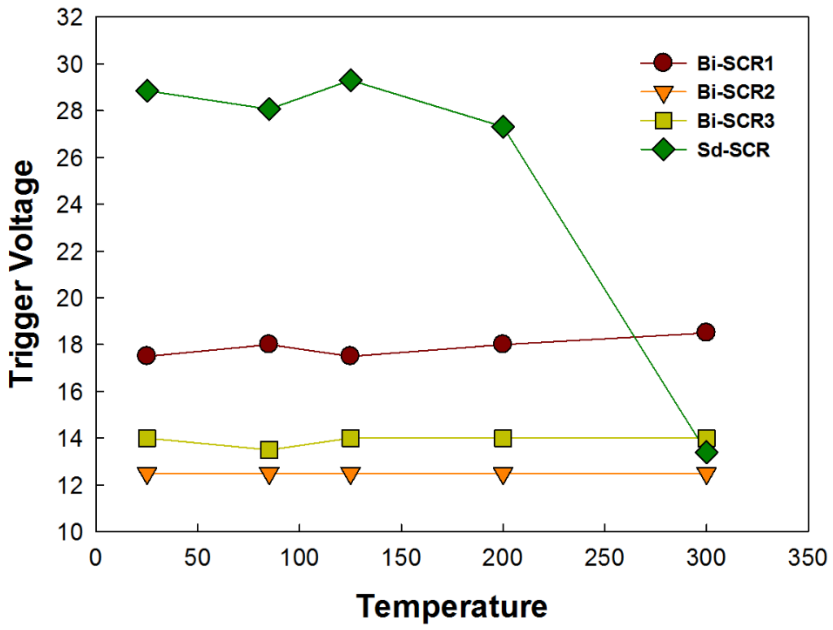


Figure 5-4 Trigger voltage variations at different temperature

Both Bi-SCRs and the Sd-SCR have similar turn on mechanism. At the device trigger point, usually it will be the avalanche breakdown of the PN junction of the parasitic bipolar

transistor. For the Bi-SCRs, it will be from a floating Nwell to the Pwell, or a floating N+/P+ to the Pwell, and when the lattice temperature increases there will be more electron pumping into the parasitic bipolar. However, the lower doping concentration from the Nwell limited the avalanche breakdown of that Pwell to Nwell junction, so the trigger voltage stays the same. While looking into the Sd-SCR, the trigger event happens when the avalanche breakdown happens between the Nwell to the P-sub. There will be more electron pumping into the Nwell due to the N+ connection to the anode, with the higher lattice temperature, there will be a positive feedback brings even more available electron into the Nwell. Finally, when the temperature exceeds a critical point, which is 200°C in our case, the trigger event happens much more early than to the normal temperature range.

5.3.2 Holding voltage and Holding current

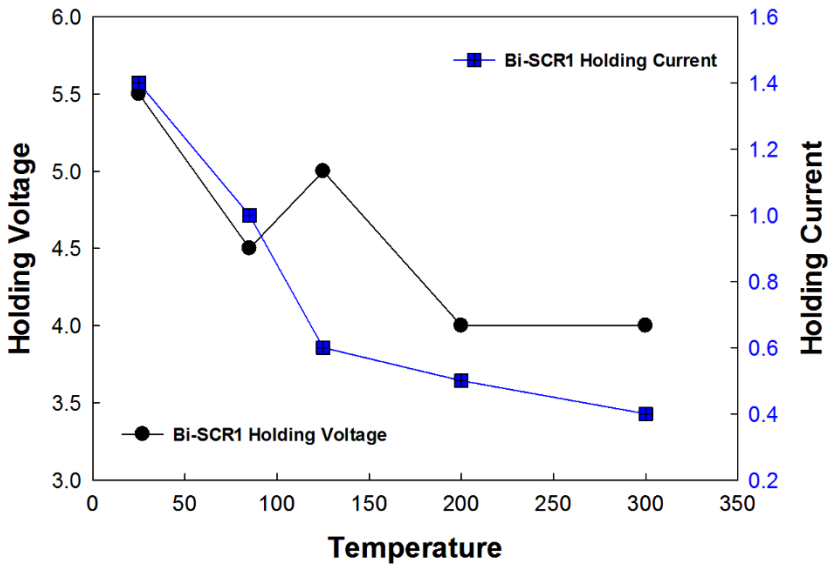


Figure 5-5 Holding Voltage and Holding Current performance of Bi-SCR1 at different temperature

Aside from the trigger voltage, another parameters to look at is the holding voltage and holding current. Among the three Bi-SCRs, the Bi-SCR2 and Bi-SCR3 are the improved version by using the N+ and P+ inserts between the Nwell and Pwell junction, resulting the increases of the holding voltage and decreases of trigger voltage.

Figure 5-5 shows the holding voltage and holding current changes of the Bi-SCR1. Both holding voltage and current showing a decreasing trend with the increasing temperature condition. There are 27% drop in the holding voltage and 71% drop in the holding current. Figure 5-6 shows the results of the Bi-SCR2, which shows a similar trend of decreasing by 50% of the holding voltage and 70% of the holding current. The Bi-SCR3 in the Figure 5-7 are shown the similar characteristics, drop 56% of holding voltage and 80% of the holding current.

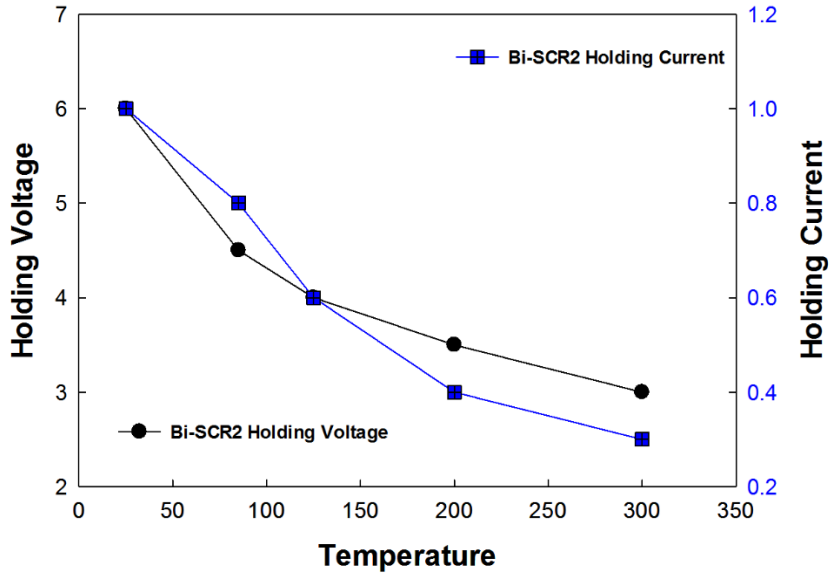


Figure 5-6 Holding Voltage and Holding Current performance of Bi-SCR2 at different temperature

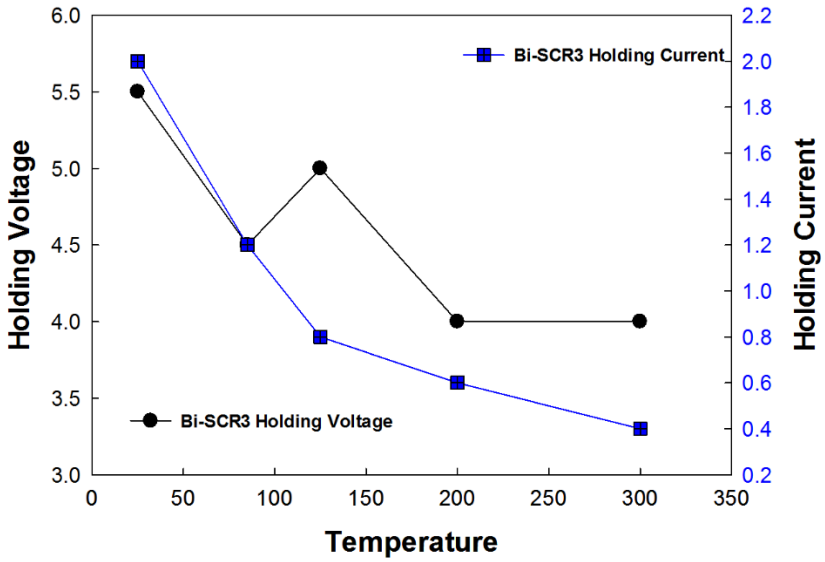


Figure 5-7 Holding Voltage and Holding Current performance of Bi-SCR3 at different temperature

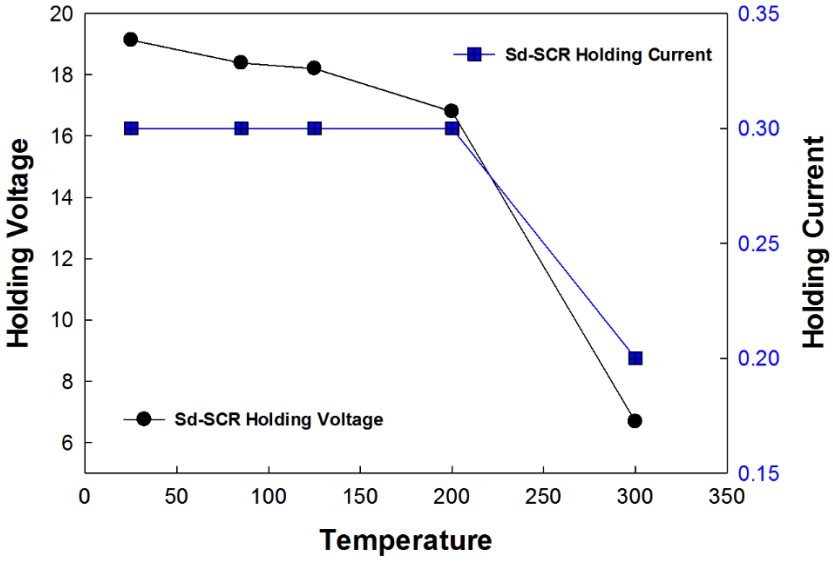


Figure 5-8 Holding Voltage and Holding Current performance of Sd-SCR at different temperature

When looking at the Sd-SCR structure, the holding voltage has slightly decrease from 25°C to 200°C and holding current stays relatively the same before the 200°C. However, when the device go beyond the 200C, it was showing a drastic drops in both the holding voltage and holding current.

For both Bi-SCRs and Sd-SCR, the V_{BE} of the embedded bipolar will decrease with the increasing of the temperature. After the device turns on, the lower base-emitter voltage and the higher resistance from the junction, result the overall holding current drops. We could not see the Sd-SCR drop the holding current, this is due to the 50Ω TLP system limitations, after device turns on, the earliest points that can capture is around 0.2-0.4A current level. But it is expecting that all the devices will be showing the similar trend with the decreasing of the trigger voltage and trigger current when increasing the device temperature. And the Bi-SCRs will saturate when reaching a very high current level, while the Sd-SCR will becomes worse and worse after a critical temperature point.

5.3.3 Failure Current and leakage current

Figure 5-9 shows the failure current of all four types of devices. There will be 10~15% degradation at 300°C compare to the room temperature (25°C). The ESD failure is happened in the junction of those devices. Usually it will results from a large current going through the junction and it reaches a critical point result the junction rupture brings the total failure of the protection device. At 300°C the increased lattice temperature helps the junction reaches the failure point more easily, and also decreased the heat dissipation abilities while during the ESD stress. Resulting the overall degradation at the failure current.

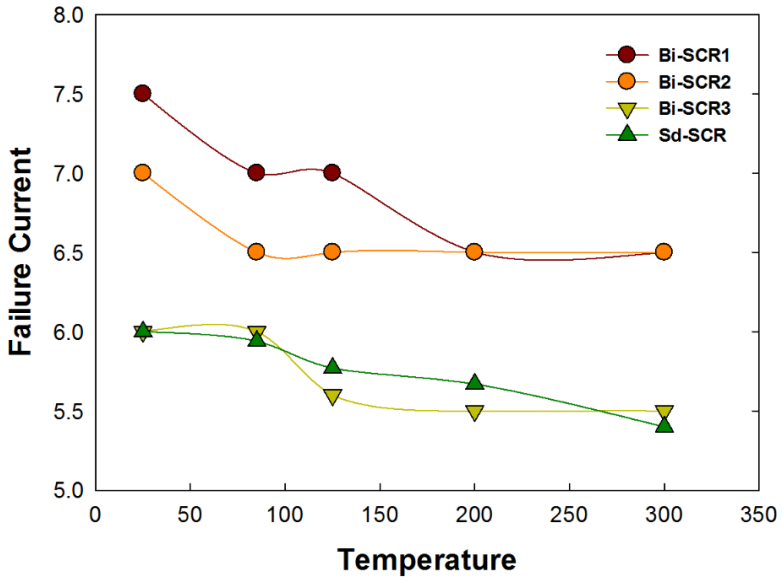


Figure 5-9 Failure current of different devices under various temperature

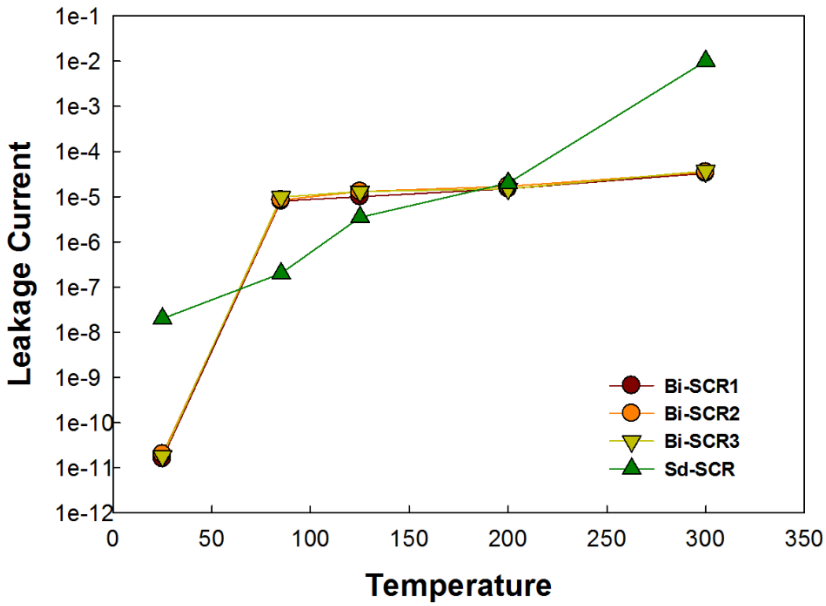


Figure 5-10 Leakage current of different devices under various temperature

Another thing to look at is the leakage current. Figure 5-10 shows the leakage current of all four devices under various temperature condition. The tested leakage point is at 20% below the breakdown voltage point, which is similar to the operational point of the protected circuit. All the Bi-SCRs shows a saturation characteristics after the temperature exceeds 100°C, however, the Sd-SCR keeps increasing with the increasing temperature. At 300°C, the leakage for the Bi-SCRs are still acceptable while the Sd-SCR will short the protected internal circuit.

5.4 Conclusion

In this research work, we have compared four types of devices, three of them are Bi-SCR and one of them are the Sd-SCR. It is shown that, all four ESD protection structure are showing similar tendency of decreasing the holding voltage and holding current dramatically while increasing the temperature. For the high temperature environment ESD protection solutions, those devices becomes more vulnerable to the latch-up issue, which will need to have special solutions regarding this issue. And same decreasing trend has been shown in the failure current as well, but the degradation is not very dramatic from the SCR devices we are looking at. Another aspect we need pay special attention to the ESD solutions for the high temperature environment is the trigger voltage. Compare the Bi-SCR to the Sd-SCR, the Bi-SCR's trigger voltage stays relatively the same even though it reaches 300°C. However, the Sd-SCR's trigger voltage drops dramatically. Another advantage of the Bi-SCRs is the leakage current is saturated at a certain level and won't increase future with the increase temperature. But Sd-SCR will performs like as a short, at the internal circuit operation level, after reaching a critical temperature point. Depending on the environmental conditions of different application, the

performance of the ESD protection devices need to be characterized and selected accordingly. Overall it will be more appropriate to choose Bi-SCR at the very high temperature environment rather than the Sd-SCR.

CHAPTER 6 SUMMARY AND OUTLOOK

ESD failure has becomes a real threat to the semiconductor industry, resulting one third of the ICs failures. A lot of research works has been put into the ESD solution and stratagems nowadays to solve the real word ESD issue to improving the reliability of the modern ICs.

With the better understanding of the ESD event, there are more and more new standards coming out. One of them is the human metal model, which gives a designer an understanding about the system level ESD performance at the component level. To implement this technique into the characterization of the ICs at wafer level, there are a lot of issues that haven't been discovered. The first part of my research work has been focused on finding the best way to accurately characterize the wafer level circuit's ESD performance. And we have developed a novel method using the waveform as a reference to eliminate the potential errors from the conventional leakage evaluation method. This new method successfully achieves better accuracy compare to the conventional way. However, the test setup is very complex and it will also depending on which system is using. To extend the usability of this methodology needs the optimization in the test system.

After we can achieve the more accurate characterization of the IC's ESD performance, optimization and design a better ESD protection device is the essential of achieving higher robustness. At the second part of the research work, we have designed for high voltage interface ESD protection applications fabricated in low voltage processes. A new bidirectional SCR fabricated in a low-voltage, 180-nm CMOS process was developed for enabling the ESD protection of high-voltage-tolerant communication interface pins. The SCR high trigger voltage was successfully achieved by selectively defining and adding native-buffer regions in the device.

The new SCR offered a high trigger voltage up to 24 V. When a T-island active-region topology was implemented, the proposed SCR, in addition to the high trigger voltage, yielded a highly desirable high trigger current of over 1 A and the low parasitic capacitance.

While the device dimension is shrinking down in the semiconductor industry, the ESD protection becomes more and more challenging. And it requires not only the best performance, but also the smaller size. In this part of research work, an electrostatic discharge (ESD) structure capable of providing multiple discharge-paths and multiple operating voltages (0.5-3.5 V) for in-situ IO protection in distributed CMOS communication applications has been proposed and demonstrated in a 28-nm CMOS process. The optimization criteria for the VDD to IO and the IO to VSS protection schemes were presented and discussed. TLP, very-fast TLP, and C-V measurements were conducted to characterize and verify the performances of the new protection cell, and excellent ESD performances were obtained and illustrated in this study. Based on the experimental results shown in this paper, optimized and effective protection solutions can be realized using different junction configurations in advanced CMOS metal-gate processes. The proposed building blocks components of the protection cell can also be used independently to build single-power-reference standalone IO protection structure with variable operating voltage.

The ESD protection devices not only works in the normal room temperature, with the wild range of the applications that extended to the extreme work environment, such as high temperature, high radiation. With the increasing demand of ESD protections for those applications, a study of how the ESD protection device behaves is needed. Four types of SCRs has been compared the ESD performance under various temperature condition, from 25C to 300C. Different degradation trend has been shown in this section. Based on the application the

ESD protection devices implemented, those data can helps a better selection of the proper protection design. And also this research work has been shown the potential latch-up issue at the higher temperature is another issue that needs the designers pay special attention to.

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