

RF ENERGY HARVESTING FOR IMPLANTABLE ICS WITH ON-CHIP ANTENNA

by

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## ABSTRACT

Nowadays, as aging population increasing yearly, the health care technologies for elder people who commonly have high blood pressure or Glaucoma issues have attracted much attention. In order to care of those people, implantable integrated circuits (ICs) in human body are the direct solution to have 24/7 days monitoring with real-time data for diagnosis by patients themselves or doctors. However, due to the small size requirement for the implanted ICs located in human organs, it's quite challenging to integrate with transmitting and receiving antenna in a single chip, especially operating in 5.8-GHz ISM band. This research proposes a new idea to solve the issue of integrating an on-chip antenna with implanted ICs. By adding an additional dielectric substrate upon the layer of silicon oxide in CMOS technology, utilizing the metal-6, it can form an extremely compact 3D-structure on-chip antenna which is able to be placed in human eye, heart or even in a few mm-diameter vessels. The proposed 3D on-chip antenna is only  $1 \times 1 \times 2.8 \text{ mm}^3$  with -10 dB gain and 10% efficiency, which has capability to communicate at least within 5 cm distance. The entire implanted battery-less wireless system has also been developed in this research. A designed 30% efficiency Native NMOS rectifier could generate 1 V and 1 mA to supply the designed low power transmitter including voltage-controlled oscillator (VCO) and power amplifier (PA). The entire system performance is well evaluated by link budget analysis and the simulation result demonstrates the possibility and feasibility of future on-demand easy-to-design implantable SoC.

**To my parents and my future**

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# TABLE OF CONTENTS

LIST OF FIGURES .....	ix
LIST OF TABLES .....	xiii
LIST OF ACRONYMS AND ABBREVIATIONS .....	xiv
CHAPTER ONE: INTRODUCTION.....	1
1.1 Motivation .....	1
1.2 Goal of Research .....	2
1.3 Results Outline .....	3
CHAPTER TWO: SCHOTTKY BARRIER DIODE RECTIFIER.....	4
2.1 Introduction .....	4
2.1.1 DC Analysis of Diode.....	4
2.1.2 AC analysis of Diode.....	5
2.2 Theoretical Principle of The RF Rectifier.....	5
2.3 Function Analysis of RF Rectifier .....	8
2.3.1 Clamper .....	8
2.3.1.1 Positive Unbiased.....	9
2.3.1.2 Negative Unbiased.....	9
2.3.1.3 Positive Biased.....	10
2.3.1.4 Negative Biased .....	10
2.3.2 Envelope Detector .....	11
2.3.3 Summary in Clamper and Envelope Detector .....	12
2.4 Parameters of The RF Rectifier.....	13
2.4.1 Output DC voltage ( $V_{out}$ ).....	13
2.4.2 Efficiency ( $\eta$ ).....	14
2.4.3 Sensitivity .....	14
2.5 Conventional Rectifiers.....	15
2.5.1 Matching of RF Rectifier.....	16
2.5.2 Load Effect of RF Rectifier .....	17
2.5.2.1 Optimal $R_L$ .....	18
2.5.2.2 Load Resistance Compensation for Efficiency Enhancement.....	18

2.5.3 Multi-stage RF Rectifier .....	21
2.6 Temperature Variation of SBD RF Rectifier .....	25
2.7 Summary .....	26
CHAPTER THREE: DIODE-CONNECTED MOSFET RF RECTIFIER .....	28
3.1 Introduction .....	28
3.2 Diode-connected MOSFET .....	28
3.2.1 Normal NMOS .....	28
3.2.2 Normal PMOS .....	30
3.2.3 Native NMOS .....	32
3.3 Three-port RF Rectifier .....	34
3.3.1 Introduction .....	34
3.3.2 Three-port RF Rectifier Design .....	36
3.3.3 Lossless Three-port Network .....	36
3.3.4 Multi-stage Diode-connected MOSFET with Native NMOS .....	38
3.3.5 Load Resistance Variation .....	40
3.3.6 Temperature Variation .....	42
3.3.7 Compared with Papers .....	42
3.4 Antenna Design .....	43
3.5 Summary .....	46
CHAPTER FOUR: ON-CHIP RECTENNA FOR BIOMEDICAL APPLICATION .....	47
4.1 Introduction .....	47
4.2 Link Budget Analysis .....	48
4.3 RF Rectifier for Biomedical Application .....	51
4.4 On-chip Antenna Design .....	52
4.4.1 Introduction .....	52
4.4.2 3D On-chip Antenna .....	57
4.4.3 Simulation Results of the Proposed 3D On-chip Antenna .....	60
4.5 Rectenna Integration .....	64
4.6 Summary .....	65
CHAPTER FIVE: IMPLANTABLE WIRELESS SYSTEM FOR BIOMEDICAL APPLICATION .....	67

5.1 Introduction .....	67
5.2 Implanted RF Transmitter .....	68
5.3 External Antenna.....	70
5.4 Biomedical Wireless System.....	72
5.5 Summary .....	74
CHAPTER SIX: IMPLANTALBE WIRELESS SYSTEM WITH ON-CHIP ANTENNA FOR CARDIOVASCULAR PRESSURE MONITOR .....	75
6.1 Introduction .....	75
6.2 On-chip Antenna for Global Blood Pressure Monitoring .....	76
6.3 Wireless system Global Blood Pressure Monitoring .....	79
6.4 On-chip Antenna for Local Cardiovascular Pressure Monitoring .....	80
6.5 Wireless system for Local Cardiovascular Pressure Monitoring .....	84
6.6 Conclusion.....	86
CHAPTER SEVEN: CONCLUSION .....	87
7.1 Accomplishments .....	87
7.2 Future Work .....	87
APPENDIX: DERIVATION OF EQUATION OF INPUT VOLTAGE TO A RF RECTIFIER	90
REFERENCES .....	93



## LIST OF FIGURES

Fig. 1 (a) A diode on the forward bias (b) I-V curve of a diode on forward bias.....	4
Fig. 2 (a) A diode with AC voltage source (b) Voltage and current waveform cross the diode with a voltage source .....	5
Fig. 3 The RF rectifier on (a) negative cycle (b) positive cycle .....	6
Fig. 4 $V_{out}$ versus $V_{rf}$ of the rectifier in Fig.3 based on equation (1) and (a) ADS ideal diode model ( $V_{th}=0.7$ V) (b) TSMC SBD ( $V_{th}=0.3$ V) .....	7
Fig. 5 (a) Equivalent circuit and (b) TSMC SBD layout .....	7
Fig. 6 Sub-circuits on RF Rectifier.....	8
Fig. 7 The voltage reference shifts up by a clamper circuit.....	9
Fig. 8 Positive unbiased clamper .....	9
Fig. 9 Negative unbiased clamper.....	10
Fig. 10 Positive biased clamper .....	10
Fig. 11 Negative biased clamper.....	11
Fig. 12 Envelope detector circuit.....	11
Fig. 13 Waveform at node of (b) $V_{in}$ (c) $V_n$ and (d) $V_{out}$ of the rectifier (a) with ADS diode model .....	13
Fig. 14 Waveform at node of $V_{in}$ , $V_n$ , and $V_{out}$ of the rectifier with TSMC SBD model .....	13
Fig. 15 (a) Output voltage (b) efficiency of the rectifier in Fig. 13(a) .....	15
Fig. 16 (a) Conventional RF rectifier and its (b) equivalent circuit.....	16
Fig. 17 Input impedance of the RF rectifier shown on smith chart .....	17
Fig. 18 The RF Rectifier with a matching inductor .....	17
Fig. 19 (a) $V_{out}$ and (b) efficiency versus $P_{in}$ of the RF rectifier with and without a matching inductor .....	17
Fig. 20 Variation of load resistance versus (a) output voltage (b) efficiency at 0 dBm input power level .....	18
Fig. 21 Variation of load resistance versus (a) output voltage and (b) efficiency at -20 dBm.....	19
Fig. 22 RF Rectifier with an additional diode to compensate the load resistance .....	20
Fig. 23 $R_j$ versus $P_{in}$ of the RF rectifier with load compensation.....	21
Fig. 24 (a) $V_{out}$ and (b) efficiency versus $P_{in}$ of the RF rectifier with and without load compensation diode .....	21
Fig. 25 Multi-stage RF rectifier .....	22
Fig. 26 Comparison of simulation and calculation of multi-stage rectifier .....	22
Fig. 27 (a) TSMC SBD multi-stage RF rectifier and (b) its equivalent circuit .....	24
Fig. 28 Efficiency versus input power with different number of stages .....	25
Fig. 29 Efficiency versus input power with different temperature value .....	25
Fig. 30 Variation of threshold voltage with varied temperature at (a) DC source and (b) AC source.....	26

Fig. 31 (a) A diode-connected NMOS and (b) its equivalent circuit (c) I-V curves of a NMOS with and without gate and drain connected to each other.....	29
Fig. 32 Diode-connected MOSFET rectifier with two NMOS transistors .....	30
Fig. 33 A diode-connected NMOS RF rectifier with a matching inductor and 50-Ω source terminal.....	30
Fig. 34 (a) Output voltage and (b) efficiency of diode-connected NMOS rectifier and SBD rectifier versus input power .....	30
Fig. 35 (a) A diode-connected PMOS and (b) its equivalent circuit and(c) I-V characteristic curves.....	31
Fig. 36 A diode-connected PMOS RF rectifier with a matching inductor and 50-Ω source terminal.....	31
Fig. 37 (a) Output voltage and (b) efficiency of diode-connected MOSFET RF rectifier with PMOS and NMOS versus input power.....	31
Fig. 38 Cross-sectional view of CMOS technology .....	32
Fig. 39 I-V curve of diode-connected MOSFET with Normal NMOS and Native NMOS .....	32
Fig. 40 A diode-connected Native NMOS RF rectifier with a matching inductor and 50-Ω source terminal.....	33
Fig. 41 Comparison in Efficiency versus input power of the diode-connected MOSFE rectifier with NMOS, PMOS, Native NMOS and SBD.....	33
Fig. 42 (a) two-port and (b) three-ports RF rectifier block diagrams .....	36
Fig. 43 (a) A arbitrary three-port network (b) A lossless three-port network.....	37
Fig. 44 Proposed three-port 13 stages diode-connected Native NMOS RF rectifier with a load resistance compensation diode. ....	39
Fig. 45 (a) $V_{out}$ versus $P_{in}$ (b) Efficiency versus $P_{in}$ of proposed three-port RF rectifier.....	39
Fig. 46 The simulation results of (a) output voltage at -20 dBm (b) Efficiency at -18.5 dBm with different rectifier approaches.....	39
Fig. 47 Load resistance variation of +/-10% with 250 samples (a) without load compensation (b) with load resistance compensation diode .....	41
Fig. 48 Load resistance variation of +/-20% with 250 samples (a) without and (b) with load resistance compensation diode .....	41
Fig. 49 (a) $V_{out}$ and (b) efficiency versus $P_{in}$ with different temperature.....	42
Fig. 50 Block diagram of the proposed three-port RF rectifier system .....	44
Fig. 51 Layout of the designed two IFAs .....	45
Fig. 52 HFSS simulation model (Blue is copper and green is the dielectric substrate).....	45
Fig. 53 (a) Return loss at (a) IFA 1 and (b) IFA 2 .....	45
Fig. 54 (a) 3D polar plot (b) radiation efficiency of the designed IFA.....	46
Fig. 55 The communication between external source and implanted device .....	48
Fig. 56 Use an external reader to receive the data of eye pressure from the IC inside human eyes. ....	49
Fig. 57 Implanted chip inside the Anterior chamber. <sup>[4]</sup> .....	49

Fig. 58 Link budget block diagram of the biomedical wireless system.....	50
Fig. 59 5.8-GHz diode-connected Native NMOS RF rectifier with TSMC 0.18 $\mu$ m models .....	51
Fig. 60 (a) Output voltage and (b) efficiency of the designed RF rectifier .....	52
Fig. 61 $S_{11}$ of the designed RF rectifier .....	52
Fig. 62 Efficiency and input impedance versus frequency of the designed RF rectifier .....	53
Fig. 63 Simplified 0.18- $\mu$ m CMOS process stack-up.....	54
Fig. 64 An IC is placed inside the anterior chamber in huamn eye .....	55
Fig. 65 Equivalent circuit of conjugate matching between antenna and RF rectifier.....	55
Fig. 66 Microstrip line fed dielectric resonator antenna .....	57
Fig. 67 Cross view of the proposed 3D- structure for on-chip antenna.....	58
Fig. 68 3D-view of the proposed on-chip antenna. (a) HSS model (b) Detail dimensions (Unit: mm).....	59
Fig. 69 Simulation model built up of the proposed on-chip antenna.....	59
Fig. 70 Simulated (a) return loss and (b) input impedance of the proposed on-chip antenna .....	60
Fig. 71 Simulated radiation pattern and gain in the E-plane and H-plane of the proposed on-chip antenna (Unit: dB) .....	61
Fig. 72 3D polar plot of the proposed on-chip antenna .....	61
Fig. 73 Surface current on the conductor of the proposed on-chip antenna .....	62
Fig. 74 (a) E-field distribution around the on-chip antenna (b) E field magnitude on the radiator and ground .....	62
Fig. 75 Efficiency and peak gain versus frequency of proposed on-chip antenna .....	63
Fig. 76 Rectenna system block diagram .....	64
Fig. 77 On-chip antenna integrated with an example RF wireless system .....	64
Fig. 78 (a) Output voltage (b) output current (c) efficiency of the proposed rectenna system at 5 dBm input the RF rectifier .....	65
Fig. 79 Simplified block diagram of the entire biomedical wireless system .....	67
Fig. 80 Implanted transmitter include a VCO and a PA.....	68
Fig. 81 (a) The output spectrum (b) return loss (c) voltage tuning range versus frequency of the designed RF transmitter.....	69
Fig. 82 OOK modulation by switching $M_7$ on and off through the control signal $V_{con}$ .....	70
Fig. 83 5.8-GHz patch antenna for the external device .....	70
Fig. 84 3D-polar plot (radiation pattern) of the 5.8-GHz patch antenna .....	71
Fig. 85 External antenna is placed 5-cm away from the human eye to communicate with the implanted on-chip antenna.....	71
Fig. 86 Simplified model placement for simulation of the loss between external and implanted on-chip antenna.....	72
Fig. 87 (a) Return loss and (b) propagation loss from the external patch antenna to the implanted on-chip antenna.....	72
Fig. 88 Schematic of the entire biomedical system .....	73
Fig. 89 Voltage ( $V_{rec}$ ) and current ( $I_{rec}$ ) of the implanted RF rectifier.....	73

Fig. 90 Frequency spectrum at external receiver .....	74
Fig. 91 (a) Carotid artery in the human neck (b)Pulmonary artery near heart.....	76
Fig. 92 3D-view of the proposed on-chip antenna for blood pressure. (a) HSS model (b) Detail dimensions (Unit: mm).....	77
Fig. 93 The on-chip antenna placed inside the carotid artery .....	77
Fig. 94 Simulation model for the on-chip antenna placed inside a blood vessel and Muscle box	78
Fig. 95 (a) Return loss and (b) radiation pattern of the proposed on-chip antenna for blood pressure monitor .....	78
Fig. 96 External antenna is placed 5-cm away from the human neck to communicate with the implanted on-chip antenna in carotid artery .....	79
Fig. 97 Propagation loss from the external patch antenna to the implanted on-chip antenna .....	80
Fig. 98 Output frequency spectrum at external receiver of the cardiac monitor system .....	80
Fig. 99 3D-view of the proposed on-chip antenna for placing in pulmonary artery. (a) HSS model (b) Detail dimensions (Unit: mm) .....	81
Fig. 100 Human chest model .....	81
Fig. 101 (a) Simulation model for the on-chip antenna placed in blood with muscle and bone around (b) Close view of simulated pulmonary which is right next to the heart .....	83
Fig. 102 (a) Radiation pattern (b) 3-D polar plot (c) return loss of the proposed on-chip antenna for local blood pressure monitor.....	84
Fig. 103 External antenna is placed 6-cm away from the heart to communicate with the implanted on-chip antenna in pulmonary artery.....	85
Fig. 104 Simulation result of (a) Return loss of external and implanted antenna (b) insertion loss from the external to the internal antenna to the implanted on-chip antenna .....	85
Fig. 105 Output power at external receiver of the cardiac monitor system.....	86
Fig. 106 Simplified circuit with a source terminal and a load of rectifier .....	91

## LIST OF TABLES

Table 1 Parameters of multi-stage RF rectifier .....	24
Table 2 Parameters and performances comparison in different technologies .....	34
Table 3 Comparison of the probability to achieve output voltage of 1V w/o load resistance compensation diode .....	41
Table 4 Proposed RF rectifier compares with different papers .....	43
Table 5 Link budget table of the biomedical wireless sensing system .....	51
Table 6 Performance summary and comparison with papers .....	63
Table 7 Parameters of the external patch antenna .....	71
Table 8 Parameters of the designed on-chip antenna for blood pressure monitor .....	79
Table 9 Material properties of human organs .....	82
Table 10 Parameters of the designed on-chip antenna in pulmonary artery .....	84

## LIST OF ACRONYMS AND ABBREVIATIONS

ADS	Advanced Design System
ASIC	Application Specific Integrated Circuits
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FET	Field Effect Transistor
IC	Integrated Circuit
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NMOSFET	N-type MOS Field Effect Transistor
OPAMP	Operation Amplifier
PA	Power Amplifier
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
SBD	Schottky Barrier Diode
SOC	System on Chip
$V_{DD}$	DC Supply Voltage
$V_{th}$	Threshold Voltage

# CHAPTER ONE: INTRODUCTION

## 1.1 Motivation

Nowadays, wireless communication technologies, such as GSM, GPS, Wi-Fi, etc., have been developed all around the world and the RF energy has scattered around our ambient that people are easily ignored the existence. In the past, the common ideas when people mention to the term of “Energy harvesting” are always sun light, wind, water, tide and etc. However, energy harvesting technologies are not limited to those but have been extended into radio frequency energy which surrounds people for centuries in daily life. In recent years, many researches focus on how to utilize this subtle energy and store it for driving electronic device to achieve the battery-less purpose. For accomplish this goal, one of the techniques evolved recently is the RF rectifier. A rectifier is an electrical device that can convert alternating current (AC) to the direct current (DC). Many applications such as RFID tag and implantable device are applying this technique to achieve this goal, which means all these applications are able to work by converting RF signal into DC supply without any external batteries. However, many limitations including short transmitting distance, low efficiency and sensitivity, costly fabrication and large size have to be overcome, especially in biomedical application which required to be implanted into human body.

Energy harvesting techniques for biomedical implantable applications have been widely researched <sup>[1 - 4]</sup> in this few years, for example, blood and eye pressure monitoring device. Because the patients are not able to replace the batteries or plug in an adaptor to charge the implanted device, utilizing the wireless energy to run the system is the most critical task. Therefore, small size and low power system are the two necessities for implanting a device into human body. One of the solutions is to use the CMOS technology. Silicon-based CMOS

technology has become a competitive technology for rapidly-developing wireless communications due to its low-cost, high-level integration, and a micro- or nano- meter compact size. Due to these advantages, it's possible to integrate with RF rectifier, transmitter and receiver in a small single chip and place inside the human body.

Beside the rectifier, transmitter and receiver, another challenging is to design an implantable antenna to catch RF energy and transmit data. A radiated antenna has to have at least half or quarter wavelength of desired frequency which is relative large compare to the integrated circuits. In order to integrate with CMOS technology, on-chip antenna is quite necessary. However, low efficiency, low gain and low input impedance are the common issues which most designer have faced because of the space constraint.

All the challenges mentioned above motivate the author of this thesis to do this research and seek a total solution for the energy harvesting system to meet the goal of achieving batteries-less function for portable personal device, implantable device and other possible application.

## **1.2 Goal of Research**

This thesis is mainly focused on the research listed below:

1. Principle and theoretical study of a typical schottky barrier diode (SBD) rectifier.
2. Circuit design and performance improvement of SBD and diode-connect MOSFET (DCMOS) rectifier.
3. Link budget analysis for evaluating and building up the wireless system specs.
4. Design the rectenna system and evaluate the performance in the human body environment.
5. System design and integration of the implantable device for biomedical application.



### **1.3 Results Outline**

To summarize this thesis, chapter two provides an overview of a RF rectifier based on SBD and explains the theory to better understand the operation principle. Moreover, different techniques to improve the performance of a rectifier have been discussed and compared. A limitation of the SBD will be addressed in the end of this chapter. In chapter three, this thesis switches from SBD to DCMOS in order to overcome the limitation of SBD. Different types of DCMOS will be compared such as PMOS, NMOS and Native NMOS. Furthermore, in the end of this chapter, this thesis proposed a high efficiency two-port rectifier structure with a designed dual antenna for mobile device application. A link budget analysis for an entire implantable wireless system will be presented in the beginning of chapter four. Based on the link budget analysis, a single stage diode-connect Native NMOS (DCNNMOS) rectifier and an innovative 3D on-chip antenna for Glaucoma-monitoring application will be proposed. Chapter five focuses on the integration and evaluation of the entire wireless system includes rectenna, transmitter and external receiver. Another implantable device for cardiovascular pressure monitor will be designed in chapter six to fit in carotid artery in human neck. Chapter seven is the final conclusion and future work.

## CHAPTER TWO: SCHOTTKY BARRIER DIODE RECTIFIER

### 2.1 Introduction

Schottky barrier diode (SBD) is a semiconductor diode with a very low forward voltage drop and a very fast switching action compared to a p-n junction diode. Basically, a normal p-n junction diode has a 0.7 V voltage drop typically, while a SBD is between 0.2 V to 0.4 V. This lower voltage drop is an advantage to compose a RF rectifier. The reason will be explained in section 2.1.2.

#### 2.1.1 DC Analysis of Diode

Fig. 1(a) shows a diode on the DC forward bias and Fig. 1(b) shows the I-V curve of a p-n junction diode and a SBD. As can be seen, SBD is turned on when  $V_d$  is equal to 0.3 V, but p-n junction diode has to be greater than 0.7 V. Therefore, the threshold voltage ( $V_{th}$ ) of the SBD is much lower than the p-n junction diode.

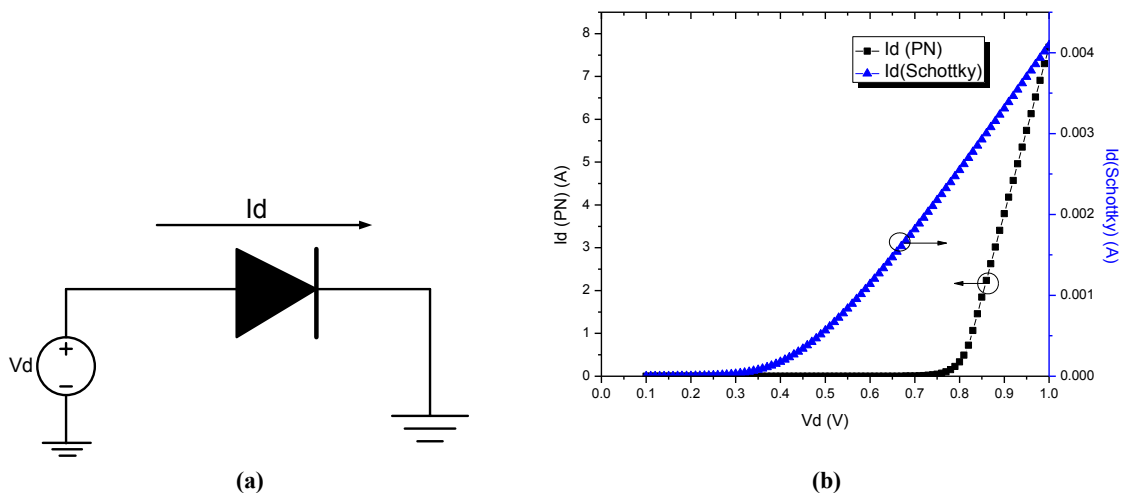


Fig. 1 (a) A diode on the forward bias (b) I-V curve of a diode on forward bias

### 2.1.2 AC analysis of Diode

Consider the AC behavior of a SBD, as shown in Fig.2 (a). The input voltage is a sine wave with amplitude of 1 V, as shown in Fig.2 (b) (blue line). While the sine wave is greater than the threshold voltage of 0.3 V, the SBD turns on, and it turns off when the voltage drops below the  $V_{th}$ . Based on this ideal experiment, the amplitude of 1V is much larger than the  $V_{th}$  of 0.3 V. However, in the real ambience, the RF energy is much lower. For example, the amplitude of a RF voltage may only have 0.5 V near the network tower. Therefore, if the  $V_{th}$  is greater than 0.5 V such as a p-n junction diode, it would not be able to turn on with this low input voltage amplitude. Thus, this is why SBDs are popular used in the RF energy harvesting circuits.

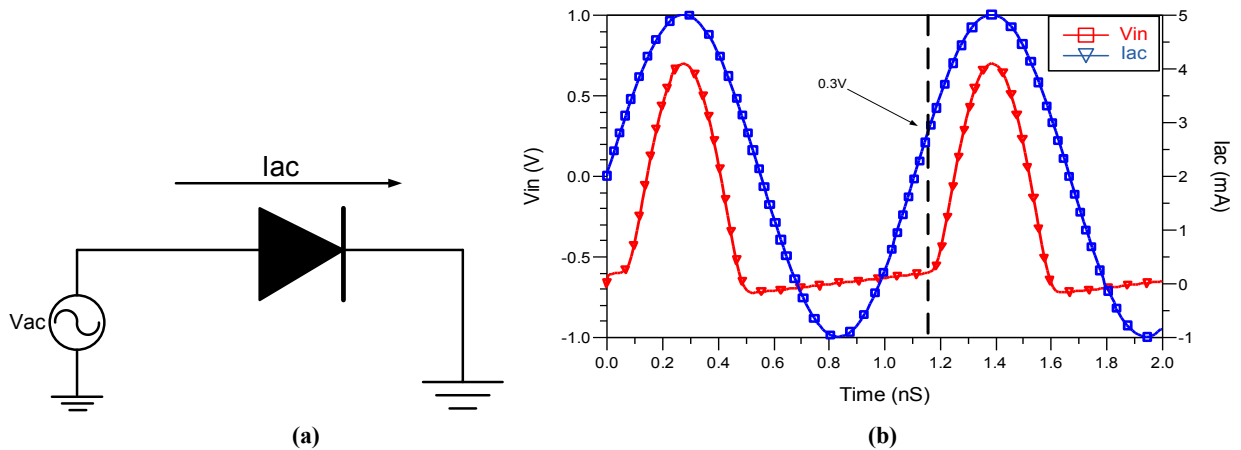


Fig. 2 (a) A diode with AC voltage source (b) Voltage and current waveform cross the diode with a voltage source

### 2.2 Theoretical Principle of The RF Rectifier

Fig.3 shows a typical circuit structure of a RF rectifier composed by two SBDs (D1 and D2) with certain  $V_{th}$  and two capacitors (C1 and C2). The output ( $V_{out}$ ) could connect with a load resistor ( $R_L$ ) or other circuits.

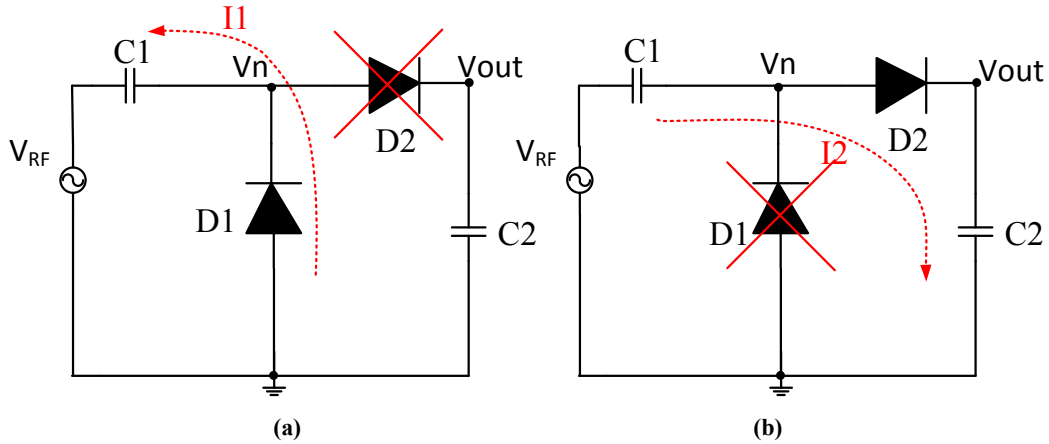


Fig. 3 The RF rectifier on (a) negative cycle (b) positive cycle

As shown in Fig.3 (a), during the negative cycle of the input signal ( $V_{RF}$ ), D2 is in the reverse bias and turns off. While decreasing  $V_{RF}$ ,  $V_n$  decreases as well. Then, D1 turns on when  $|V_n| > |V_{th}|$ . The current  $I_1$  flows from the ground to  $C_1$  and charges the capacitor to  $|V_{RF}| - V_{drop}$ , where  $V_{drop}$  is determined by the turn-on resistance ( $R_S$ ) of D1 and the capacitance of C1. When the input source switches to the positive phase shown in the Fig. 2 (b), D2 turns on when  $|V_n| > |V_{th}|$  and D1 turns off. Then, the current  $I_2$  flows from the source to charge C2. Also, in this cycle, C1 is also discharging toward C2. Therefore, the voltage of  $V_{out}$  is equal to the voltage of the source plus the voltage of C1 and minus the voltage drops by D1 and D2, which is given by (1).

$$|V_{out}| = |V_{RF}| + |V_{C1}| - 2V_{drop} = 2(|V_{RF}| - V_{drop}) \quad (1)$$

Fig.4 (a) shows the difference of  $V_{out}$  between the calculation from (1) and simulation by ADS model. The  $V_{th}$  of ADS diode model is 0.7 V and the  $V_{drop}$  is around 0.3 V for each turn-on diode. The capacitance of C1 and C2 are both 1 fF and the frequency is 10 kHz. As can be seen, the simulation results (red dots) match the calculation from (1) which is a linear line. However, by applying the TSMC SBD model to the RF rectifier, the simulation results are close to (1) only at low input voltage level. This variation is because of the parasitic capacitance which is shown in

the equivalent model [5] in Fig.5. (a). In the SBD equivalent circuit,  $C_{GEO M}$  comes from the capacitance between fingers shown in the layout in Fig.5 (b). Typically the value is around 0.1 pF to 1 pF. Resistance  $r_D$  and the capacitance  $C_J$  are both from the depletion region which are determined by the external voltage. Due to the parasitic capacitance  $C_{GEO M}$  and  $C_J$ , on the positive cycle in Fig.3 (b), these two capacitors are also discharging to generate a reverse leakage current. Once the input voltage goes higher, the reverse leakage current increases and eventually cancels the forward current. Therefore, there is a limit of  $V_{out}$ , which is around 5 V shown in Fig.4 (b).

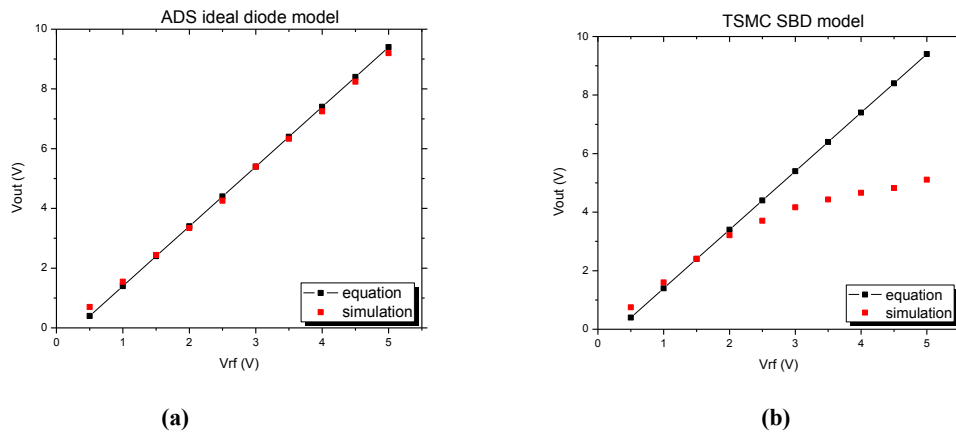


Fig. 4  $V_{out}$  versus  $V_{rf}$  of the rectifier in Fig.3 based on equation (1) and (a) ADS ideal diode model ( $V_{th}=0.7$  V) (b) TSMC SBD ( $V_{th}=0.3$  V)

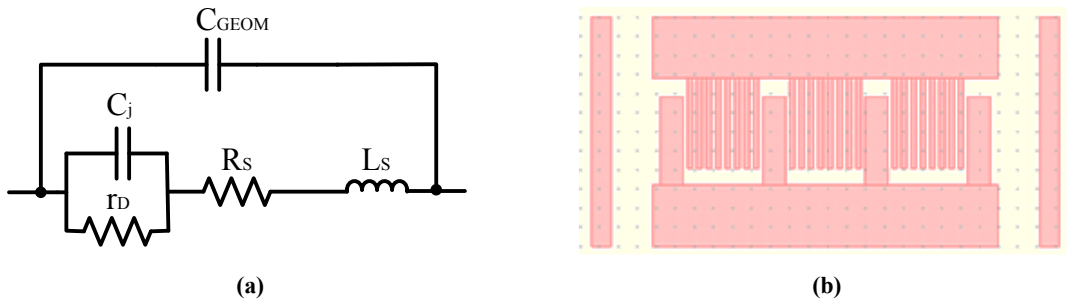


Fig. 5 (a) Equivalent circuit and (b) TSMC SBD layout

## 2.3 Function Analysis of RF Rectifier

Section 2.2 illustrated the basic theoretical principle of the RF rectifier which can generate roughly twice of the source amplitude. However, readers might still not well understand how it converts AC signal to DC output. The secret of the RF rectifier is basically taking advantages from two composed circuits which have different functions. As shown in Fig.6, a RF rectifier could be separated into two sub-circuits, Circuit 1 is a clamper and Circuit 2 is an envelope detector. In the following section, this thesis will explain these two circuits separately in section 2.3.1 and 2.3.2 in order to help the readers better understand the behavior of the RF rectifier.

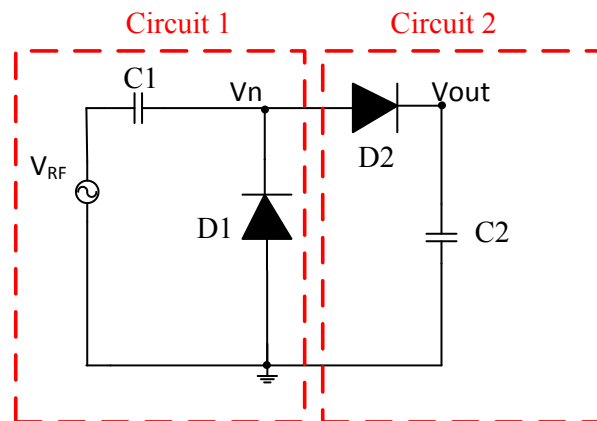


Fig. 6 Sub-circuits on RF Rectifier

### 2.3.1 Clamper

A clamper is a circuit combined with a capacitor and a diode, which could either shift the voltage reference (DC value) up (Fig.7) or down based on the diode on forward or reverse bias. There are two types of clamper: positive unbiased and negative unbiased

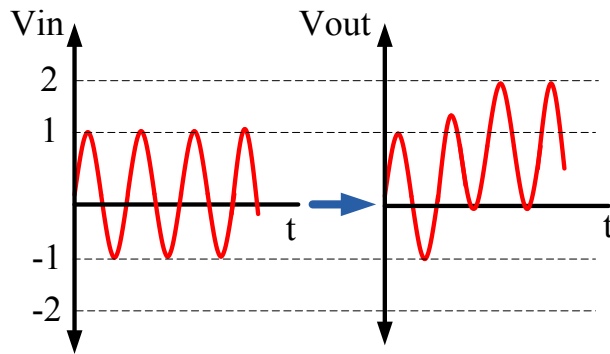


Fig. 7 The voltage reference shifts up by a clamper circuit

### 2.3.1.1 Positive Unbiased

Fig.8 shows the components and input/output waveform of a positive unbiased clamper. During the negative cycle of the input AC signal, the diode is forward biased and conducts, charging the capacitor to the peak positive value of  $(|V_{in}| - V_{drop})$ . During the positive cycle, the diode is reverse biased and thus does not conduct.  $V_{out}$  is therefore equal to the voltage stored in the capacitor plus the input voltage, which is  $(2|V_{in}| - V_{drop})$  or  $(|V_{in}| + V_{cap} - V_{drop})$ . For example, if the peak of  $V_{in}$  is 1V, the peak of the output will be 2 V when  $V_{drop}$  is equal to zero. It can be seen from the waveforms in Fig.8, the reference of the input voltage shifts up and the lowest peak of the sine wave is close to 0 V.

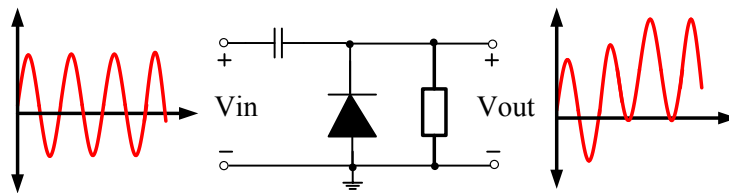


Fig. 8 Positive unbiased clamper

### 2.3.1.2 Negative Unbiased

A negative unbiased clamper is in the opposite way of positive clamper. As can be seen from Fig.9, the diode arrow direction is toward to the ground. In the positive cycle of the input

AC signal, the diode is forward biased and conducts, charging the capacitor to the peak value of  $(|V_{in}| - V_{drop})$ . During the negative cycle, the diode is reverse biased and thus does not conduct. The output voltage is therefore equal to the voltage stored in the capacitor plus the input voltage, which is  $V_{out} = -2|V_{in}| + V_{drop}$ . It can be seen from the waveforms on Fig.8, the reference of the input voltage shifts down and the peak value is below the 0 V.

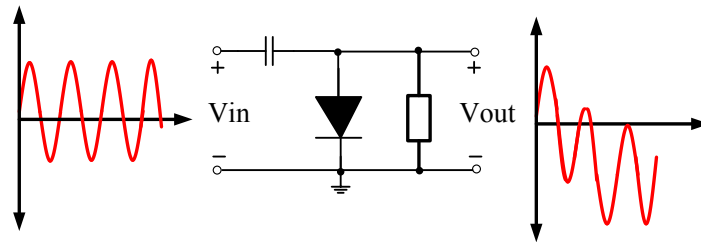


Fig. 9 Negative unbiased clamper

### 2.3.1.3 Positive Biased

A positive biased voltage clamp is identical to an equivalent positive unbiased clamp with an additional  $V_{bias}$  connected between diode and ground, which is shown on Fig. 10. The output voltage is offset by the bias amount  $V_{bias}$ . Thus,  $V_{out} = 2|V_{in}| - V_{drop} + V_{bias}$ .

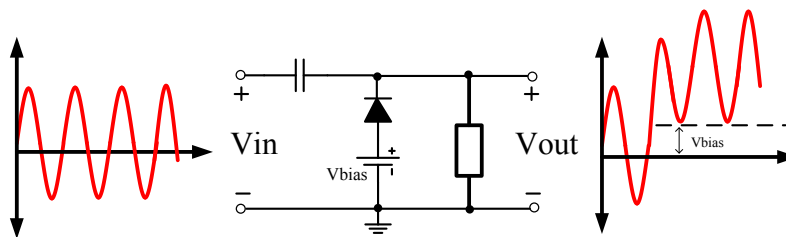


Fig. 10 Positive biased clamper

### 2.3.1.4 Negative Biased

A negative biased voltage clamper is identical to an equivalent negative unbiased clamper with an additional  $V_{bias}$  in reverse direction connected between diode and ground, which is



shown in Fig. 11. The output voltage offset by the bias amount  $V_{bias}$ . Thus,  $V_{out} = 2|V_{in}| + V_{drop} - V_{bias}$ .

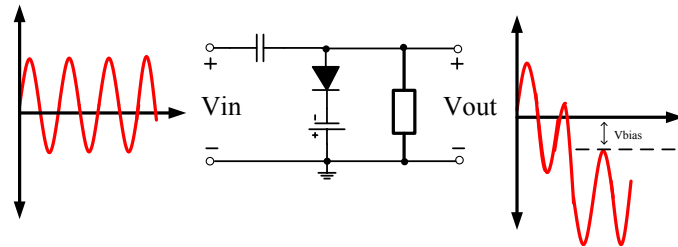


Fig. 11 Negative biased clamper

### 2.3.2 Envelope Detector

An envelope detector includes a forward biased diode and a capacitor shown in Fig.12 (a). It takes an AC signal as input and provides an output which is the envelope of the original signal. The capacitor is used for charging on the rising edge when the diode turns on, and releases voltage gradually through the load when the input signal falls. As the result, it keeps the output voltage level high once the input signal falls. The capacitance of the capacitor determines the ripple of the output voltage. Once the ripple is small, the output waveform can be seen as a smooth envelope shown in Fig.12 (b).

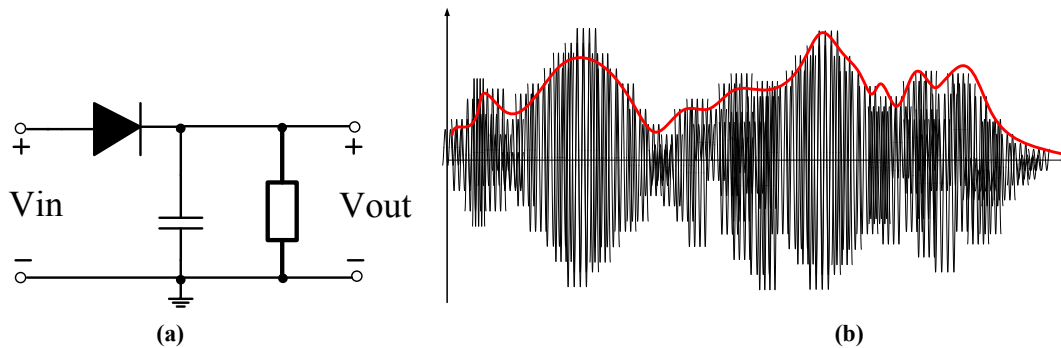


Fig. 12 Envelope detector circuit

### 2.3.3 Summary in Clamper and Envelope Detector

Review the above four types of clamper, Circuit 1 in Fig. 6 in fact is the same as positive unbiased clamper in Fig. 8. Therefore, the function of Circuit 1 is to boost up the input RF signal to a  $|V_{RF}|$  level and keep the peak to peak value the same as source signal, which means it still behaves like an AC signal. Circuit 2 in Fig. 6 performs like an envelope detector shown in Fig. 12. After the input signal goes from Circuit 1 to Circuit 2, the envelope of the shifting voltage will be tracked and shown across the load, and as the result, the output voltage behaves as a DC voltage.

Consider a typical RF rectifier shown in Fig. 13(a) and observe the waveform of voltage at node  $V_{in}$ ,  $V_n$ , and  $V_{out}$  shown in Fig. 13(b), (c) and (d). It can be seen,  $V_{in}$  is an AC sine wave with amplitude of 1 V shown in Fig. 13(a). The voltage shifts up with a level of roughly 1 V by the clamper shown in Fig. 13(c) when it goes through the node  $V_n$ . Then, the envelope of  $V_n$  has extracted to form the  $V_{out}$  by the envelope detector shown in Fig. 13(d) (pink curve). As the result, the output voltage behaves like a DC voltage which is roughly 1.7 V. Therefore, input AC signal with amplitude of 1 V can be converted into a DC signal with 1.7 V.

Fig. 14 is the result in Fig. 6 by using TSMC SBD model and 1 nf capacitor. The waveform at node  $V_{in}$ ,  $V_n$  and  $V_{out}$  are also similar to the ADS model shown in Fig. 13(d).

In brief, we can realize the RF rectifier is, in fact, combined a clamper and an envelope detector to function as an AC/DC converter. In the following sections, this thesis will introduce how to evaluate the performance of a rectifier and what are the common topologies to improve it.

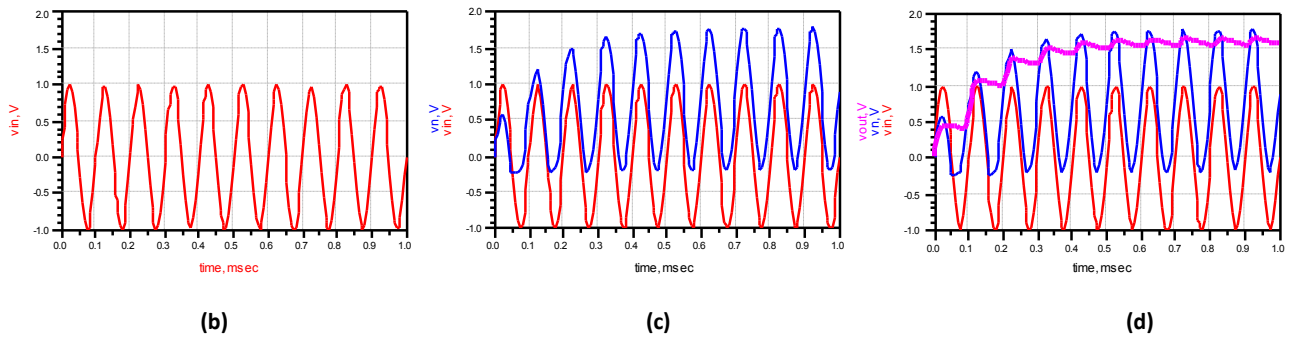
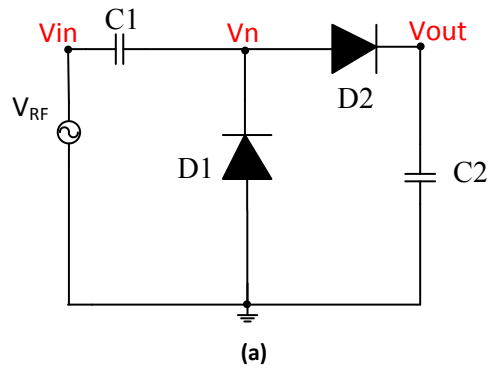


Fig. 13 Waveform at node of (b)  $V_{in}$  (c)  $V_n$  and (d)  $V_{out}$  of the rectifier (a) with ADS diode model

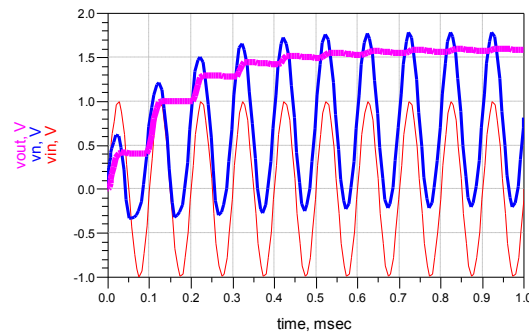


Fig. 14 Waveform at node of  $V_{in}$ ,  $V_n$ , and  $V_{out}$  of the rectifier with TSMC SBD model

## 2.4 Parameters of The RF Rectifier

This section will introduce the parameters which have been used to evaluate the performance a rectifier.

### 2.4.1 Output DC voltage ( $V_{out}$ )

RF Rectifier is an AC/DC converter and the level of DC output voltage will determine the capability to drive the load such as transmitter or receiver. For the modern low power CMOS

circuit design, the DC voltage is typically 1 V. Therefore, the goal of this thesis is to design a rectifier which is able to generate at least 1 V for charging batteries or running the lower power CMOS circuits.

### 2.4.2 Efficiency ( $\eta$ )

Efficiency is a parameter determines the power ratio between the input and output power, is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\left(\frac{V_{out}^2}{R_L}\right)}{P_{in}} \quad (2)$$

where  $V_{out}$  is the output voltage and  $R_L$  is the load resistance to represent the circuits after the rectifier. For example, if the input power from an antenna is 1 mW (0 dBm), with a rectifier of 50% efficiency, the output power will be 0.5 mW, which is half of the input power. Typically the efficiency of a rectifier is below 50% due to the loss in the diodes or transistors.

### 2.4.3 Sensitivity

Sensitivity is defined as the lowest power level which a rectifier could utilize. Higher sensitivity means the rectifier could convert even low level RF power to 1 V DC output voltage. For example, the sensitivity of a typical RF rectifier is -5 dBm, which means it is able to convert the input power of -5 dBm to 1V DC level. High efficiency rectifiers usually have high sensitivity. High sensitivity rectifier is quite difficult to design due to the limitation of the threshold voltage of diodes; once the input power level is too low, the diodes are not able to turn on.

## 2.5 Conventional Rectifiers

Consider a conventional rectifier shown in Fig. 13(a) with TSMC SBD model and Murata lump component model.  $R_L$  is  $5\text{ k}\Omega$  and both capacitors are  $100\text{ pF}$ . The simulation tool is ADS and the simulation function is harmonic balance with one-tone  $50\ \Omega$  terminal. The frequency is  $900\text{ MHz}$  which is for radio frequency identification (RFID) application. The output voltage and efficiency are shown in Fig. 15(a) and (b).  $V_{\text{out}}$  is equal to  $1\text{ V}$  and efficiency is  $8\%$  when the input power level reaches to  $4\text{ dBm}$  ( $2.5\text{ mW}$ ). That means only  $0.2\text{ mW}$  ( $2.5 \times 0.08$ ) output to the load. Why the efficiency is worse may be due to two reasons:

1. Most of the energy input is reflected because of the non-matching to  $50\ \Omega$  terminal.
2.  $R_L$  is not in the optimal value.

The first reason will be discussed in section 2.5.1 and the second in 2.5.2. Moreover, in Fig. 15, it can be noticed, the output voltage and efficiency are almost zero while  $P_{\text{in}}$  is relative low. When the  $P_{\text{in}}$  is above  $-10\text{ dBm}$  the SBDs start to work properly. Thus, it indicates that the input power has to reach a certain level in the rectifier design.

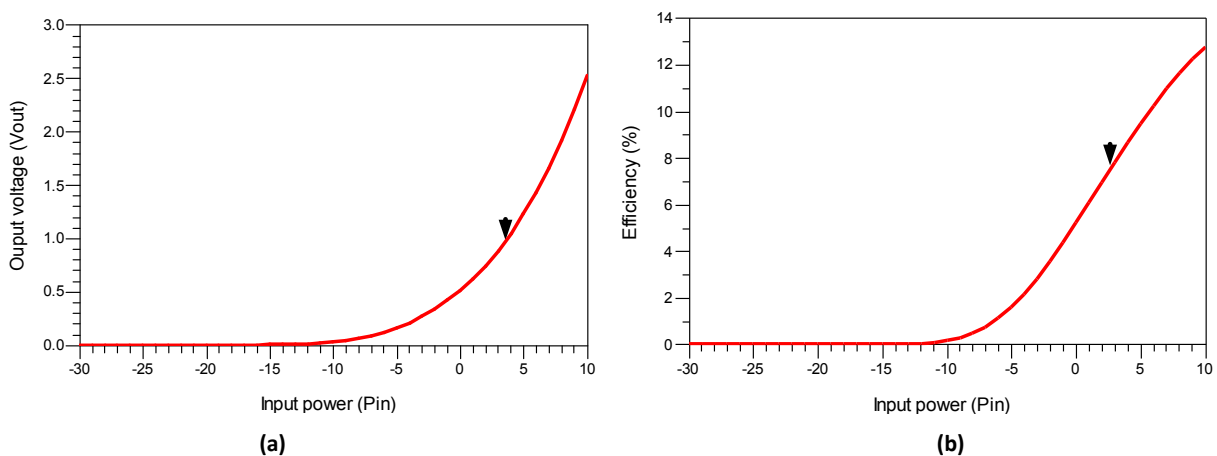


Fig. 15 (a) Output voltage (b) efficiency of the rectifier in Fig. 13(a)

### 2.5.1 Matching of RF Rectifier

Fig. 16(b) shows the equivalent circuit of a certain RF rectifier in Fig. 16(a). Since the high input capacitance of the RF rectifier, the impedance ( $Z_{in}$ ) is equal to  $(R - jX)$  and thus it could be simplified into a series capacitance ( $C_{rec}$ ) and series resistance ( $R_{rec}$ ). In order to match to  $Z_{in}$ , the source impedance ( $Z_s$ ) has to be in conjugate matching which is  $(R + jX)$ . Therefore, an matching inductor is needed to cancel the capacitance. Fig. 17 shows the impedance  $Z_{in}$  of the rectifier is equal to  $(14 - j305 \Omega)$ . High capacitance is the common issue for a RF rectifier because of the two charging and discharging capacitors and the junction parasitic capacitance of the diodes. Fig. 18 shows a matching inductor is placed between the input capacitor and the source. The optimal inductance is 54 nH. However, in reality, the Murata inductor model only has 39 nH. Thus, a series 39 nH and 3.3 nH inductor could achieve the optimal matching of  $Z_{in} = 30 - j3$ . The comparison between with and without a matching inductor are shown in Fig. 19 (a) and (b). It can be seen both  $V_{out}$  and efficiency increase dramatically with a matching inductor.

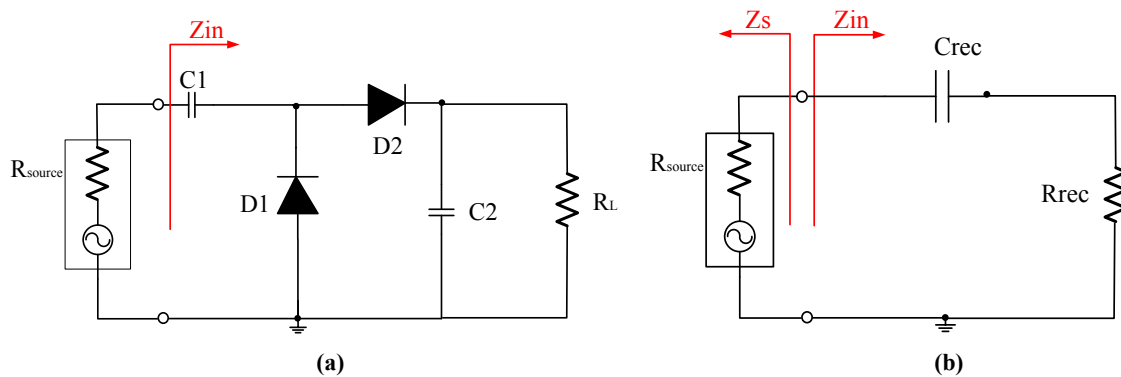


Fig. 16 (a) Conventional RF rectifier and its (b) equivalent circuit

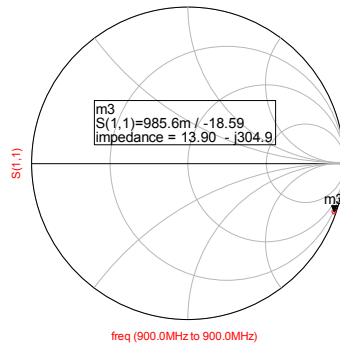


Fig. 17 Input impedance of the RF rectifier shown on smith chart

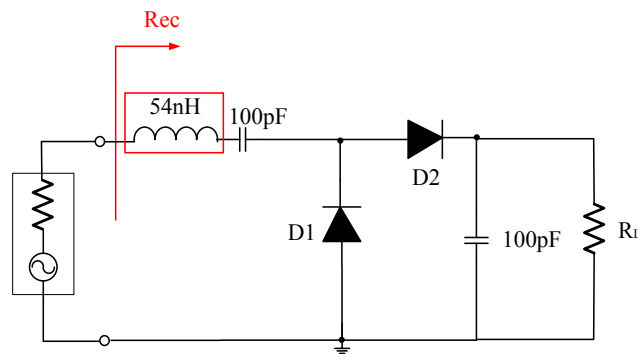


Fig. 18 The RF Rectifier with a matching inductor

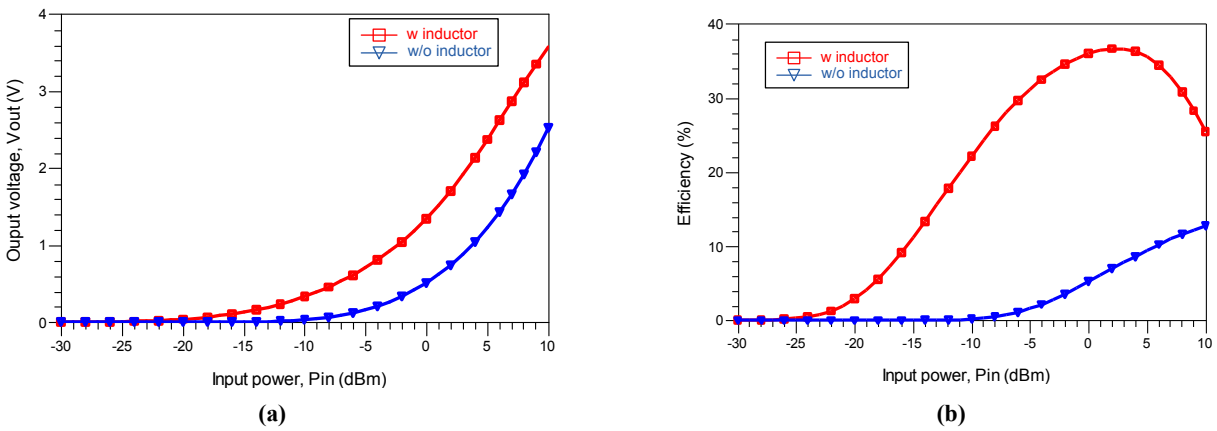


Fig. 19 (a)  $V_{out}$  and (b) efficiency versus  $P_{in}$  of the RF rectifier with and without a matching inductor

### 2.5.2 Load Effect of RF Rectifier

Another factor affects the efficiency and output voltage is the load resistance. As can be seen from (2), when  $R_L$  increases,  $P_{out}$  decreases and eventually the overall efficiency decreases.

However, the variation of  $R_L$  would change the  $V_{out}$ . For example, once the  $R_L$  increases,  $V_{out}$  will increase. Therefore, there is an optimal load resistance that could achieve maximum efficiency.

### 2.5.2.1 Optimal $R_L$

In Fig. 20(a), it can be seen  $R_L$  and  $V_{out}$  are in the direct proportion at 0 dBm input power level. However, in Fig. 20(b), the efficiency achieves maximum peak of 35% when  $R_L$  is equal to 5 k $\Omega$  and it decreases with  $R_L$  above 5 k $\Omega$ . Obviously, the trade-off between output voltage and efficiency is needed for the rectifier design.

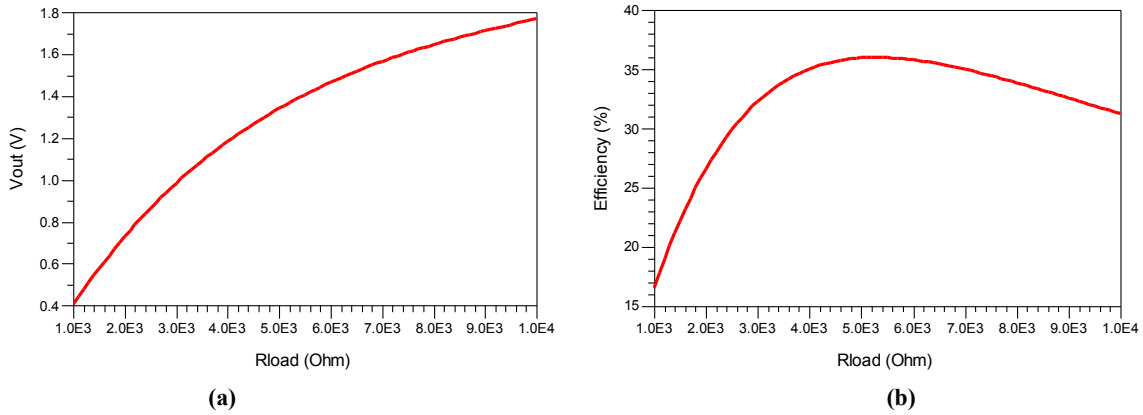


Fig. 20 Variation of load resistance versus (a) output voltage (b) efficiency at 0 dBm input power level

### 2.5.2.2 Load Resistance Compensation for Efficiency Enhancement

Fig. 20(a) and (b) are based on 0-dBm input which is on the high power level. However, the curve of efficiency versus  $R_L$  is different on input low power level shown in Fig. 21(b). On the low input power level, for example -20 dBm,  $V_{out}$  and efficiency are both direct proportion to  $R_L$ . This is because  $V_{out}$  dominates the result in (3). While the input power is extremely low, the swing of the voltage cause part of it is below the  $V_{th}$  of the diodes. The voltage input to the RF rectifier is given by (3)



$$V_{in} = \sqrt{2 * P_{in} * R_s} \quad (3)$$

where  $V_{in}$  is the voltage input to the RF rectifier,  $P_{in}$  is the input power and  $R_s$  is the source resistance. The detail derive will present in the appendix A. In the case of  $P_{in}$  equal to -20 dBm (10 uW) and  $R_s$  equal to 50Ω, the  $V_{in}$  is only 0.032 V by the following calculation.

$$V_{in} = \sqrt{2 * 0.00001 * 50} = \sqrt{0.001} = \sqrt{0.001} = 0.032$$

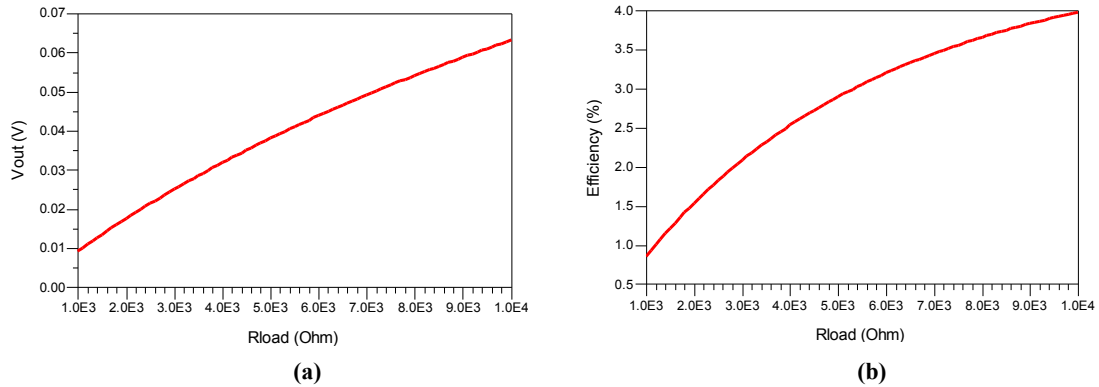
Obviously, 0.032V is lower than the  $V_{th}$  of a SBD (0.3 V). The conductive current is generated by the leakage current which is much small and can be seen as a constant. Also, the  $V_{out}$  is given by (4).

$$V_{out} = I_{out} * R_L \quad (4)$$

If the  $I_{out}$  is a constant,  $V_{out}$  and  $R_L$  will be in the direct proportion. Then we substitute (4) into (2) to derive as (5).

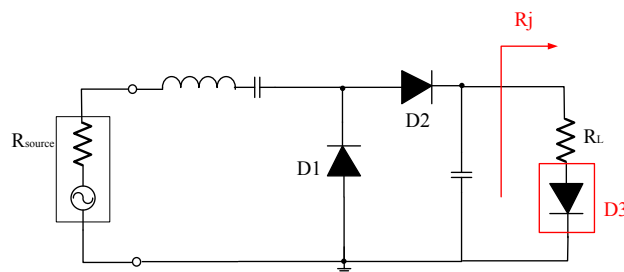
$$\eta = \frac{P_{out}}{P_{in}} = \frac{\left(\frac{V_{out}^2}{R_{load}}\right)}{P_{in}} = \frac{(I_{out} R_{load})^2}{P_{in} R_{load}} = \frac{I_{out}^2 R_{load}}{P_{in}} \quad (5)$$

From (5),  $I_{out}$  and  $P_{in}$  are constants, and therefore the efficiency is direct proportion to  $R_L$ , which can be verified in Fig. 21 (b).



**Fig. 21 Variation of load resistance versus (a) output voltage and (b) efficiency at -20 dBm**

Low efficiency on low input power level is always an issue in RF rectifier design. In Fig. 19 (b), the efficiency is only 3% at -20 dBm input. Due to the direct proportion between efficiency and  $R_L$  at this level, we can simply increase  $R_L$  to improve the efficiency. However, if we increase  $R_L$ , the efficiency at high input power level will decrease. One solution to solve this dilemma is to add an additional diode D3 below  $R_L$  which is shown in Fig 22. The total load resistance  $R_j$  is equal to  $R_L$  plus  $R_{D3}$ , where  $R_{D3}$  is the parasitic resistance of D3. The value of  $R_{D3}$  is varied with input power levels and can be a compensation for the  $R_L$  at lower power level. Fig. 23 shows the resistance  $R_j$  versus  $P_{in}$ . As can be seen, on the high input power level, the resistance  $R_j$  is almost equal to  $R_L$  which is 5 k $\Omega$ . When  $P_{in}$  decreases,  $R_j$  increases dramatically. Therefore, by applying an additional diode at the load, the efficiency on low input power level could be improved and also maintains a better efficiency on the high power level. The result is shown in Fig. 24(a) and (b). Both voltage and efficiency are improved on low and high input power level.



**Fig. 22 RF Rectifier with an additional diode to compensate the load resistance**

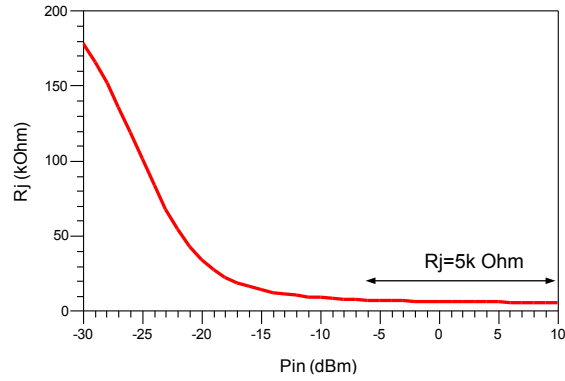


Fig. 23  $R_j$  versus  $P_{in}$  of the RF rectifier with load compensation

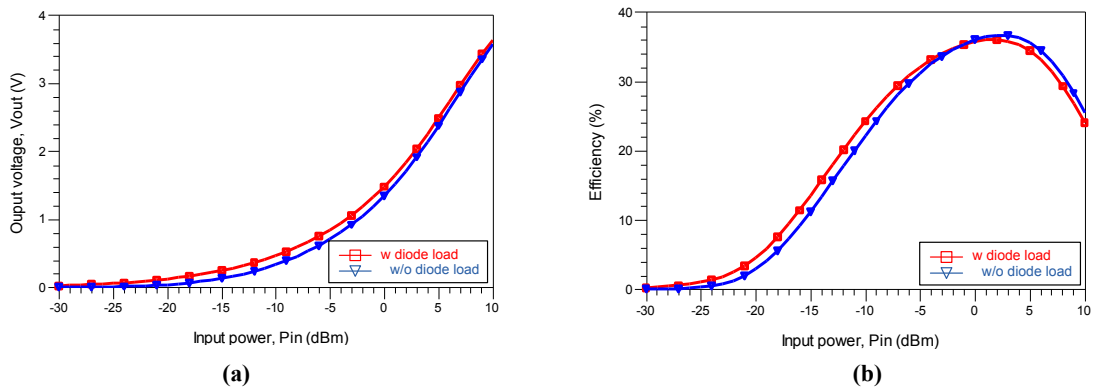


Fig. 24 (a)  $V_{out}$  and (b) efficiency versus  $P_{in}$  of the RF rectifier with and without load compensation diode

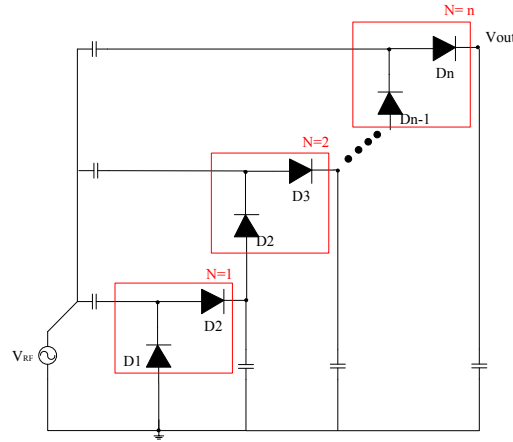
### 2.5.3 Multi-stage RF Rectifier

Instead of single-stage rectifier, one of the most popular techniques for improving the output voltage is the multi-stage rectifier, which is known as Dickson charge pump, or Dickson multiplier. Fig. 25 shows the structure of multi-stage rectifier. The output voltage  $V_{out}$  is predicted by (6).

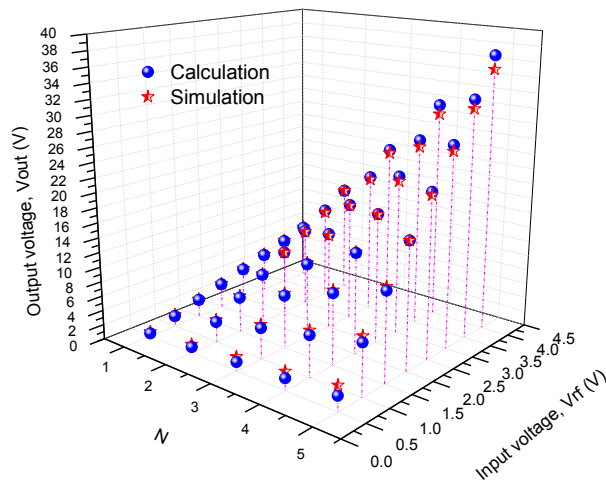
$$V_{out} = 2N( |V_{RF}| - V_{drop} ) \quad (6)$$

where  $N$  is the number of stages,  $V_{RF}$  is the amplitude of input voltage and  $V_{drop}$  is the voltage drop at each stage. Fig. 26 shows the comparison with calculation by (7) and simulation on ADS diode model. The X axis is the number of stages and Y is the input voltage and Z is the output

voltage. As can be seen, the simulation result matches to the calculation. When the number of stages increases, the output voltage also increases.



**Fig. 25 Multi-stage RF rectifier**



**Fig. 26 Comparison of simulation and calculation of multi-stage rectifier**

However, it's not always true that the number of stages is the proportion to the output voltage. Couple of factors has to be considered.

1. The value of  $Z_{in}$  when the number of stages increases
2. The efficiency of multi-stage RF rectifier
3. The overall switching delay to achieve maximum output voltage

With TSMC SBD model, the multi-stage RF rectifier can be seen as Fig.27 (a), where  $R$  is the real part of  $Z_{in}$ ,  $L_{match}$  is the matching inductor to cancel the imaginary part of  $Z_{in}$ . All the parameters including the number of stages  $N$  are listed in Table 1. Once  $N$  increases, the efficiency achieves maximum value when  $N$  is equal to 2 and it degrades while  $N$  increasing. Also, the increment of output voltage degrades while  $N$  increases. This degradation is due to the input impedance  $Z_{in}$  decreases half when adding one more stage. From the equivalent circuit of Fig. 27(a) which is shown in Fig. 27(b), the multi-stage RF rectifier can be seen as  $N$ -stage paralleled units and each unit has a resistor  $R_n$  and a capacitor  $C_n$ . More stages means more paralleled resistors, and as the result the overall resistance will decrease. Furthermore, if the input impedance is much lower than  $50\text{-}\Omega$   $R_s$ , the power from the source  $P_s$  will be reflected depends on the reflection correction  $\Gamma$  given by (7) and (8).

$$P_{in} = P_s(1 - |\Gamma|) \quad (7)$$

$$\Gamma = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \quad (8)$$

For example, if  $Z_s$  is  $5\ \Omega$ , according to (8),  $\Gamma$  is  $(5 - 50) / (5 + 50)$  which is  $-0.8$ . And then substitute  $\Gamma$  into (7) and get  $P_{in} = 0.2P_s$ . That mean only 20% energy would be fed into rectifier and 80% energy is reflected back to the source. From the Table 1, as can be seen,  $R_{in}$  is extremely small when  $N$  is 4. Therefore, the overall efficiency decreases.

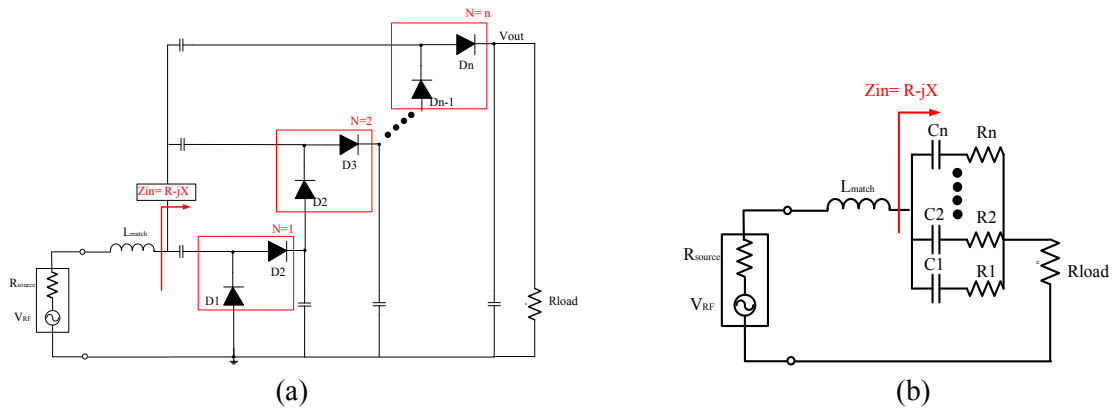


Fig. 27 (a) TSMC SBD multi-stage RF rectifier and (b) its equivalent circuit

Table 1 Parameters of multi-stage RF rectifier

N (# of stages)	$R_{in}$ ( $\Omega$ )	$L_{match}$ (nH)	$R_L$ ( $\Omega$ )	$V_{out}$ @ 0dbm (V)	Efficiency @ 0dbm
1	13.6	55	5000	1.5	45%
2	6.8	27	11000	2.4	51%
3	4.5	18	18000	2.9	46.5%
4	3.4	14	24000	3.1	39%

Another concern is the sensitivity issue of multi-stage RF rectifier. Fig. 28 shows the efficiency versus  $P_{in}$  when N is equal to 1 to 5. As can be seen, on high input power level (>10 dBm), efficiency is direct proportion to the number of stages. However, on the low input power level is in the inverse proportion. More stages means more voltage drops after each diodes, thus, once the input voltage is too low, the voltage drops diminish the output voltage in each stage. Therefore, multi-stages topology is not suitable for the low input power application.

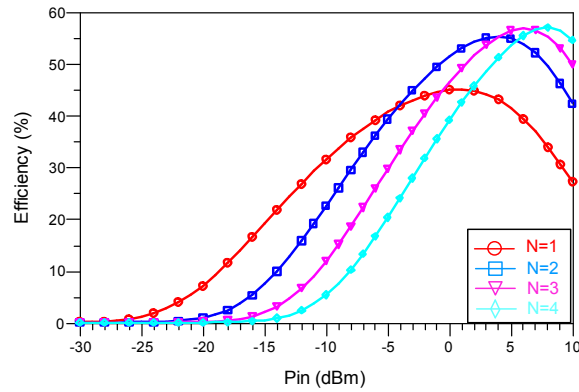


Fig. 28 Efficiency versus input power with different number of stages

## 2.6 Temperature Variation of SBD RF Rectifier

From the previous section, it can be realized that SBD has a low threshold voltage and high switching speed to fit the RF rectifier requirement. However, temperature variation is a limitation of the SBD RF rectifier. Based on the single-stage RF rectifier in Fig. 14(a), Fig. 29 shows the efficiency versus  $P_{in}$  with different temperature. As can be seen, the efficiency and temperature are in inverse proportion, and obviously, when temperature is above 80 degrees the efficiency drops dramatically. Even worse is once the temperature is above 100 degrees; the efficiency is close to zero.

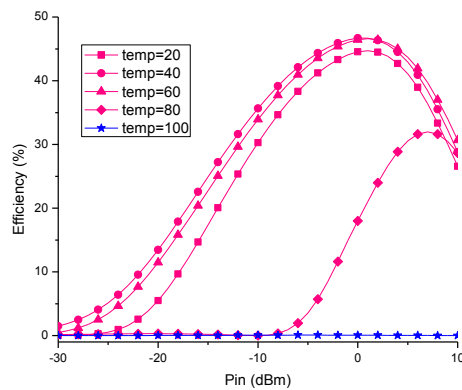


Fig. 29 Efficiency versus input power with different temperature value

This temperature variation is due to the leakage current while the diode operates in the reverse biased mode. Fig. 30(a) shows the variation of threshold voltage with varied temperature based on DC analysis in Fig. 1(a). At 100 degrees the threshold voltage is zero which means the diode behaves like a resistor. Fig.30 (b) shows with the AC source in Fig.2 (a), on the negative cycle, the current is almost zero at low temperature condition. However, once the temperature is high, the leaking current still induced even on negative bias. Therefore, the SBD is not able to perform a good switch at high temperature condition, which limits its application.

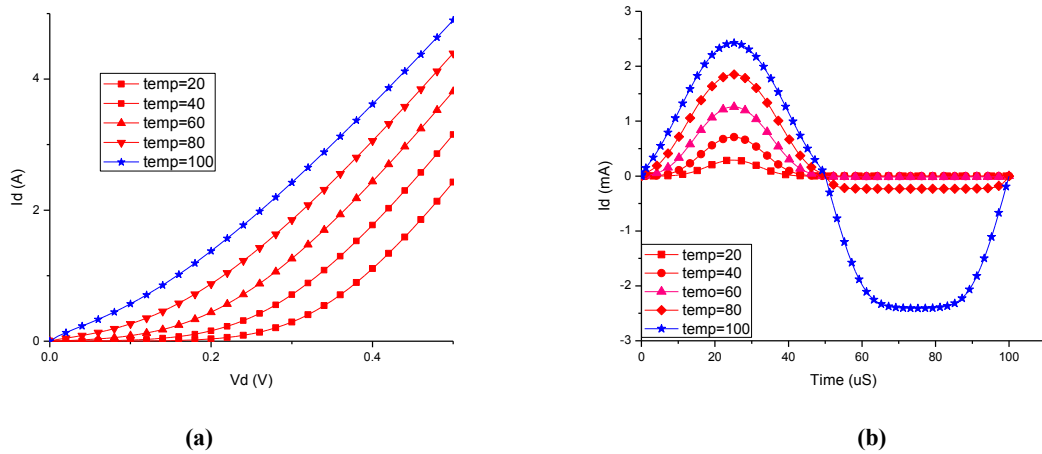


Fig. 30 Variation of threshold voltage with varied temperature at (a) DC source and (b) AC source

## 2.7 Summary

In this chapter, the basic theoretical principle of a SBD RF rectifier has been well explained and verified based on equation and ADS simulation. Moreover, different topologies for improving the performance including efficiency, output voltage and sensitivity have also been presented and compared with the conventional SBD RF rectifier. The temperature variation of the SBD has been well studied and illustrated the limitation of its application. All the simulation is using either TSMC or Murata model in order to achieve similar result of real



fabrication and measurement. Due to the limitation of SBD, in the next chapter, another approach to achieve a RF rectifier will be presented.

## CHAPTER THREE: DIODE-CONNECTED MOSFET RF RECTIFIER

### 3.1 Introduction

Review chapter two, several advantages of SBD allow it to be widely used in the wireless powered systems for quite years. However, there are some limitations which restrict its application. First, the fabrication of SBD is costly, complicated and mostly incompatible with current CMOS technology. Second, the leakage current causes the function of rectifier degrades dramatically especial above 80 Celsius degrees. In this chapter, at the beginning, this thesis will introduce an alternative way to achieve diode function by CMOS technology, and then, in the section 3.3, an innovative rectifier will be proposed to improve the sensitivity on low input power level.

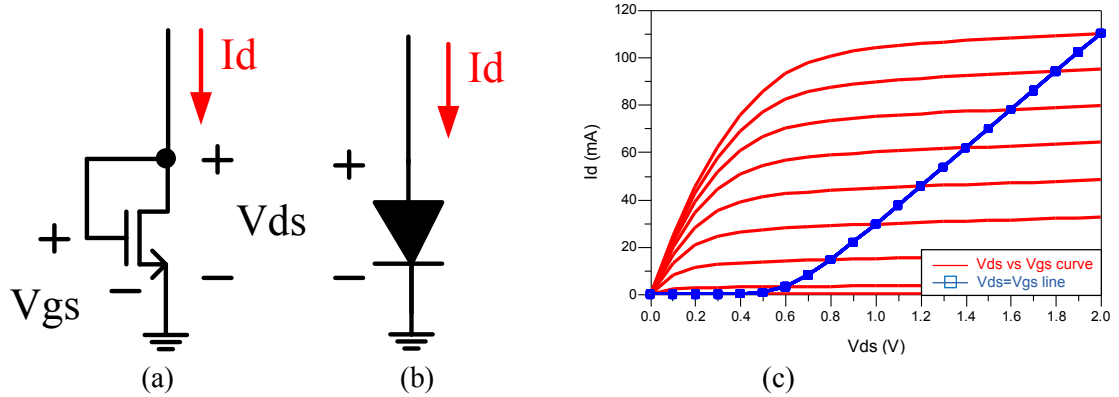
### 3.2 Diode-connected MOSFET

Diode-connected MOSFET is an alternative way to achieve the switching function as a typical diode. Based on the TSMC 0.18 $\mu$ m CMOS technology, there are different types of MOSFET which can be fabricated through silicon wafer processes, such as Nominal NMOS/PMOS, medium VT NMOS/PMOS and Native NMOS.

#### 3.2.1 Normal NMOS

Fig. 31(a) shows a NMOS which gate and drain are connected and its I-V curve is shown in Fig. 31(c) (blue line). As can be seen, based on the condition of  $V_{ds} = V_{gs}$ , this I-V curve is a linear line when  $V_{ds}$  greater than a certain value, which is similar to a diode with a certain  $V_{th}$ . Therefore, due to this characteristic, the NMOS which gate and drain are connected can be seen as a diode toward to ground shown in Fig. 31(b), and this certain NMOS can be used to replace

the SBDs in Fig. 13(a) of chapter two to form a diode-connected MOSFET RF rectifier shown in Fig. 32. The  $V_{th}$  of the diode-connected NMOS is around 0.5 V which can be read in Fig. 31(c).



**Fig. 31 (a) A diode-connected NMOS and (b) its equivalent circuit (c) I-V curves of a NMOS with and without gate and drain connected to each other**

The operation principle of a diode-connected MOSFET RF rectifier is the same as SBD RF rectifier in section 2.2 which is based on the charging and discharging process on positive and negative cycle. Also, according to section 2.5.1 and 2.5.2, the same as SBD RF rectifier, it needs to find the matching inductor  $L_m$  and optimal load resistance  $R_L$ . The diode-connected NMOS RF rectifier is shown in Fig. 33 with detail component values. The transistors M1 and M2 are using TSMC 0.18 $\mu$ m Nominal NMOS model and the off-chip lump components are by Murata model. The simulation results including output voltage and efficiency are shown in Fig. 34(a) and (b), which are also compared with the conventional SBD RF rectifier. It can be seen, the curves of output voltage both are quite the same, which demonstrates that the function of the diode-connected MOSFET is similar to SBD. However, the efficiency at low input power level of the diode-connected NMOS rectifier is lower than SBD rectifier. This is because the  $V_{th}$  of diode-connected NMOS (0.5V) is greater than SBD (0.3V), causing too low input power unable to turn on the diode-connected NMOS, as the result, the sensitivity degrades.

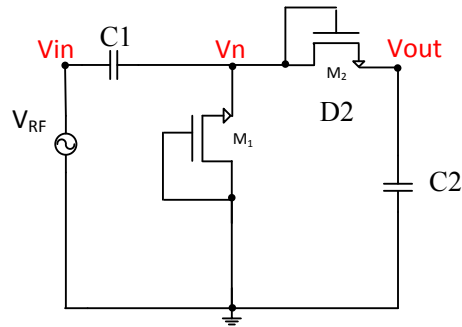


Fig. 32 Diode-connected MOSFET rectifier with two NMOS transistors

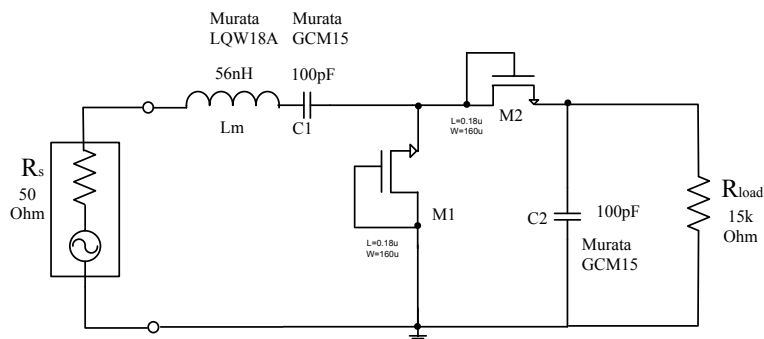


Fig. 33 A diode-connected NMOS RF rectifier with a matching inductor and 50- $\Omega$  source terminal

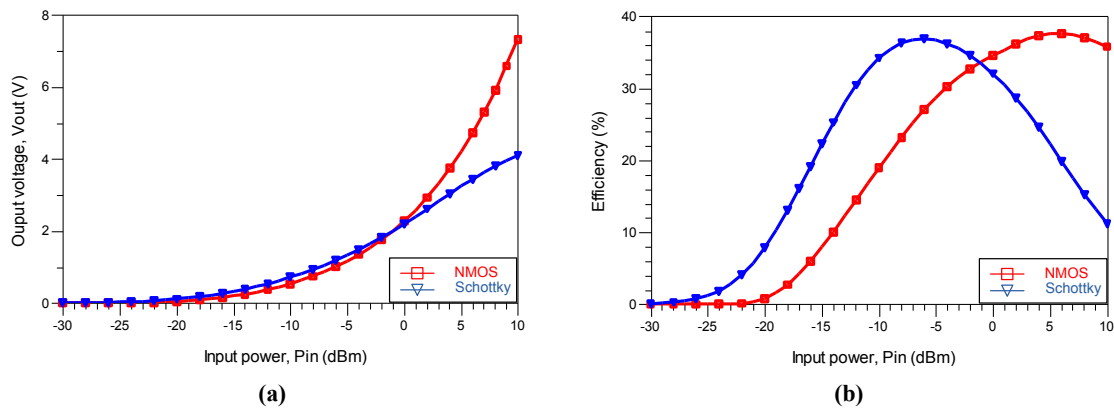


Fig. 34 (a) Output voltage and (b) efficiency of diode-connected NMOS rectifier and SBD rectifier versus input power

### 3.2.2 Normal PMOS

Except n-channel MOSFET, PMOS is also able to compose a diode-connected MOSFET. Similar to Fig.31, PMOS operates in a opposite way. Fig. 35(a) shows a PMOS with gate and drain connected and Fig. 35(c) is the I-V curve when  $V_{ds} = V_{gs}$ . As can be noticed, the PMOS

turns on when  $V_{sg} > V_{th}$ . The  $V_{th}$  is roughly 0.4 V which is lower than NMOS. The diode-connected PMOS RF rectifier circuit is shown in Fig. 36 with detail values of transistors and and. Fig. 37 shows the simulation result compared with diode-connected NMOS RF rectifier.

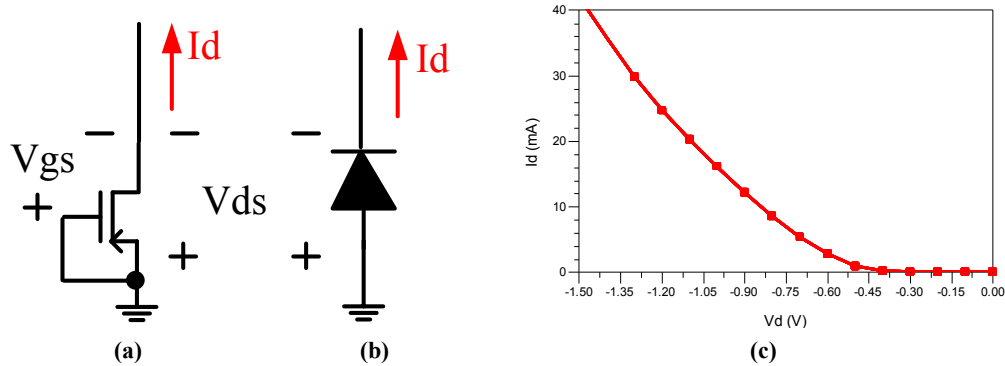


Fig. 35 (a) A diode-connected PMOS and (b) its equivalent circuit and (c) I-V characteristic curves

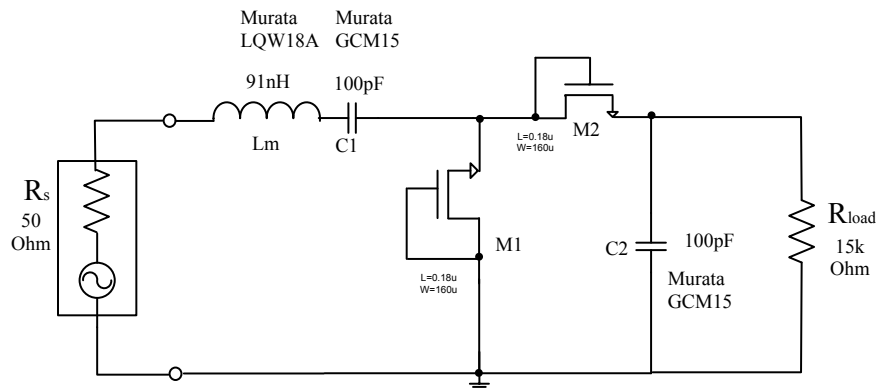


Fig. 36 A diode-connected PMOS RF rectifier with a matching inductor and 50-Ω source terminal

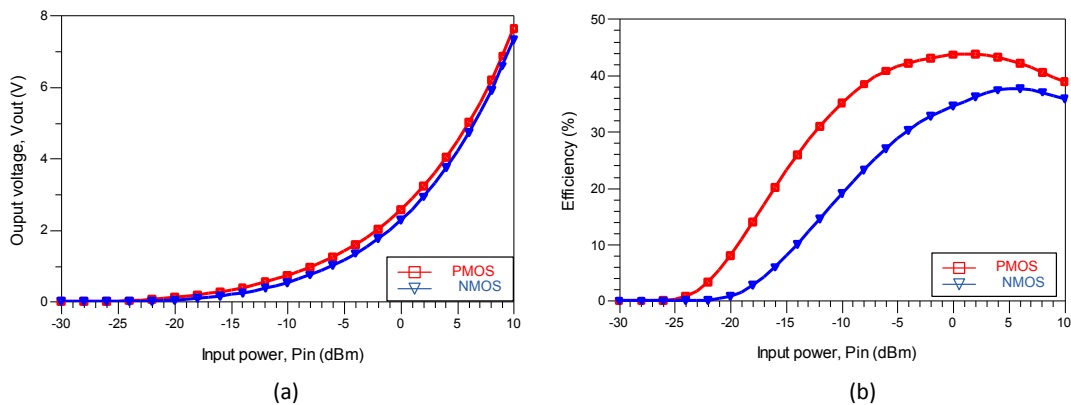


Fig. 37 (a) Output voltage and (b) efficiency of diode-connected MOSFET RF rectifier with PMOS and NMOS versus input power

### 3.2.3 Native NMOS

A native transistor or natural transistor is a variety of the MOS field-effect transistor without p-well or n-well shown in Fig. 38 and mostly with n-channel native transistor. Compared with normal NMOS and PMOS technology which are built in the heavily doped p-well or n-well, Native NMOS is built only in the lightly doped p-substrate, and therefore, the threshold voltage is almost zero ( $\sim 0.1$  V). The comparison in threshold voltage of a diode-connected MOSFET with Normal NMOS and Native NMOS is shown in Fig. 39. Fig. 40 shows the diode-connected Native NMOS RF rectifier and Fig.41 shows its simulation result compared with different types of RF rectifier.

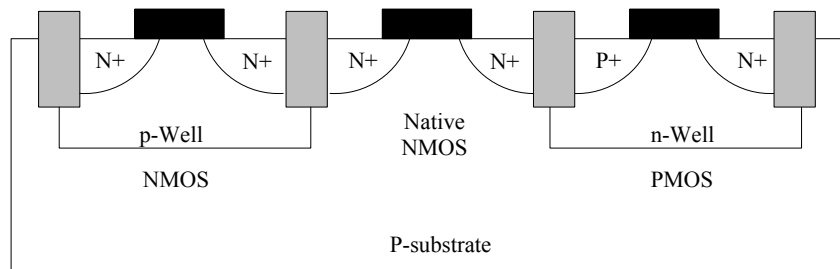


Fig. 38 Cross-sectional view of CMOS technology

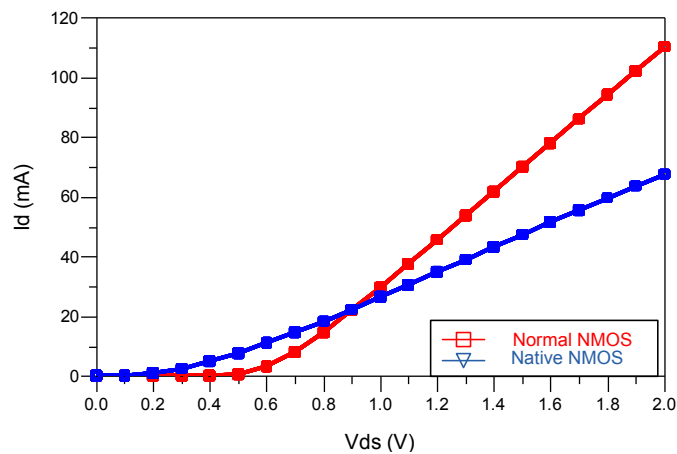


Fig. 39 I-V curve of diode-connected MOSFET with Normal NMOS and Native NMOS

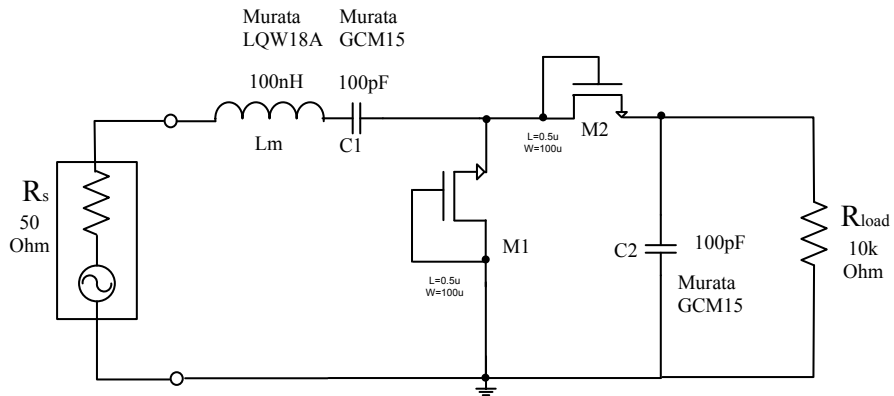


Fig. 40 A diode-connected Native NMOS RF rectifier with a matching inductor and 50-Ω source terminal

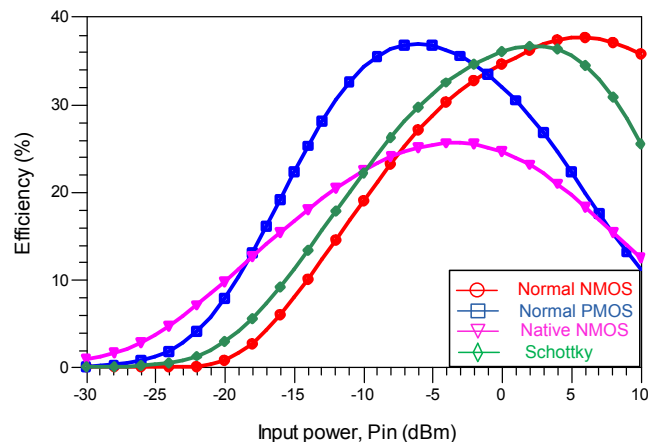


Fig. 41 Comparison in Efficiency versus input power of the diode-connected MOSFET rectifier with NMOS, PMOS, Native NMOS and SBD

As can be seen in Fig. 41, thanks to the low threshold voltage of Native NMOS, at low power level, it performs a good efficiency compared with other technology. However, due to the size restriction of Native NMOS with 100  $\mu\text{m}$ , the current is smaller compared with Normal NMOS and PMOS transistors. Therefore, the efficiency at high level input power is lower than others. Table 2 is the parameter summary of diode-connected MOSFET RF rectifier with Normal NMOS and PMOS, Native NMOS, and SBD. All the technologies have their own strength and weakness. Thus, the designers have to pick the suitable technology for related application in order to achieve maximum performance.

**Table 2 Parameters and performances comparison in different technologies**

Param. Tech.	$Z_{in}$ ( $\Omega$ )	L (nH)	$R_L$ ( $k\Omega$ )	Efficiency (%) @0 dBm	Efficiency (%) @-20 dBm	$V_{out}$ (V) @0 dBm	$V_{out}$ (V) @-20 dBm
Normal NMOS	56	91	1.5	34.5	0.8	2.3	0.04
Normal PMOS	5	100	1.5	43.7	8	2.6	0.1
Native NMOS	343	100	10	24.6	9.8	1.7	0.1
SBD	30	54	5	35	2.9	1.3	0.04

### 3.3 Three-port RF Rectifier

#### 3.3.1 Introduction

Review the chapter one, one of the goals of this thesis is to design a high sensitivity RF rectifier which is able to utilize the weak RF energy in our ambience for charging the batteries or running the low power device. High sensitivity means low input power level, and the efficiency and output voltage of a RF rectifier degrade once the input power decreases. One solution is to increase the load resistance ( $R_L$ ) to improve the output voltage. However, increasing  $R_L$  may decrease the efficiency. It is quite difficult to have a good efficiency ( $> 10\%$ ) and usable output voltage ( $> 1V$ ) at the same time, especial at the low input power level ( $< -15$  dBm). Thus, many



trade-offs and tuning efforts in efficiency and output voltage occurs when designing the RF rectifier.

There are two ways to improve the low power sensitivity: either by reducing the diode threshold voltage or by boosting the input voltage. Preview the relevant studies in this area. [6][7][8][9] used the self or external  $V_{th}$  cancellation topologies to increase the sensitivity. However, the variation of output voltage of the RF rectifier itself varies with the input power level. A slightly output voltage changed causes the efficiency degrades dramatically. Moreover, stable external voltage biasing requires an additional voltage source and eventually the power consumption and cost will increase. [10] used different matching networks, which requires a 5.6 MOhm optimal load to boost the input voltage. Furthermore, the common problem occurs from the previous references is the load variation effect which will be discussed in chapter two, section 2.5.2. The best performance mostly is based on the optimal load resistance, but usually we are not able to anticipate what the other circuits behind the RF rectifier. As the result, the load resistance is unknown.

In this section, this thesis will provide three solutions to solve the issues: 1. Reducing threshold voltage 2. Boosting input power 3. Minimizing load resistance variation effect. From section 3.2.3, diode-connected Native NMOS has low threshold voltage and better sensitivity at low input power, and thus, it's the best candidate for high sensitivity rectifier design to achieve the first solution. The next is how to boost the input voltage. The solution is to combine more power from different antenna sources. Once the input power level increases, the input voltage will be boosted up a level. Therefore, a three-port RF rectifier with two antennas is proposed in later section in order to double the input power into the RF rectifier. Finally, the issue of the

load variation will be minimized by adding an additional diode load which is similar to the section 2.5.2.2.



Fig. 42 (a) two-port and (b) three-ports RF rectifier block diagrams

### 3.3.2 Three-port RF Rectifier Design

Fig. 42(a) is a conventional two-port RF rectifier (one input and one output) which has an antenna and a matching network to match rectifier to 50Ω. Fig. 42(b) is the proposed three-port RF rectifier network. The first different is the proposed rectifier combined the matching circuit into the rectifier, and it does not need to design an extra matching network for 50 Ohm terminal. The second is the two antennas double the power into the RF rectifier. Due to the high frequency, the power fed into RF rectifier from antennas is not as simple as one plus one equal to two. Without any modification, the power feeds into the RF rectifier is not twice of the power from one antenna. It depends on the matching condition form each port. In the following section, this thesis will discuss how to feed maximum power form two antennas to the RF rectifier.

### 3.3.3 Lossless Three-port Network

Consider a three-port network with two inputs and one output is shown In Fig. 43. The source resistances and power at port1 and port2 are  $R_1, P_1$  and  $R_2, P_2$ . The load resistance is  $R_3$  and output power is  $P_3$ . At the node n, the two source impedances are  $Z_1$  and  $Z_2$ , and the impedance toward the output is  $Z_3$ . If the three-port network is lossless and source 1 is identical to source 2, then statement (9) and (10) will be true.

$$I_1 = I_2 \tag{9}$$

$$I_3 = I_1 + I_2 = 2I_1 \quad (10)$$

The power  $P_3$  at the output is given by (11), and  $P_1$  is given by (12)

$$P_3 = I_3^2 Z_3 \quad (11)$$

$$P_1 = I_1^2 Z_1 \quad (12)$$

Then we substitute  $I_3$  in (11) by (10). We can get the (13)

$$P_3 = I_3^2 Z_3 = (2I_1)^2 Z_3 = 4I_1^2 Z_3 \quad (13)$$

The lossless condition at this three-port network is given by (14)

$$P_3 = P_1 + P_2 = 2P_1 = 2I_1^2 Z_1 \quad (14)$$

Finally, plug (14) into (13), the relation between  $Z_1$  and  $Z_2$  is given by (15).

$$Z_1 = 2Z_3 \quad (15)$$

Therefore, for a lossless three-port network, at node n, the impedance toward the load must be one half of the impedance toward either source 1 or source 2. In our case, the two input terminals are 50- $\Omega$ , thus  $Z_3$  has to be 25  $\Omega$  to achieve maximum power transfer shown in Fig. 43(b).

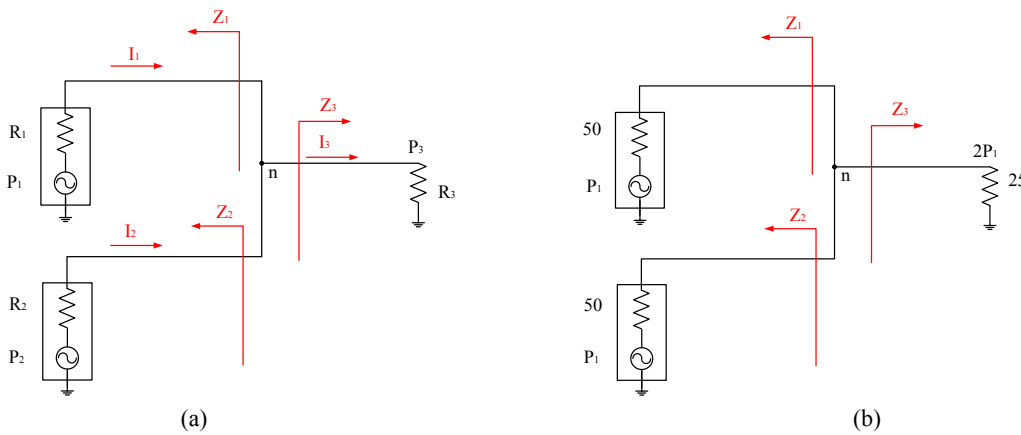


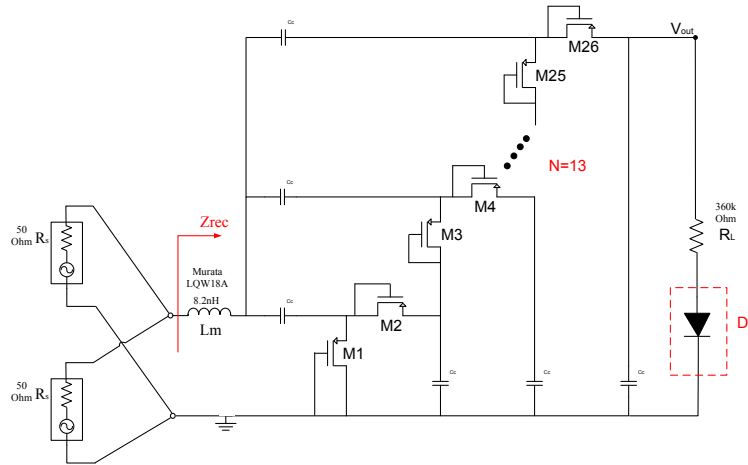
Fig. 43 (a) A arbitrary three-port network (b) A lossless three-port network

### 3.3.4 Multi-stage Diode-connected MOSFET with Native NMOS

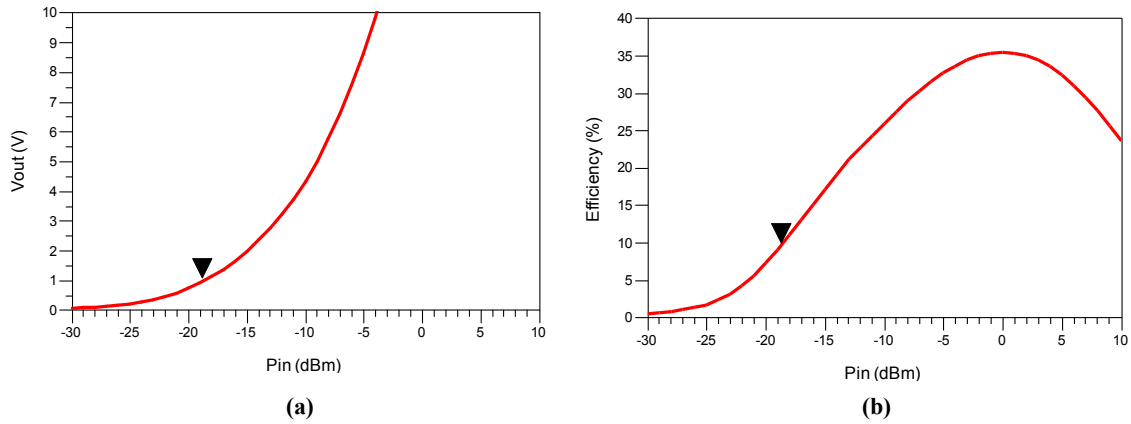
Observe the impedance  $Z_{in}$  in Table 2, it can be noticed this impedance is quite large for a diode-connected Native NMOS RF rectifier, which is around 300  $\Omega$ . According to the section 2.5.3, the multi-stage technique for RF rectifier could decrease the input impedance since more paralleled resistance in the equivalent circuit in Fig. 27. Also, in order to achieve the three-port rectifier, the number of stages depends on the output impedance  $Z_3$  which is  $\frac{1}{2} Z_1$ . In this case, both the sources impedance are 50- $\Omega$ , thus, the input impedance of the multi-stage RF rectifier dhas to be 25 $\Omega$  to achieve maximum power transferred. Fig. 44 shows the proposed three-port 13 stages RF rectifier with a load resistance compensation diode ( $D_L$ ). 13 stages are able to have a 25- $\Omega$  input impedance ( $Z_{rec}$ ) to achieve a maximum power transferred with two 50- $\Omega$  input terminals. The inductor  $L_m$  is used to cancel the input capacitance of the RF rectifier. The optimal  $R_L$  is 360 k $\Omega$  to achieve best efficiency and output voltage of 1 V. Due to the two input power sources, the efficiency of (2) in chapter two will be revised into (16).

$$\eta = \frac{P_{out}}{P_{in,total}} = \frac{V_{out}^2}{(2P_{in})R_{load}} \quad (16)$$

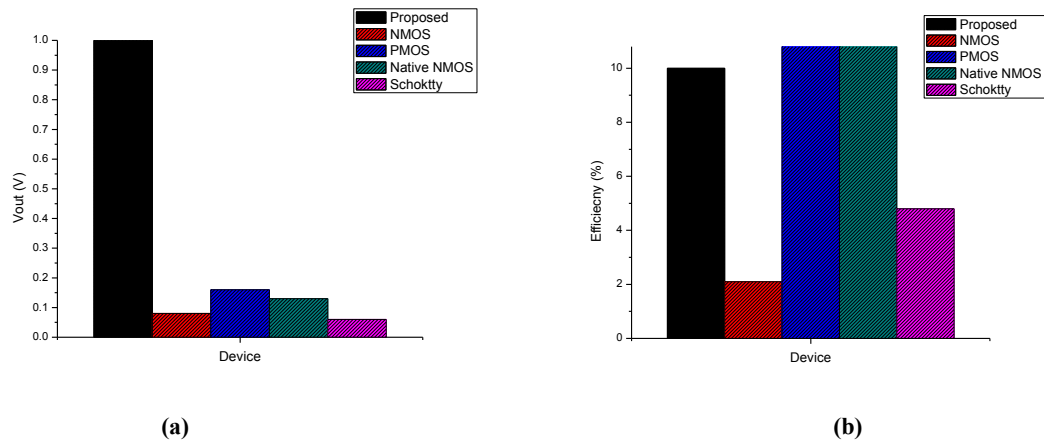
The simulation result of output voltage and efficiency are shown in Figs. 45(a) and 45(b). The sensitivity of the proposed RF rectifier at 900MHz could achieve -18.5dBm (14 $\mu$ W)  $P_{in}$  with 1 V  $V_{out}$  and 10% efficiency, which is able to utilize weak RF power in such a environment.



**Fig. 44 Proposed three-port 13 stages diode-connected Native NMOS RF rectifier with a load resistance compensation diode.**



**Fig. 45 (a) V<sub>out</sub> versus P<sub>in</sub> (b) Efficiency versus P<sub>in</sub> of proposed three-port RF rectifier**



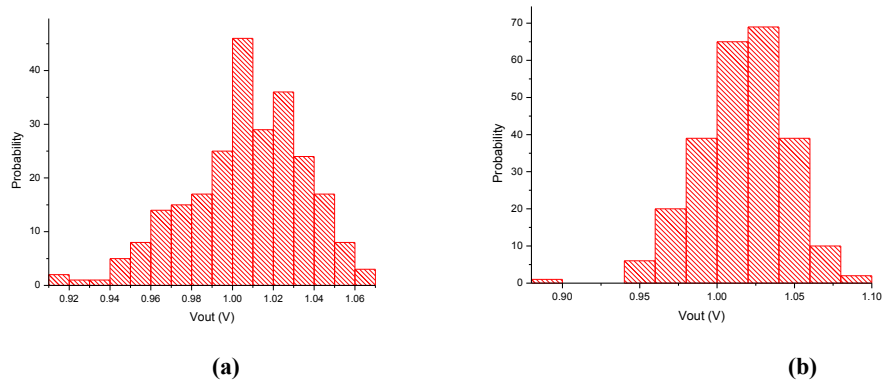
**Fig. 46 The simulation results of (a) output voltage at -20 dBm (b) Efficiency at -18.5 dBm with different rectifier approaches**

Fig.46 shows the efficiency and output voltage of the proposed RF rectifier compared with different rectifier approaches. As can be seen, the proposed RF rectifier could achieve 10% efficiency and 1V output voltage at the same. The rest approaches may achieve 10% efficiency but the output voltages are below 0.2 V which are unable to recharge the battery or run the low power devices.

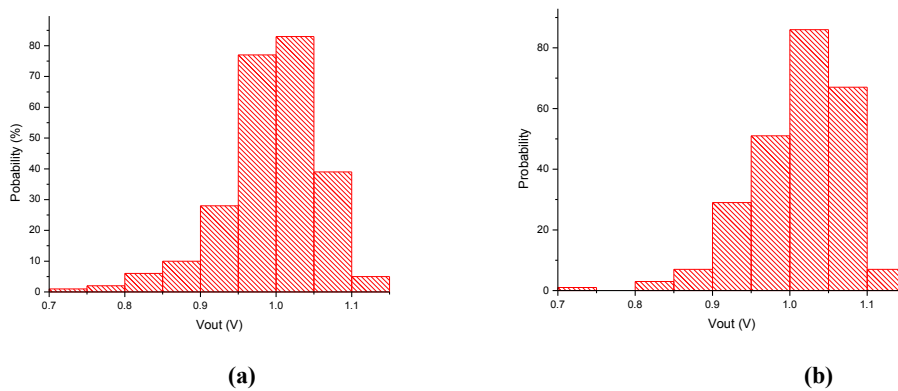
### 3.3.5 Load Resistance Variation

In Fig. 44, a load resistance compensation diode ( $D_L$ ) is added below the load resistor ( $R_L$ ). In chapter two, Fig. 23, the total resistance  $R_j$  is the same as  $R_L$  at high power level and to be infinity when the power level is extremely low. Thanks to this characteristic, the load resistance compensation diode dominates the total resistance at low input power level and eventually the  $R_L$  variation effect can be minimized. Fig. 47(a) and (b) show the probability histogram at different voltage based on +/-10% variation of load resistance. Fig.48 (a) and 48 (b) show the 20% variation. These simulations are achieved by ADS Monte Carlo function for the proposed rectifier operates at -18.5 dBm input power at 900 MHz frequency. The optimal load is 360 k $\Omega$  and the range of 10% variation is from 356.4 k $\Omega$  to 363.6 k $\Omega$ , and 20% variation is from 352.8 k $\Omega$  to 367.3 k $\Omega$ . As can be seen in Fig. 47 and Fig. 48, without the resistance compensation diode the voltage less than 1 V has scattered more frequently than the one with compensation diode. Due to the goal of this design is to maintain at least 1 V voltage when the load resistance varied, we can sum all the probabilities which are above 1 V and find the average probability over 1 V with 250 samples. The simulation result is shown in Table 3. With the load resistance compensate diode the probability to achieve at least 1 V output voltage is close to 90% at 10% variation, which means the proposed RF rectifier is more insensitive to the change of

load resistance. Moreover, 20% variation is also shown in the Table 3. With the compensation diode, the probability is 14% which is higher than the one without compensation diode both on 10% and 20% variation.



**Fig. 47** Load resistance variation of +/-10% with 250 samples (a) without load compensation (b) with load resistance compensation diode



**Fig. 48** Load resistance variation of +/-20% with 250 samples (a) without and (b) with load resistance compensation diode

**Table 3** Comparison of the probability to achieve output voltage of 1V w/o load resistance compensation diode

Item \ Load resistance	The probability of the output voltage above 1 V	
	10% variation	20% variation
With $D_L$	89%	64%
Without $D_L$	75%	50%

### 3.3.6 Temperature Variation

According to section 2.6 in chapter two, SBD RF rectifier is not suitable for the high temperature operation due to the leaking reverse current. On the other hand, diode-connected MOSFET has a better performance while the temperature is high. Fig. 49(a) and 49(b) shows the output voltage and efficiency based on the temperature variation from  $-20^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  of the proposed RF rectifier. As can be seen both efficiency and output voltage are reverse proportion to temperature. Although the temperature degrades all the performance, diode-connected MOSFET RF rectifier still perform 10% efficiency and 3.5 V output voltage at  $P_{in}$  equal to -8 dBm at  $100^{\circ}\text{C}$ . The minimum  $P_{in}$  to generate 1 V output is -13 dBm. Therefore, compared with the SBD RF rectifier, diode-connected MOSFET has better chance to work well in the harsh environment.

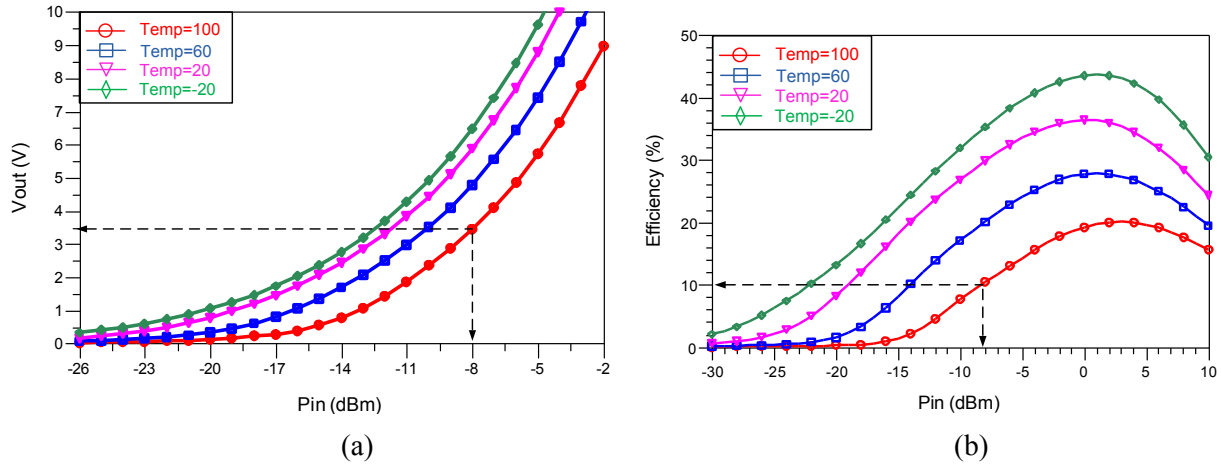


Fig. 49 (a)  $V_{out}$  and (b) efficiency versus  $P_{in}$  with different temperature

### 3.3.7 Compared with Papers

Table 4 is the comparison with different papers. As can be seen, this work has a good sensitivity ( $-18.5$  dBm) without any additional voltage source or programming effort. Also, the load variation is not been considered in others papers.

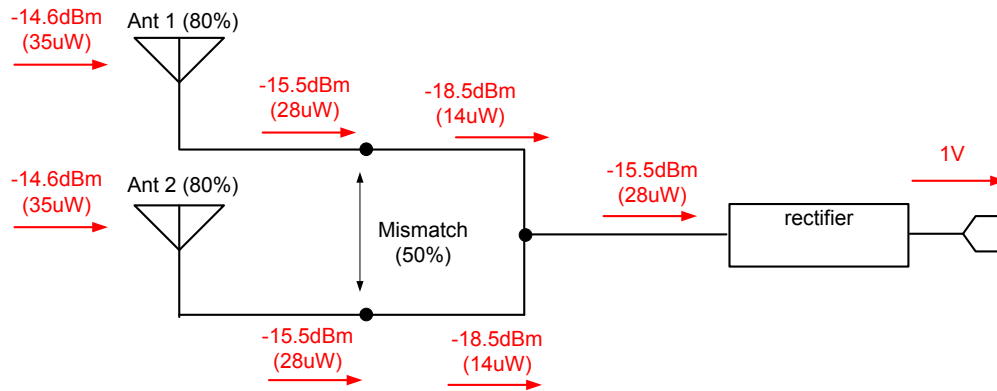


**Table 4 Proposed RF rectifier compares with different papers**

Design	This work	[1]	[2]	[3]	[4]
Technology	0.18um	0.3um	0.35um	0.5um	0.25um
Efficiency	10% @900MHz -18.5dBm	1.2% @950MHz -14 dBm	15% @953M Hz -9dBm	14.5% @869 MHz -20dBm	8.6% @906 MHz -20dBm
Output voltage	1V	1.5V	>1V	1.5	2.2V (5.6MΩ)
Programming for addition voltage source	NO	NO	NO	Yes	Yes
Load compensation	Yes	No	No	No	No

### 3.4 Antenna Design

In order to achieve maximum power feeding into the RF rectifier, the efficiency of the antenna for the three-port RF rectifier has to be more than 80%. Fig. 50 shows the block diagram of the proposed RF rectifier system. For the worst case, assume that power inputs the rectifier is -15.5 dBm, and thus the power from each port is -18.5dBm because of the maximum power transferred. Due to the 50% mismatched from 50-Ω antenna to the 17-Ω system, the power will be half reflected and therefore there is a 3 dB loss cause from the mismatch. Also, the efficiency of the antenna would not be 100%. If the efficiency is 80%, the minimum input power that can generate 1 V voltage after rectifier is -14.6 dBm, which is the limitation of this system.



**Fig. 50** Block diagram of the proposed three-port RF rectifier system

Consider different types of antennas, due to the mobile device applications, inverted-F antenna (IFA) is the best candidate because it's compatible with PCB design without additional matching components. Also, it's easy to put it as an external antenna as a portable charger. Fig. 41 is the proposed IFA antenna for the rectifier. The whole size is 125 mm x 60 mm which is the same as the size of Samsung Galaxy S3. Two IFA antennas, branch1 and branch 2, feeding in two ports are placed on the top and bent on the corner to fit the case of the device. The distance between ground and radiation element is 5mm. A shorting pin in the middle is for tuning the matching. Two IFAs are designed to share the same shorting pin in order to save space and increase the bandwidth. The simulation is using HFSS which is shown in Fig. 52. All the simulation are taken the dielectric loss (loss tangent: 0.0027) and metal loss (copper) into account. The simulation results at 900MHz are shown in Fig. 53 and Fig. 54. The input return loss both at IFA 1 and IFA 2 are below -10 dB and the efficiency are 83% which are higher than the spec.

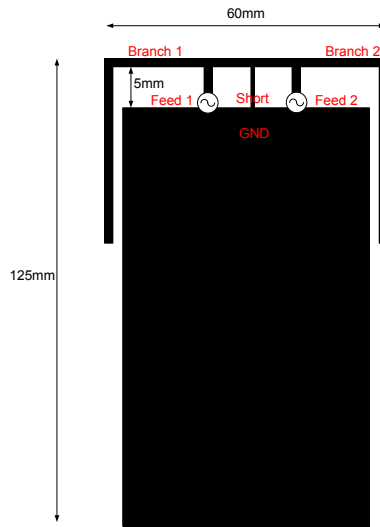


Fig. 51 Layout of the designed two IFAs

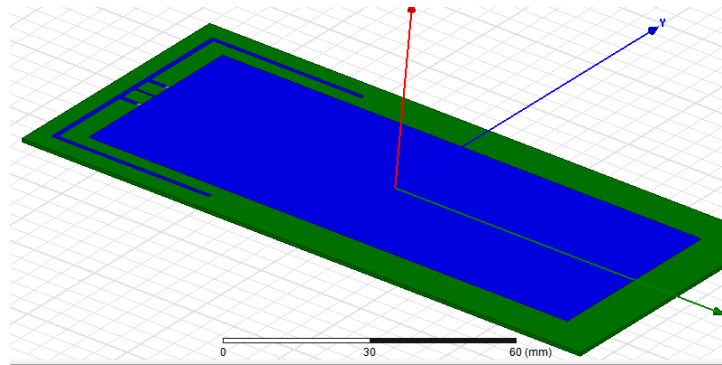


Fig. 52 HFSS simulation model (Blue is copper and green is the dielectric substrate)

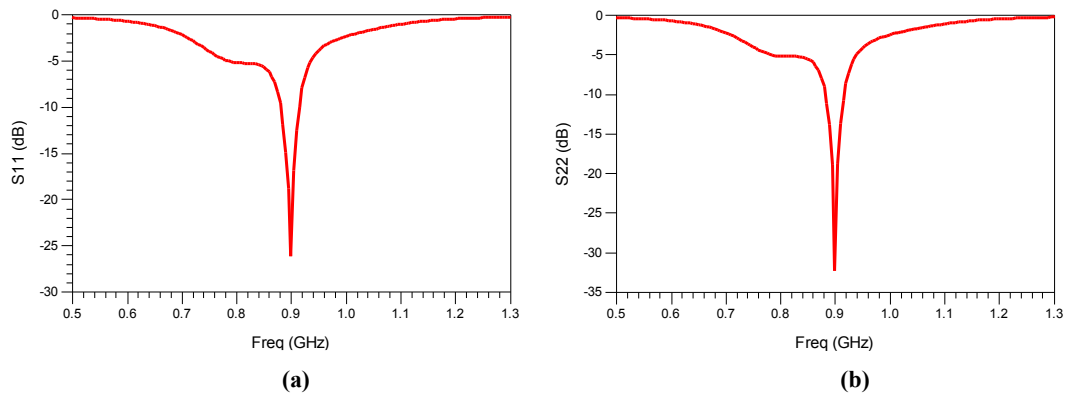


Fig. 53 (a) Return loss at (a) IFA 1 and (b) IFA 2

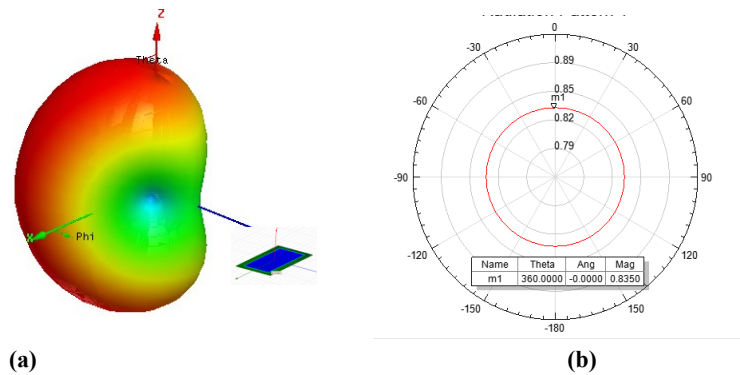


Fig. 54 (a) 3D polar plot (b) radiation efficiency of the designed IFA

### 3.5 Summary

In this chapter, different types of diode-connected MOSFET for RF rectifier are presented and also compared with the SBD RF rectifier in chapter 2. At low power level environment, Native NMOS is the best technology for RF rectifier and therefore the proposed rectifier in the end of this chapter is based on this technology. The proposed 13-stage three-port RF rectifier with load resistance compensation diode can achieve sensitivity of -18.5 dBm with 1-V output voltage and 10% efficiency. Moreover, the compensation diode can minimize the variation of load resistance which affects the performance of the RF rectifier seriously. With the compensation diode, 1-V output voltage can be achieved with the probability of 89% based on 10% load resistance variations. In section 3.4, two IFAs designed for the mobile devices are also presented to show the overall RF rectifier front end system. The sensitivity of the proposed rectifier and antenna system is -15 dBm to generate 1-V DC output.

## CHAPTER FOUR: ON-CHIP RECTENNA FOR BIOMEDICAL APPLICATION

### 4.1 Introduction

Review chapter two and chapter three, all the lump components are off-chip, which are often employed in the RF rectifier design since off-chip components have better Q value (less losses), and therefore can achieve better efficiency. However, external components increase cost and occupy large area in a PCB, which is hard to apply for biomedical applications. Recently, biomedical implantable device for such as Glaucoma or heart and eye pressure monitor are widely been researched and designed. [1] and [2] proposed a fully wireless implantable system for detecting cardiovascular pressure and eye pressure with MEMS and ASIC. However, these antennas are designed separately with the main chip, which takes the risk to fail the whole system. In order to solve this problem, this chapter will provide a co-design integrated system solution with antenna, rectifier, and transmitting circuit in a single chip for biomedical application. Fig. 55 illustrates the receiving and transmitting antennas placed outside and inside human body. Human body may be the eye, skin, vessels or muscles. The external source is a reader which can transmit RF energy to the RF rectifier inside the human body and power up the whole implanted chipset. When the chipset wakes up, it starts to work and sends data back to the reader. Then, the patient or the doctor can read the data to evaluate the health condition. In order to put the chipset inside the human body, the first requirement is to have battery-less technique otherwise surgery will be needed to take out the device in human body. The second requirement is the RF rectifier has to generate enough voltage and current to drive the whole transmitter and sensing IC. Therefore, the efficiency is the most important parameter which has to be concerned.

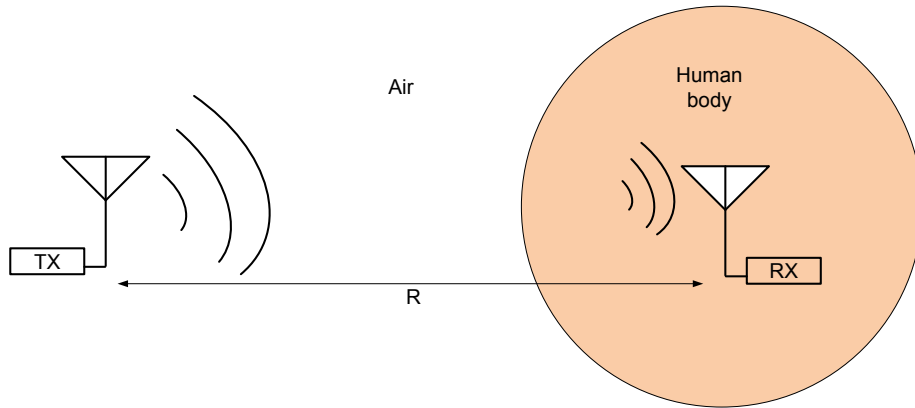


Fig. 55 The communication between external source and implanted device

## 4.2 Link Budget Analysis

Regarding the system design, link budget analysis is the first step to evaluate and build up the specs for each circuit. The designed wireless system operates at 5.8 GHz of ISM band. Why to choice this frequency is based on two reasons. First, lower frequency causes longer wavelength and eventually the antenna has to occupy large area. Second, too high frequency degrades the RF to DC efficiency of a RF rectifier and decreases its input impedance, causing large power reflection from the receiving antenna. Therefore, 5.8 GHz is the best operation frequency to maintain enough efficiency and keep the size small.

According to Federal Communications Commission (FCC) rules for unlicensed wireless equipment operating in the ISM Bands (5.725 to 5.875 GHz), the maximum transmit output power, fed into antenna is 30 dBm (1 watt) and the maximum effective isotropic radiated power (EIRP) is 36 dBm (4 watt). Thus, the output power from the external source antenna has to be less than 36 dBm. Then, the path loss in the air from the source to the implanted device is given by (16)

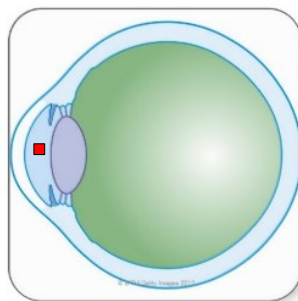
$$path\_los(dB) = 20 \log \frac{4\pi d}{\lambda} \quad (16)$$

where  $d$  is the distance between two devices and  $\lambda$  is the wavelength at operation frequency. At 5.8 GHz, we can simply calculate the loss is roughly 21 dB at 5 cm distance. 5 cm distance is maximum distance for the reader to power up the implanted IC. The application distance is between 1 and 5 cm. For example, Fig. 56 shows the application of an eye pressure detector close to the human eye and similar way for the heart pressure or other implanted IC.



**Fig. 56** Use an external reader to receive the data of eye pressure from the IC inside human eyes.

Moreover, the loss in human body for the implanted antenna has to be taken into account. This chapter uses human eyes for example, the chip must be placed 5 mm inside the Anterior chamber of human eye with high-permittivity ( $\epsilon_r = 68$ , loss tangent = 0.2677<sup>[4]</sup>) aqueous humor which composed with 98% water, which is shown in Fig. 57.



**Fig. 57** Implanted chip inside the Anterior chamber. <sup>[4]</sup>

Also, once the internal antenna integrated on-chip, the substrate loss of silicon ( $\epsilon_r = 11.9$ ) would degrade the antenna efficiency in a large amount.

Fig. 58 illustrates the entire wireless system for biomedical sensing application. The output power of each function blocks are designed and predicted based on the loss mentioned above. The external receiving sensitivity is usually at least  $-35$  dBm by most wireless communication technology such as Zigbee which has  $-60$ -dBm sensitivity. Table 5 shows the designed link budget for the whole system. Once designer have a system link budget we can know what the specs for each circuit and the limitations of the design are.

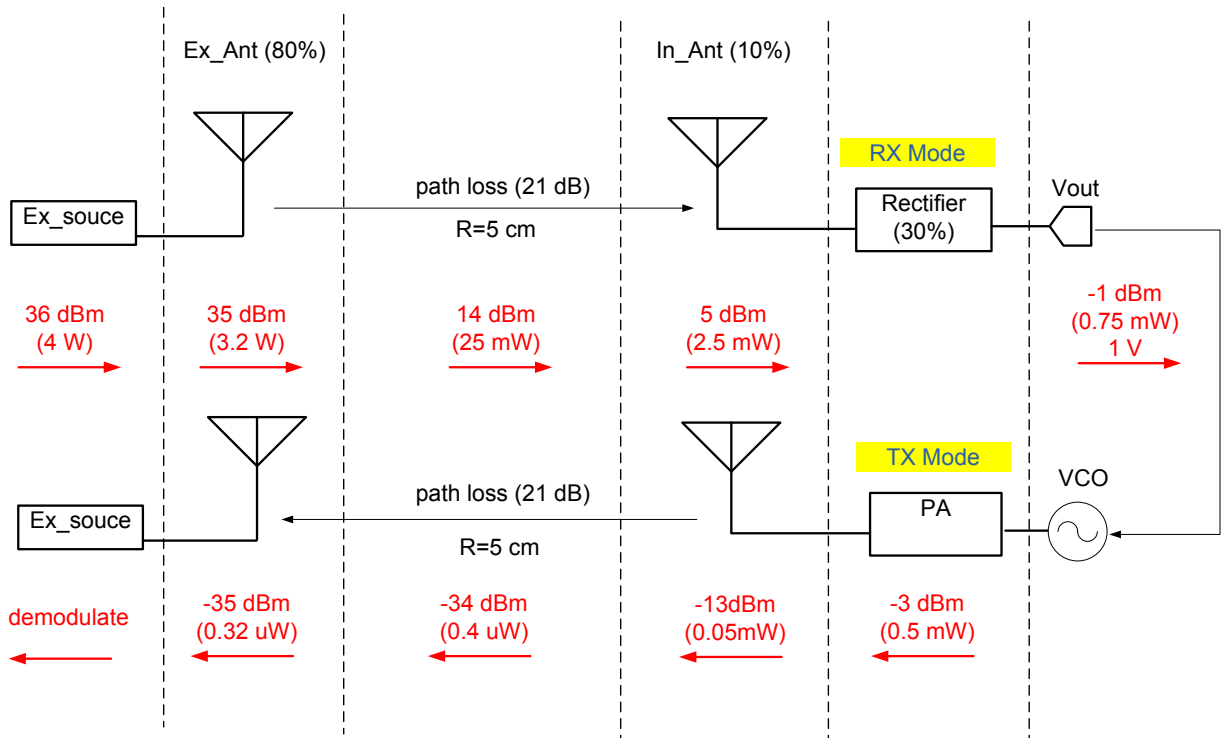


Fig. 58 Link budget block diagram of the biomedical wireless system

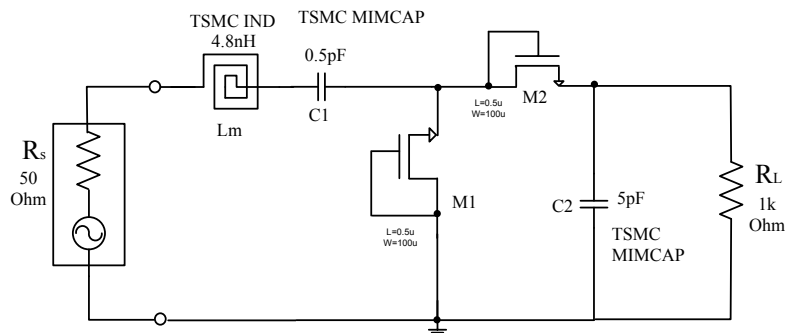


**Table 5 Link budget table of the biomedical wireless sensing system**

Item	External source	External antenna	Internal Antenna	Internal rectifier/PA	Output voltage
Efficiency		80%	10%	30%	
RX mode	36dBm	35 dBm	5 dBm	RF/DC	1V
TX mode	A/D	-35 dBm	-13 dBm	-3 dBm	

### 4.3 RF Rectifier for Biomedical Application

Based on the link budget analysis, the input power of the worst case to the rectifier is 5 dBm (3 mW) at 5.8 GHz. Higher frequency demands on high speed switching diode to improve RF to DC efficiency. Therefore, Native NMOS with almost zero threshold voltage mentioned in chapter three is the best candidate for the RF rectifier for biomedical application. Due to the on-chip requirement, all the models of this work are used TSMC 0.18 $\mu$ m technology including shielding spiral inductors, MIM capacitors, and Native NMOS transistors which are shown in Fig. 59. The simulation results are shown in Fig. 60(a) and (b). The designed RF rectifier can provide 1-V output voltage and 1- mA output current with 30% efficiency, which is able to drive a 1-k $\Omega$  load. The input impedance ( $R_{rec}$ ) is 26  $\Omega$  and  $S_{11}$  at 5.8 GHz is -10 dB shown in Fig. 61 which indicates 10% power reflected at 5.8GHz.



**Fig. 59 5.8-GHz diode-connected Native NMOS RF rectifier with TSMC 0.18 $\mu$ m models**

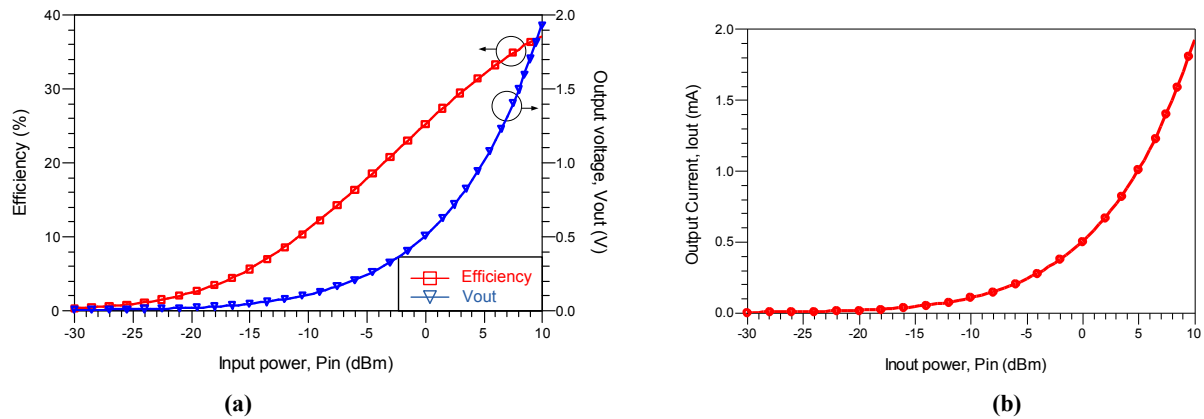


Fig. 60 (a) Output voltage and (b) efficiency of the designed RF rectifier

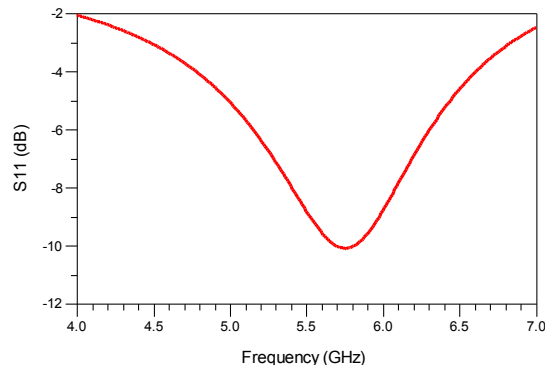


Fig. 61  $S_{11}$  of the designed RF rectifier

## 4.4 On-chip Antenna Design

### 4.4.1 Introduction

From section 4.1, we know the rectenna (antenna plus rectifier) system for the biomedical application has to be implanted into human body, eye or tissues. Therefore, integrated the antenna into silicon wafer is needed in order to have a system chipset with compact size. However, many challenges and limitations in the on-chip antenna design which have to be overcome.

First of all, frequency and size are the main issues of antenna design for biomedical application. Lower frequency causes longer wavelength. For example, the half wavelength of 5.8

GHz is 25 mm which is extremely large to put in human eye. Thus, recent researches [11 - 14] on on-chip antenna are commonly operated in the range of millimeter wave; 35-GHz, 60-GHz and 94-GHz are popular frequency for on-chip antenna. However, as to RF rectifier design, higher frequency degrades the RF to DC efficiency. Fig. 62 shows the curve of the efficiency versus frequency of the RF rectifier in Fig. 59. As can be seen, the efficiency is in the inverse proportion to the frequency and once the frequency is above 10 GHz, the efficiency is less than 10%. The reason are first higher frequency see the transistors as short circuits and the DC voltage cannot be generated and, second, the input impedance of the rectifier shown in Fig. 59 drops dramatically when frequency gets higher, which can be seen in Fig. 62 (blue line). When the impedance is too small, the mismatch from the antenna causes the power reflected and eventually decreases the efficiency. Also, high frequency degrades the transmitting and receiving distance because it's direct proportion to the loss in free space given by (16). Therefore, the RF rectifier is almost impossible to operate in mm-wave frequency by modern CMOS technology.

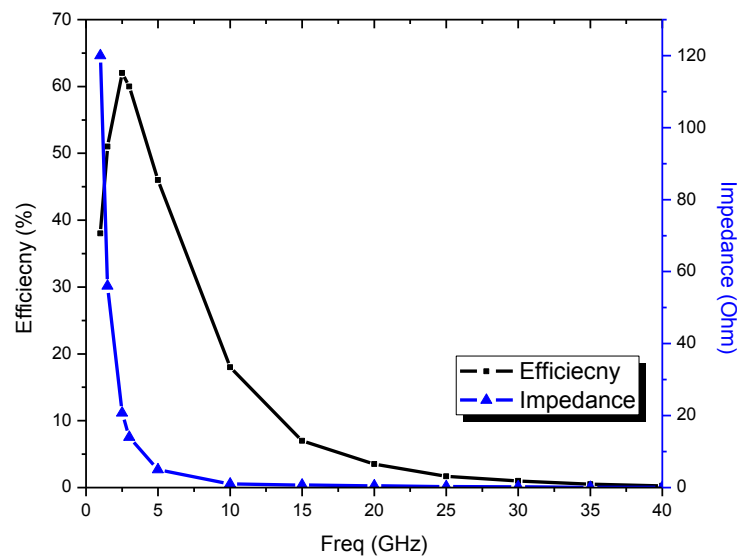


Fig. 62 Efficiency and input impedance versus frequency of the designed RF rectifier

The second challenge for the on-chip antenna is the large loss on silicon substrate and metal, which degrades the antenna efficiency. The antenna efficiency ( $e_{cd}$ ) is given by [16]:

$$e_{cd} = \frac{P_{rad}}{P_{rad} + P_{ohmic}} \quad (17)$$

where  $P_{rad}$  is the total power radiated by the antenna and  $P_{ohmic}$  is the antenna ohmic losses including conduction loss and dielectric loss. The trace of the on-chip antenna is on the top metal layer (M6) of the silicon wafer shown in Fig. 63 which shows a simplified CMOS process stack-up. All the metal layers between M6 and Si-substrate are not shown. The loss tangent of silicon substrate is 0.005 and the conductivity is  $10 \Omega$  and 0.001 of silicon dioxide. The impedance of a typical M6 with 10- $\mu\text{m}$  width on a silicon wafer is  $120\Omega$  at 5 GHz. All these dielectric loss of Si and  $\text{SiO}_2$  and conduction loss increase  $P_{ohmic}$  given by (17) and eventually decrease the antenna efficiency dramatically.

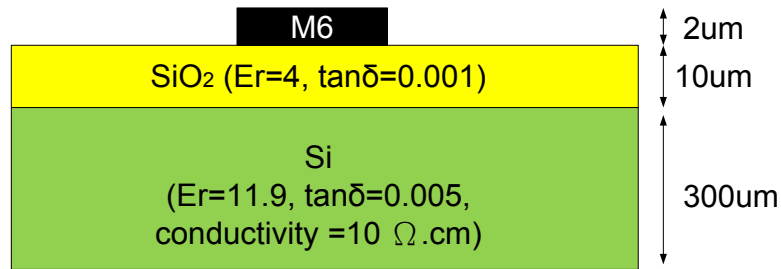
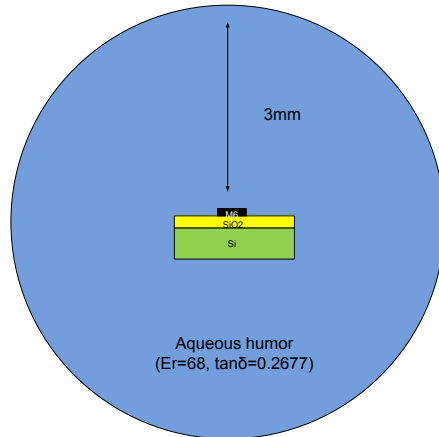


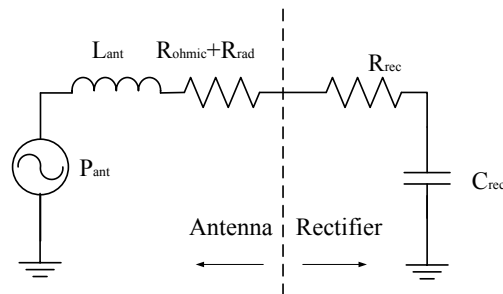
Fig. 63 Simplified 0.18-  $\mu\text{m}$  CMOS process stack-up

The third challenge is the high propagation loss inside the human eye which can be seen as additional dielectric loss. Shown in Fig. 57, the on-chip antenna is placed inside the 6  $\text{mm}^3$  Anterior chamber of human eye. Anterior chamber is fulfilled with aqueous humor ( $E_r = 68$ ) shown in Fig. 64. Aqueous humor has extremely high loss tangent ( $\tan\delta = 0.2677$ ) which is 200 times of  $\text{SiO}_2$ . This high loss tangent causes the antenna extremely difficult to implant on-chip.



**Fig. 64** An IC is placed inside the anterior chamber in huamn eye

The fourth challenge is the mismatch between RF rectifier and antenna. From chapter three, we know the input impedance of a RF rectifier is capacitive. Also, in Fig. 62, as can be seen, its impedance is quite low at high frequency. Thus, it's hard to match with low capacitive impedance with an on-chip antenna. Review the recent research rectenna design [3, 4, 17], the common way is to achieve a conjugate matching on the interface of antenna and rectifier shown in Fig. 65. For example if the impedance of rectifier is  $(7.5 - j67) \Omega$ , the impedance of antenna is designed to be  $(7.5 + j67) \Omega$  in order to cancel the capacitance.



**Fig. 65** Equivalent circuit of conjugate matching between antenna and RF rectifier

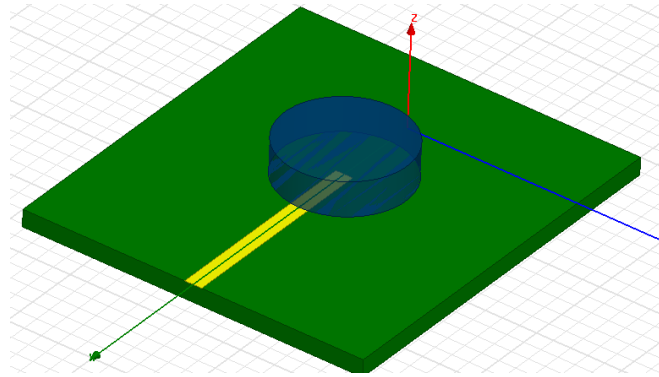
However, there are two issues in this matching technique. One is the low radiation impedance, such as  $8 \Omega$ , could degrades the antenna efficiency. The equation (17) could be derived as equation (18)<sup>[16]</sup>:

$$e_{cd} = \frac{R_{rad}}{R_{rad} + R_{ohmic}} \quad (18)$$

where  $R_{rad}$  is the radiation resistance and  $R_{ohmic}$  is the antenna loss resistance. For a certain  $R_{ohmic}$ , the efficiency could be achieved 100% when  $R_{rad} \gg R_{ohmic}$ . On the contrary, once  $R_{rad} < R_{ohmic}$ , the efficiency is less than 50% and even lower with small  $R_{rad}$ .

Another issue is the inductive impedance of the antenna which limits the design of antenna. [3][4][17] use small loop antenna to generate inductive impedance. However, the efficiency of a small loop antenna is quite low and also occupies large area. Increase the number of turns could shrink the size but degrade the efficiency even more. The antenna gain of [3][4][17] are less than -20 dB in free space which indicates the antenna efficiency are less than 5%, which are not qualified in our specs.

Based on the challenging mentioned above, one of the solutions is the dielectric resonator antenna (DRA) which has attracted much attention due to their attractive feature in terms of high radiation efficiency and smaller size depends on the dielectric constant of DR which is commonly made by ceramic. Fig. 66 shows a typical DRA with microstrip line fed. The top cylinder is the DR to create desired resonant frequency. [12][13] proposed on-chip DRA for 35 and 60 GHz to achieve 50% efficiency in CMOS technology. [13] also used metal 1 (M1) as a shielding to isolate the lossy Si-substrate.



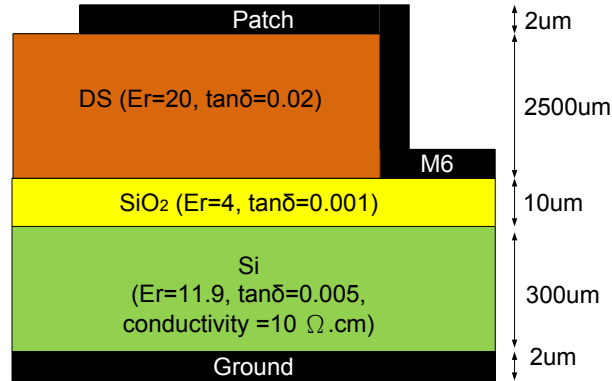
**Fig. 66 Microstrip line fed dielectric resonator antenna**

However, the disadvantage of DRA is the high tuning effort because of the complicated excitation mode in the dielectric cavity which is sensitive to the dimension of the DR. Also, the loss of DR has to be taken into account. Moreover, in our application, the on-chip antenna is surrounded by the aqueous humor which permittivity is higher than the ceramic DR. Therefore, DRA will not be able to work probably in our desired frequency.

#### **4.4.2 3D On-chip Antenna**

In order to overcome the limitation of the on-chip antenna placed in aqueous humor, in this section, this thesis proposes a new 3D structure solution to achieve high efficiency, small size, simple design, operating in low frequency range and match to 50-Ω standard network. The proposed 3D antenna is built on the polymer-ceramic dielectric and silicon substrate. According to [18], mixed with certain amount of polymer with ceramic material is able to create a high permittivity ( $\epsilon_r = 20$ ) and low loss tangent ( $\tan\delta < 0.02$ ) dielectric substrate. Also, based on the concept of DRA on silicon wafer, it's possible to integrate with the ploy-ceramic substrate upon the silicon chip. Instead of using dielectric material as a resonator, this work implants the poly-ceramic as a dielectric substrate for the patch antenna and isolates the radiated element away from the lossy silicon. Fig. 67 shows the stack-up of the proposed structure. Compared with Fig. 63 of the conventional CMOS technology, additional dielectric substrate (DS) with 2.5-mm

height is placed on the silicon dioxide. M6 bent into a shape extended along with the edge of DS to perform as a patch radiator. A ground layer placed on the bottom of the chip to create the electrical field path from the top to the bottom.

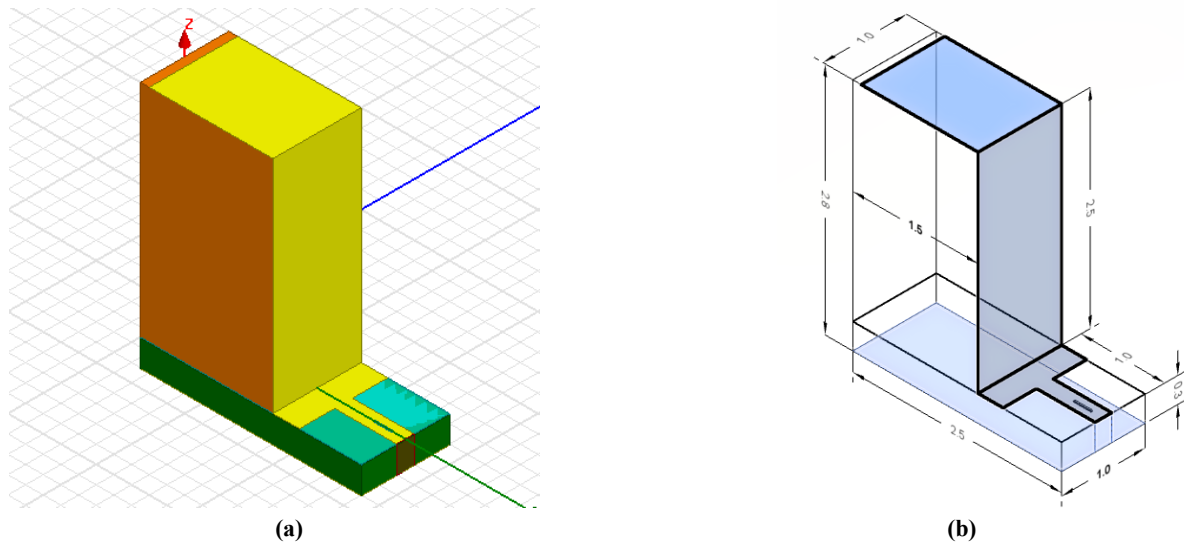


**Fig. 67 Cross view of the proposed 3D- structure for on-chip antenna**

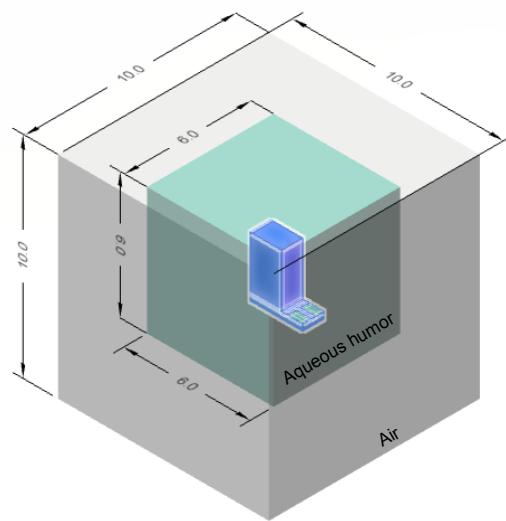
Couple of advantages in this structure allows high efficiency and small size on-chip antenna to be achieved. First of all, high-permittivity of DS is able to shrink the size of the patch. Second, 2.5- mm height of DS creates a dielectric shielding to isolate Si-substrate. Third, by 3D structure, M6 can be elongated to have enough electric length to operate at 5 GHz. The last, the antenna structure is simple and can be matched to 50- $\Omega$  by only adjusting the width of the antenna. Therefore, with 50- $\Omega$  system, it would be able to integrate with the proposed RF rectifier and other RF circuits.

Fig. 68 shows the proposed on-chip 3D patch antenna. The feeding is a 0.7-mm long 50- $\Omega$  Microstrip line (width: 0.2 mm) connected to the radiator with 1-mm width and 3.8-mm length (1.3-mm on the top + 2.5-mm on the side of DS). Between the radiator and the feeding line is a 0.3-mm long T-junction, and a 2.5 mm  $\times$  1 mm ground plane is placed under Si-substrate. The size of the antenna itself is only 1 mm  $\times$  1.5 mm  $\times$  2.8 mm which is extremely small and will be able to put inside the human eye.





**Fig. 68 3D-view of the proposed on-chip antenna. (a) HSS model (b) Detail dimensions (Unit: mm)**



**Fig. 69 Simulation model built up of the proposed on-chip antenna**

Due to the biomedical application for the Glaucoma, the on-chip antenna has to work in aqueous humor and, therefore, the ambience has to be taken into account in HFSS simulation. Fig. 69 shows the simulation model to present the human eye environment. The on-chip antenna locates inside a 6 mm × 6 mm × 6 mm aqueous humor ( $\epsilon_r = 68$ ,  $\tan\delta = 0.2677$ ). The boundary between near and far field of is given by equation (19) <sup>[16]</sup>:

$$R_f = \frac{2D^2}{\lambda_a} \quad (19)$$

where  $R_f$  is the boundary of near field,  $D$  is the longest dimension of the antenna, and  $\lambda_a$  is the propagation wavelength in certain material. In this design,  $\lambda_a$  is the wavelength in free space divided by the square root of the permittivity of aqueous humor, which is around 3 mm at 5.8 GHz. All the metal loss (copper) and dielectric losses are considered in HFSS simulation. The simulation results are presented in section 4.4.3.

#### 4.4.3 Simulation Results of the Proposed 3D On-chip Antenna

Fig. 70 shows the simulated return loss and input impedance. It can be seen that the resonant frequency occurs at 5.8 GHz with minimum  $S_{11}$  equal to -16 dB and the impedance is  $(64 - j10) \Omega$ , which indicates a good matching to 50- $\Omega$ . The bandwidth is 600 MHz (5.5 GHz-6.1 GHz) which covers the entire 5.8 GHz ISM band (5.75 GHz - 5.85 GHz).

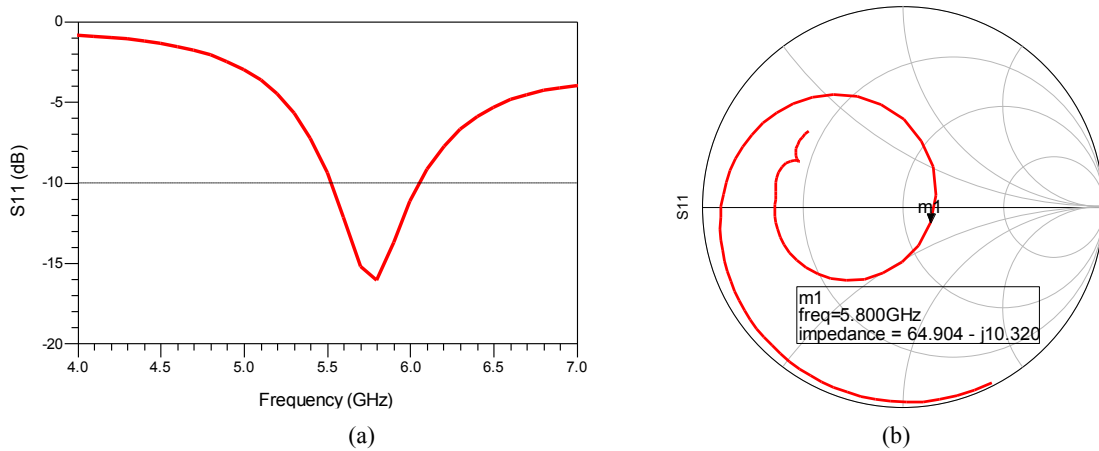
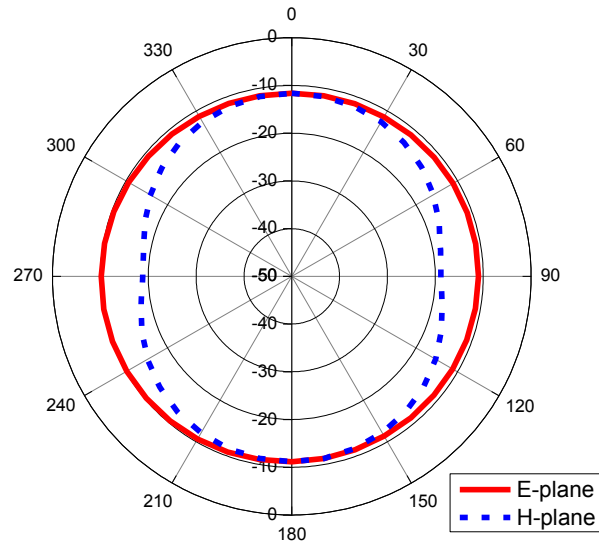
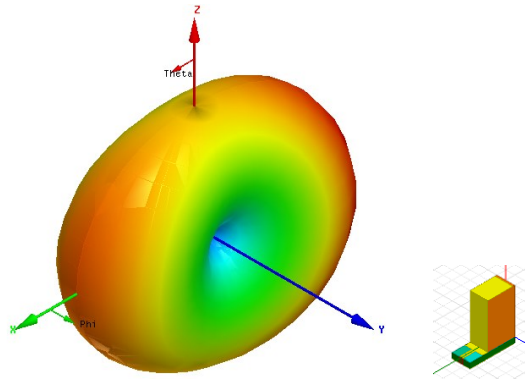


Fig. 70 Simulated (a) return loss and (b) input impedance of the proposed on-chip antenna

Fig. 71 shows the simulated radiation patterns and gain in E-plane and H-plane at 5.8GHz. The peak gain is -10 dBi both on E and H plane.



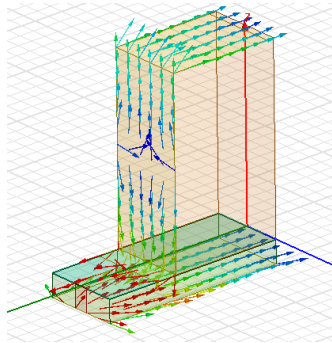
**Fig. 71 Simulated radiation pattern and gain in the E-plane and H-plane of the proposed on-chip antenna (Unit: dB)**



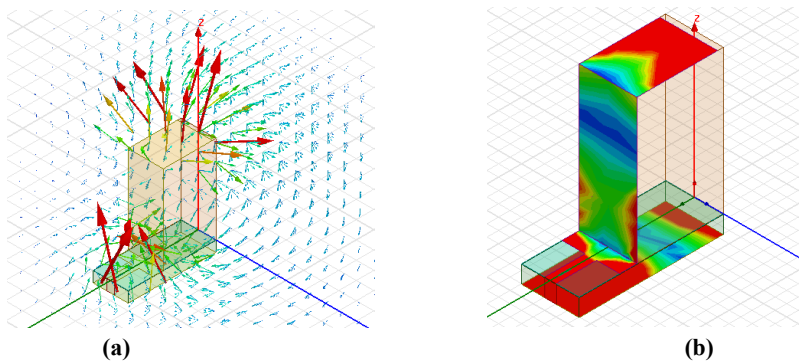
**Fig. 72 3D polar plot of the proposed on-chip antenna**

Fig. 72 shows the 3D-polar plot of the radiation pattern. As can be seen, the proposed antenna is close to an omnidirectional antenna which has the main lobe on the XZ plane. Fig. 73 and Fig. 74 show the current and E-field distribution on the metal of the on-chip antenna. As can be seen in the Fig. 74(a), the proposed on-chip antenna is a patch antenna because the top patch radiator contributes the main electrical field. The fringing field causes the antenna to radiate and thus the magnitude of E-field is stronger on the edge of the top patch and ground plane. However, due the small ground plane, this antenna resonates in a  $\frac{3}{4} \lambda$  dipole mode. As can be

noticed in Fig. 73, there is a zero current spot on the side wall and away from the spot, the current reaches zero again on the top edge to form a quarter wavelengths. The overall current path is around 7.3 mm which is roughly  $\frac{3}{4} \lambda$ .  $\lambda$  is roughly 10 mm due to part of the E-fields are located in aqueous humor. Therefore, in a summary, the top patch contribute the radiation and the  $\frac{3}{4}$  wavelength generate the resonated frequency at 5.8GHz.



**Fig. 73 Surface current on the conductor of the proposed on-chip antenna**



**Fig. 74 (a) E-field distribution around the on-chip antenna (b) E field magnitude on the radiator and ground**

Fig. 75 shows the radiation efficiency and peak gain of the proposed on-chip antenna. At the ISM band from 5.725 to 5.875 GHz, the efficiency is 10% the gain are greater than -10 dBi, which mean the proposed antenna could achieve the 150-MHz bandwidth criteria.

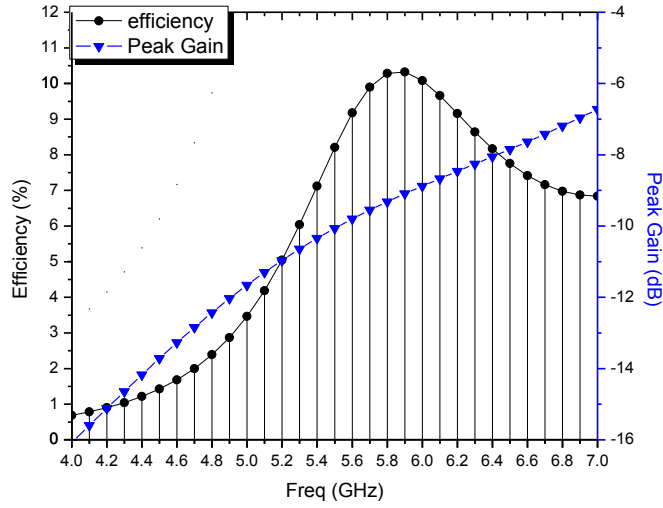


Fig. 75 Efficiency and peak gain versus frequency of proposed on-chip antenna

Table 6 shows the comparison with the similar on-chip antenna design. As can be seen, in this work, -10-dBi peak gain and 10% efficiency are the highest one compared with similar frequency range.

Table 6 Performance summary and comparison with papers

Ref	This work	[4]	[3]	[19]	[20]	[21]	[12]
Frequency (GHz)	5.8	5.2	4	9	5.8	60.5	60
Peak Gain (dBi)	-10	-14.5	-25	-10	-29.5	-3.32	0
Efficiency	10% (30% @ near field)	Below 10%	Below 10%	9%	Below 10%	15.87%	NA
Size (mm <sup>2</sup> )	1.5 × 1 (H= 2.8)	2.9 × 1.1	3 × 3	0.6 × 0.6	3 × 1.5	1.2 × 1.6	2 × 1.5 (H= 1.7)
Antenna type	Patch	Monopole	Loop	Slot	Scavenging	Patch	Slot dipole
Technique	3D	Loop load	Single loop	Meander	Inductive stubs	Ground shielding	DRA
Application	Aqueous humor	Aqueous humor	Free space	Free space	Free space	Free space	Free Space
Year	2013	2012	2010	2009	2010	2010	2012

## 4.5 Rectenna Integration

Fig. 76 is the rectenna system diagram. The Native NMOS rectifier is the proposed rectifier from section 4.3 and the on-chip antenna is from section 4.4. Once we integrated the two into a rectenna, the matching could be slightly tuned by the on-chip spiral inductor. Fig. 77 shows the placement of an example wireless system on the proposed on-chip antenna. The rectifier could be located inside the wireless system chip which occupies roughly  $1 \text{ mm} \times 1 \text{ mm}$  on a wafer. Thus, the overall wireless system might be  $2.5 \times 1 \times 2.8 \text{ mm}^3$ .

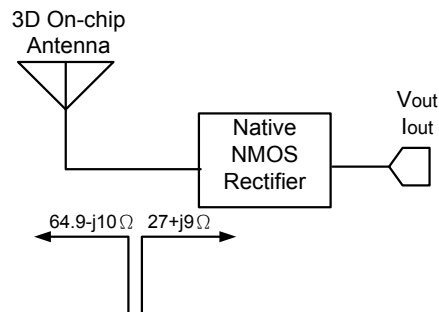


Fig. 76 Rectenna system block diagram

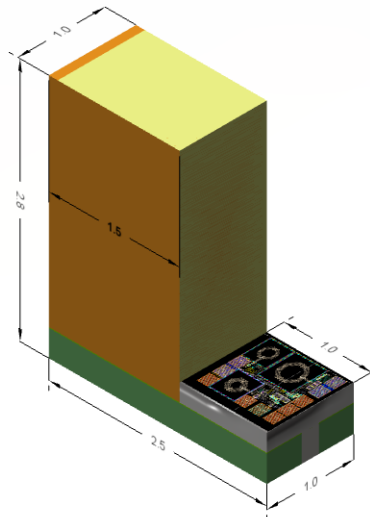
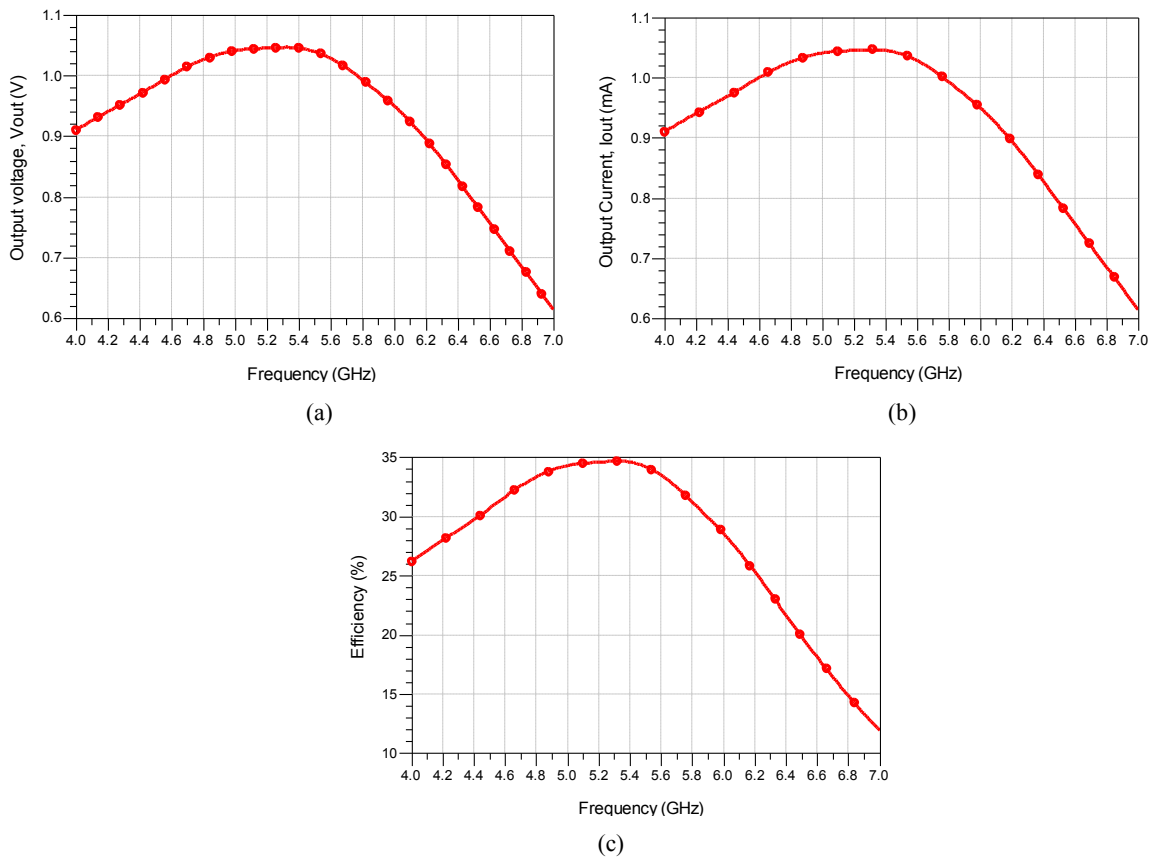


Fig. 77 On-chip antenna integrated with an example RF wireless system

The performances of the rectenna system are shown in Fig. 78. At the frequency range from 4.6 GHz to 5.8 GHz with 5-dBm input, the rectenna could achieve 1-V and 1-mA output with at least 30% RF to DC efficiency, which is able to generate enough power to run the modern low power wireless system. Due to the input power to the rectifier is 5 dBm (3.2 mW), with 30% efficiency on-chip antenna, we can calculate the input power into the entire retenna is roughly 10.3 dBm (10.7 mW).



**Fig. 78** (a) Output voltage (b) output current (c) efficiency of the proposed rectenna system at 5 dBm input the RF rectifier.

## 4.6 Summary

An on-chip 3D rectenna operating at 5.8 GHz which can generate 1-V and 1-mA output at 10.3-dBm input is proposed in this chapter. The rectenna system is combined with a single-stage diode-connected Native NMOS RF rectifier and a 3D on-chip antenna. The size of the entire

rectenna is  $2.5 \times 1 \times 2.8 \text{ mm}^3$  which is small enough to place in human eye. The performance compared with different papers also be presented and indicates that this work has a better efficiency over others. In the chapter five, a study for integrating the rectenna system with the wireless transmitter will be studied and evaluated.



# CHAPTER FIVE: IMPLANTABLE WIRELESS SYSTEM FOR BIOMEDICAL APPLICATION

## 5.1 Introduction

From the link budget analysis in chapter four, the rectenna system provides 1-V and 1-mA to power up the implanted transmitter including PA and VCO, and also drives other sensing circuits in a chipset. The system block diagram is shown in Fig. 78. The implanted rectenna could be triggered by an external RF source from 5-cm distance, and then generate voltage and current to supply the whole implanted circuits. Therefore, low power consumption design of the implanted transmitter is required.

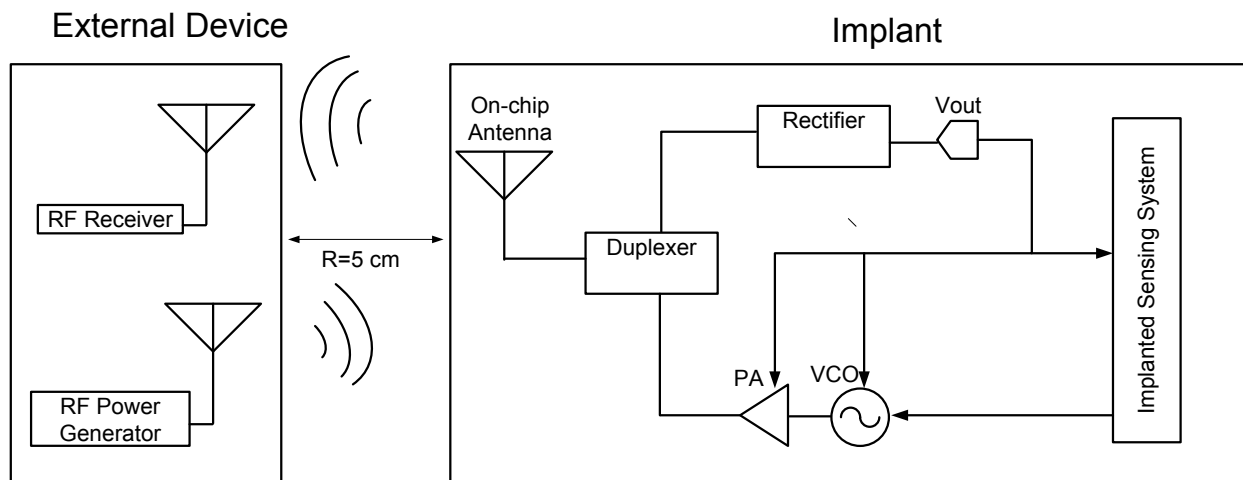
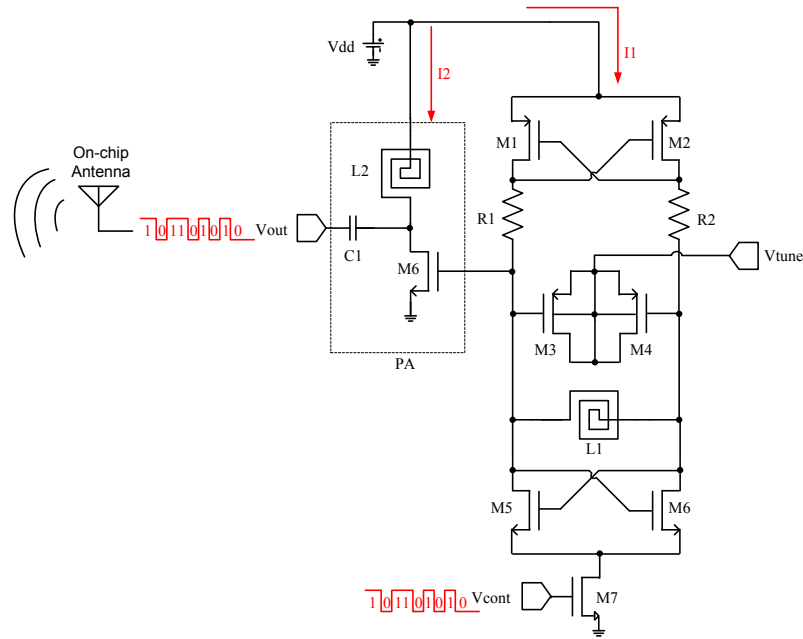


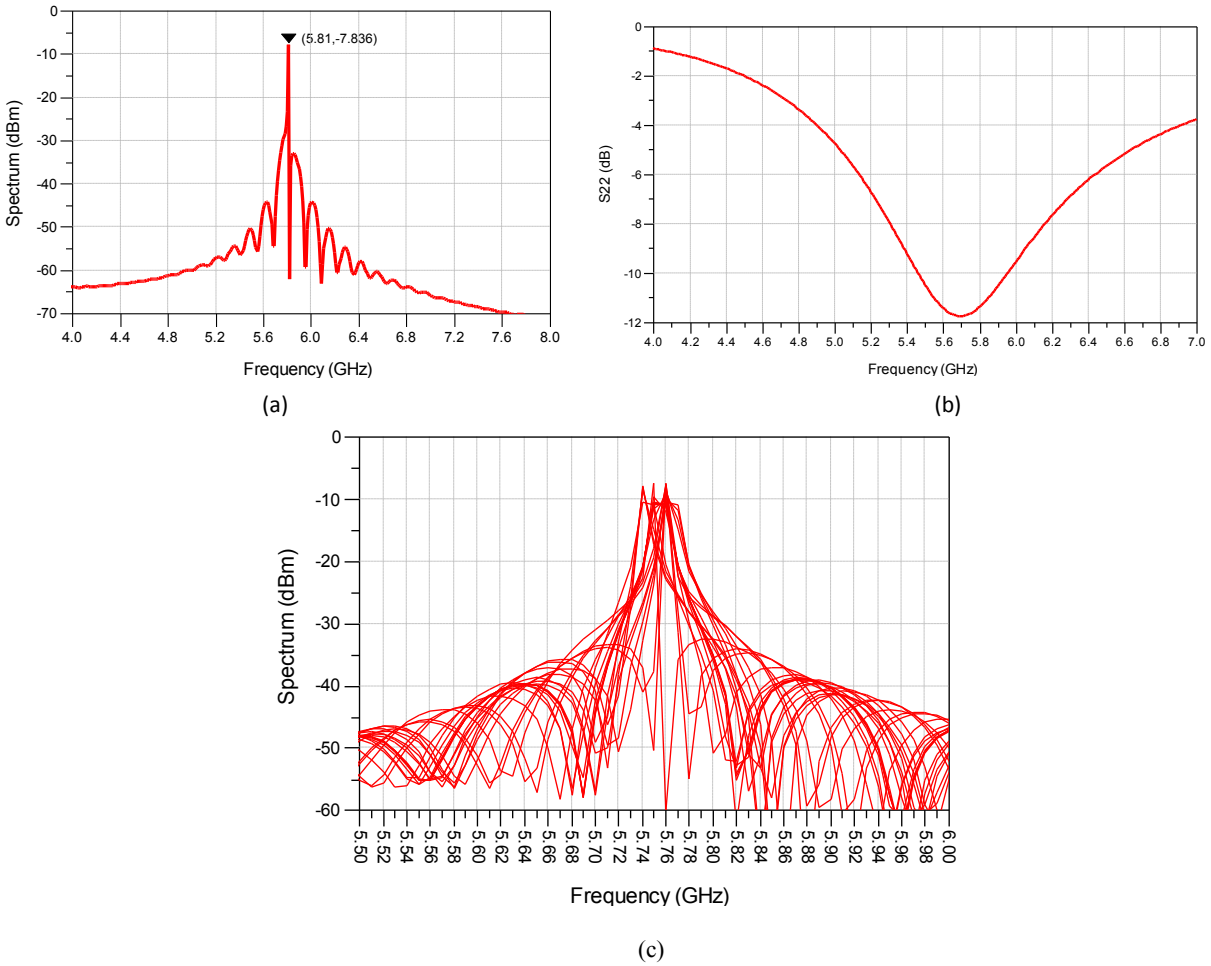
Fig. 79 Simplified block diagram of the entire biomedical wireless system

## 5.2 Implanted RF Transmitter



**Fig. 80** Implanted transmitter include a VCO and a PA

The implanted RF transmitter is combined with a low power VCO to resonate at 5.8 GHz and a PA to burst the resonated signal. Both VCO and PA are supplied by 1.2-V  $V_{dd}$ . Fig. 80 shows the circuit components of the transmitter. All the transistors and lump components are using TSMC 0.18- $\mu\text{m}$  model.  $M_1$  and  $M_2$  are PMOS to provide a negative resistance.  $M_3$  and  $M_4$  are PMOS which body, drain and source are connected to form a controllable MOS varactor. The capacitance is tuned by the voltage  $V_{\text{tune}}$  and resonates with the inductor  $L_1$ .  $M_5$ ,  $M_6$  and  $M_7$  are the current source to control the current through the VCO.  $R_1$  and  $R_2$  are two 10- $\Omega$  balance resistors to reduce the power consumption <sup>[22]</sup>. The PA, also can be seen as a buffer, is a single-stage NMOS. The current  $I_1$  through VCO is 270  $\mu\text{A}$  and  $I_2$  is 300  $\mu\text{A}$  for the PA. The overall current is only 570  $\mu\text{A}$  which is able to generate -7.8 dBm to input on-chip antenna shown in Fig. 81(a). Fig. 81(b) shows the output matching is less than -10 dB at 5.8 GHz and Fig. 81(c) shows the tuning range of the VCO is around 40MHz by adjusting the tuning voltage form 2V to -2V.



**Fig. 81 (a) The output spectrum (b) return loss (c) voltage tuning range versus frequency of the designed RF transmitter**

In the Fig. 80, the control voltage ( $V_{con}$ ) is a digital signal from the sensing circuit to switch VCO on and off in order to send the data by OOK modulation to the external device. When  $V_{con}$  is high,  $M_7$  is on and VCO start to transmit the data through  $V_{out}$  to the antenna, and in contrary, VCO is turned off while  $V_{con}$  is low. After the demodulation by external receiver, the patient will be able to read the data such as eye or heart pressure. As can be seen in Fig. 82, The data of  $V_{out}$  is the same as the signal generated by  $V_{con}$ . The amplitude of  $V_{out}$  is 0.2 V, and therefore, the external device has to have high sensitivity to detect the weak signal.

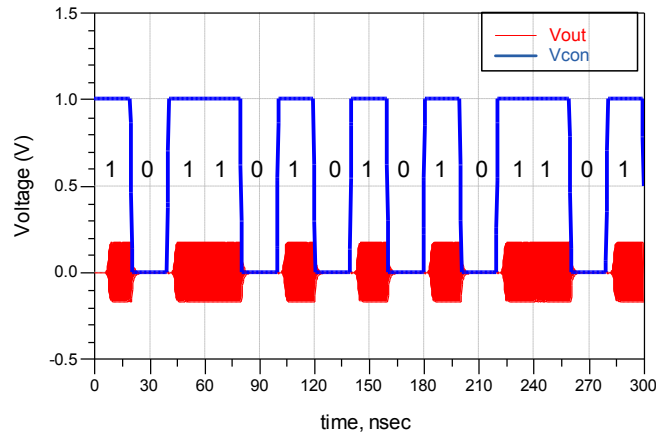


Fig. 82 OOK modulation by switching  $M_7$  on and off through the control signal  $V_{con}$

### 5.3 External Antenna

For the external antenna, this thesis use the simple patch antenna operated at 5.8 GHz shown in Fig. 83. The substrate is Roger 4003 ( $\epsilon_r = 3.55$ ,  $H = 1.27$  mm,  $\tan\delta = 0.0027$ ) and the patch size is  $13 \times 12$  mm<sup>2</sup> which is able to put inside a portable reader. The 3D-polar plot of the patch is shown in Fig. 84 and other parameters are listed is in Table 7. The peak gain is 6 dBi toward +z-direction. Therefore, +z-direction is toward the human eye with 5-cm distance and the implanted on-chip antenna is inside the anterior chamber of human eye shown in Fig. 85.

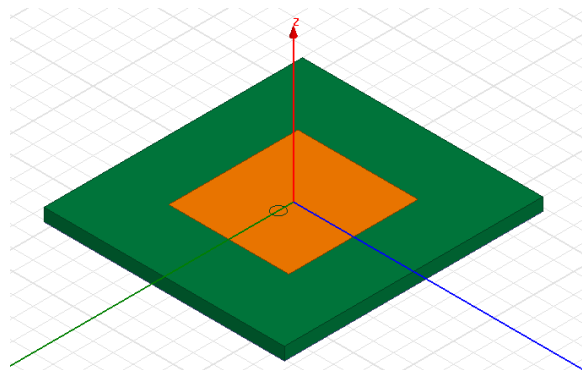


Fig. 83 5.8-GHz patch antenna for the external device

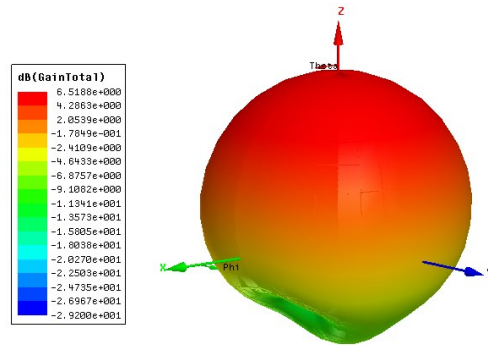


Fig. 84 3D-polar plot (radiation pattern) of the 5.8-GHz patch antenna

Table 7 Parameters of the external patch antenna

Parameter	Value at 5.8GHz
S11 (dB)	-18.6
Peak Gain (dBi)	6.5
Directivity (dB)	6.7
Efficiency	95%
Ground Size (mm <sup>2</sup> )	26 × 24

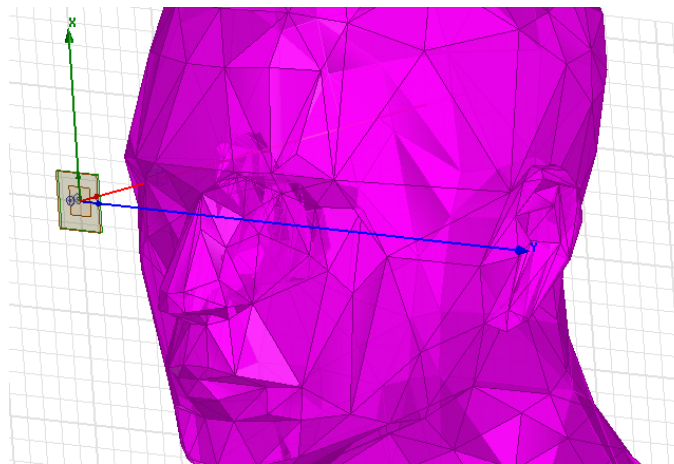


Fig. 85 External antenna is placed 5-cm away from the human eye to communicate with the implanted on-chip antenna

Fig. 86 shows a simplified model placement for the simulation. The distance is 50 mm and the on-chip antenna is placed inside a 6 mm<sup>2</sup> aqueous humor. The excitation of port 1 is on external patch antenna and port 2 is on the implanted on-chip antenna. Fig. 87 shows the loss from port 1 to port 2 is 25.7 dB at 5.8 GHz. Afterward, once we have the S- parameter between external and

implanted antenna, we can import the .S2P file into the wireless system circuits in ADS to evaluate the entire system performance.

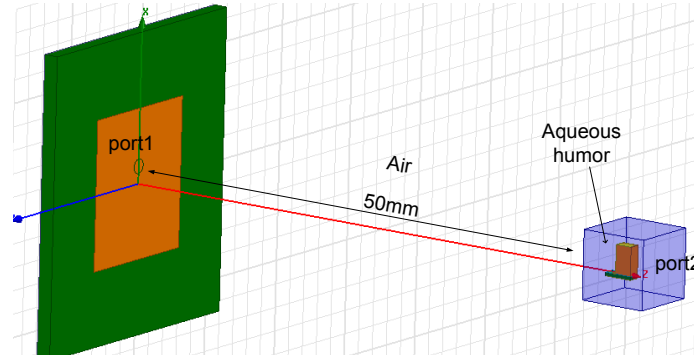


Fig. 86 Simplified model placement for simulation of the loss between external and implanted on-chip antenna

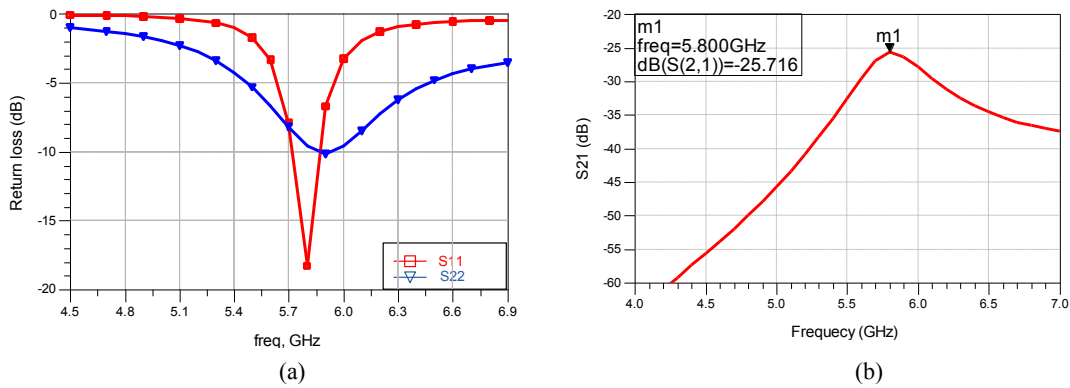


Fig. 87 (a) Return loss and (b) propagation loss from the external patch antenna to the implanted on-chip antenna

## 5.4 Biomedical Wireless System

Fig. 88 shows the entire wireless system circuit. The signal generator provides 36 dBm to the system and the loss between two antennas is 26 dB. Therefore, the power input the rectifier is roughly 10 dBm, and then it can generate a voltage ( $V_{rec}$ ) and a current ( $I_{rec}$ ) to supply the VCO and PA. Fig.11 show the  $V_{rec}$  is around 1.1 V and  $I_{rec}$  is 3 mA in average which has ability not only supply the transmitter but the other implanted circuits.

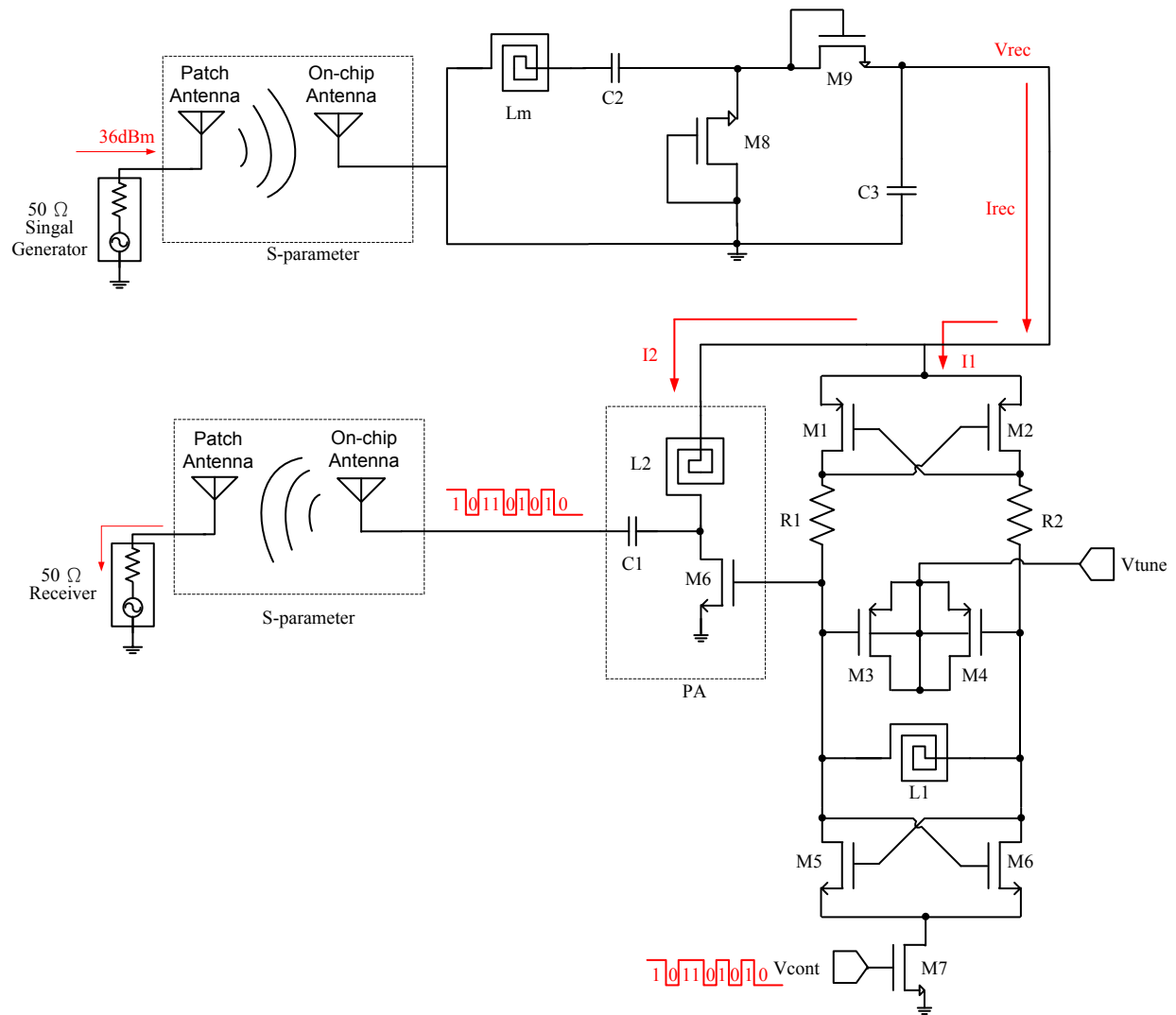


Fig. 88 Schematic of the entire biomedical system

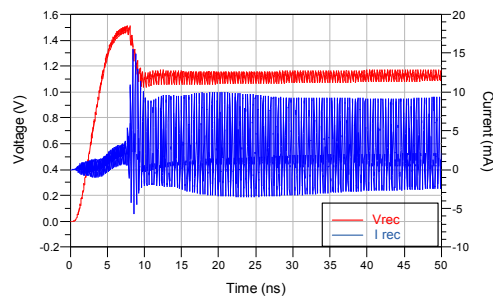
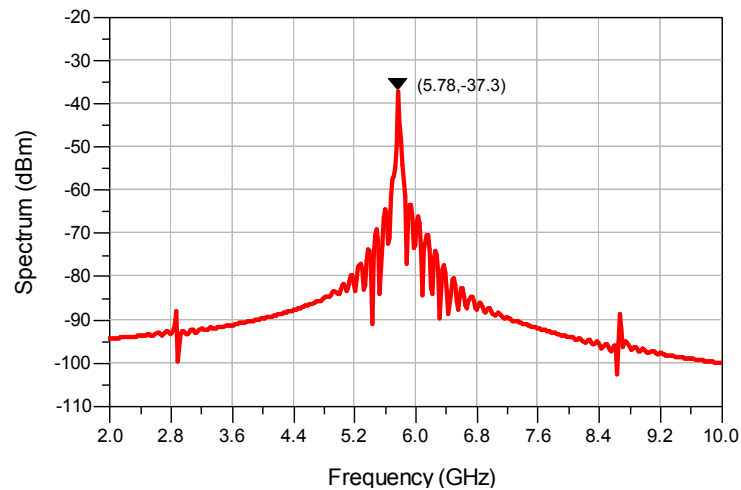


Fig. 89 Voltage ( $V_{rec}$ ) and current ( $I_{rec}$ ) of the implanted RF rectifier

Fig. 90 shows the frequency spectrum at the external receiver at 36 dBm from the external signal generator. At 5.8 GHz, the receiving power is -37.3 dBm which is high enough for the demodulation and also well matching to the link budget (-36 dBm) at chapter four.



**Fig. 90** Frequency spectrum at external receiver

## 5.5 Summary

This chapter presents a wireless on-chip integrated circuit including antenna, rectifier, VCO and PA for the biomedical application. The overall performance is well match to the link budget in chapter four. All the circuit simulation is based on TSMC model and the application environment is also being considered. Therefore, this system design will be able to fabricate in the future work.



## **CHAPTER SIX: IMPLANTABLE WIRELESS SYSTEM WITH ON-CHIP ANTENNA FOR CARDIOVASCULAR PRESSURE MONITOR**

### **6.1 Introduction**

The on-chip antenna in chapter four locates inside the human eyes for Glaucoma or eye pressure monitor. Beside this application, the entire wireless system also works for monitoring the cardiovascular pressure. Based on the reference <sup>[1]</sup>, the designed implantable cardiac monitor system is able to be placed in human circulatory and the location of pulmonary artery has been studied and experimented. The antenna is applied by a metal stent both to radiate signal and support the structure with the overall dimension of  $30 \times 10 \text{ mm}^2$ . However, two disadvantages of this structure have to be considered. First, the stent is not 50- $\Omega$  which means lots of power would be reflected from antenna to the rectifier and also from the transmitter to the antenna. Second, the size of  $300\text{-mm}^2$  is too large to put in the blood vessel and it might block the blood flow and cause serious health problem for human. In order to solve the above issues, the compact on-chip antenna proposed in chapter four can be modified to fit in any human circulatory system. Two cases will be studied in this thesis. The first case we place cardiac monitor to read the global blood pressure, for example, inside the carotid artery shown in Fig. 91(a) which is a blood vessel inside human neck and connected to the pulmonary artery. 10-mm thickness of the muscle is between skin and carotid artery. Therefore the propagation loss has to be taken into simulation. However, the diameter of the carotid artery is only 4 mm which means the system chip cannot large than half of the diameter otherwise it would affect the blood flow. The simulation result and model are presented in section 6.2 and 6.3.

In second case, we put the monitor system directly inside the pulmonary artery shown in Fig. 91(b), similar to [1], and read the localized cardiovascular-pressure information which is more accurate compared to other circulatory in human body. The result will be presented in section 6.4.

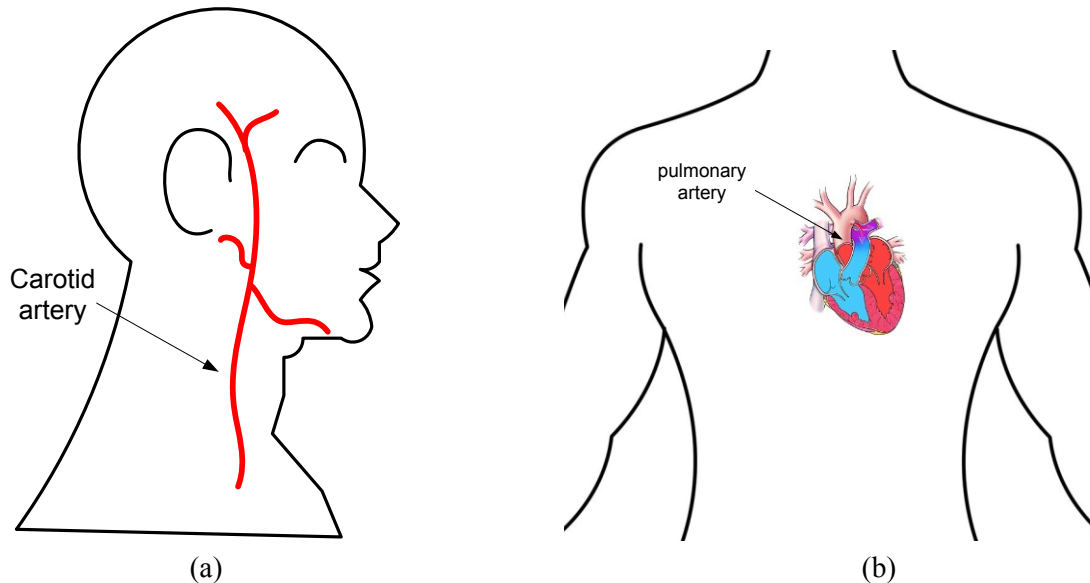


Fig. 91 (a) Carotid artery in the human neck (b)Pulmonary artery near heart

## 6.2 On-chip Antenna for Global Blood Pressure Monitoring

Fig. 92 is the modified 3D on-chip antenna for placing inside the carotid artery to monitor global blood pressure. The dimension of the antenna is  $1 \times 0.6 \times 4.8 \text{ mm}^3$  with a  $1 \times 0.6 \text{ mm}^2$  on-chip circuits. This tube shape of the on-chip antenna is designed to fit the blood vessel. Fig. 93 shows the on-chip antenna placed inside the carotid artery. It can be seen the antenna only occupies one third of the volume of the carotid artery.

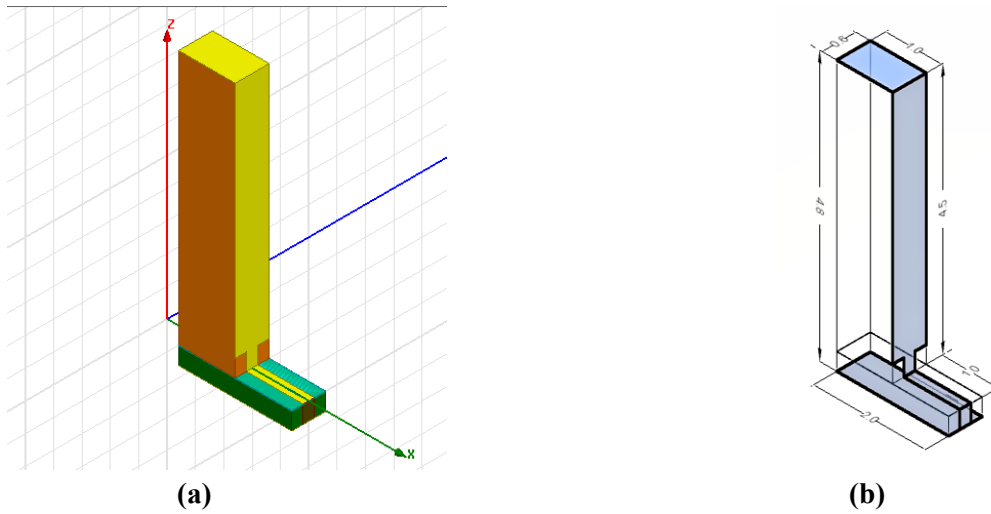


Fig. 92 3D-view of the proposed on-chip antenna for blood pressure. (a) HSS model (b) Detail dimensions (Unit: mm)

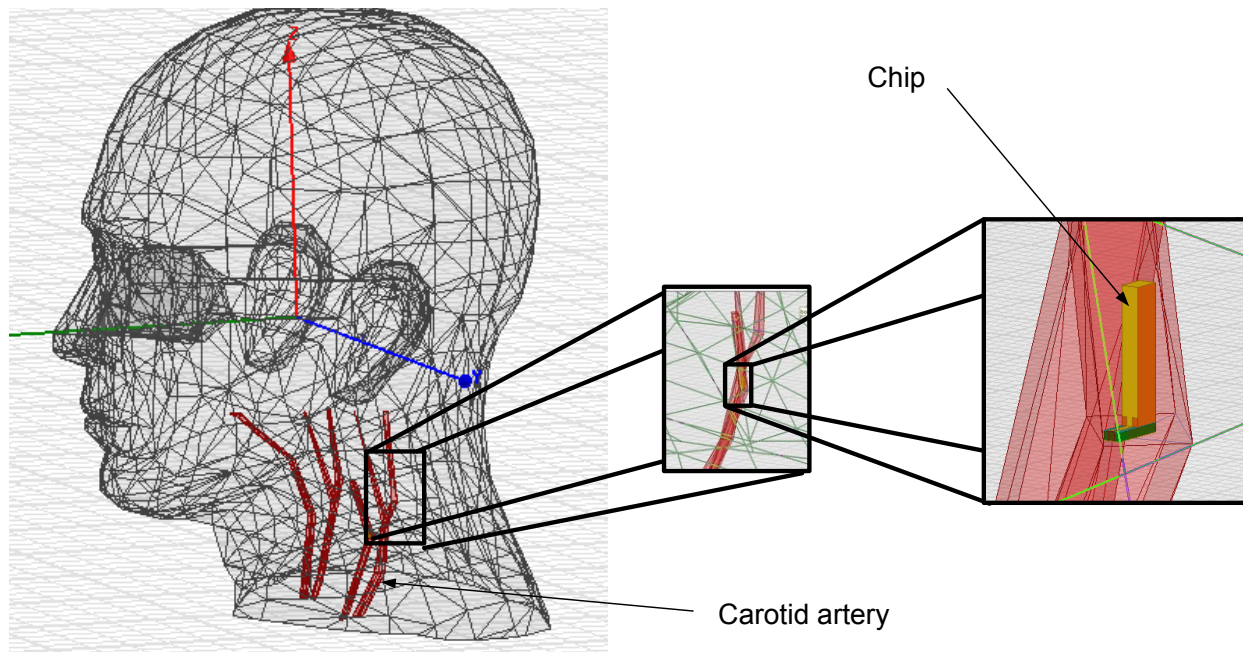
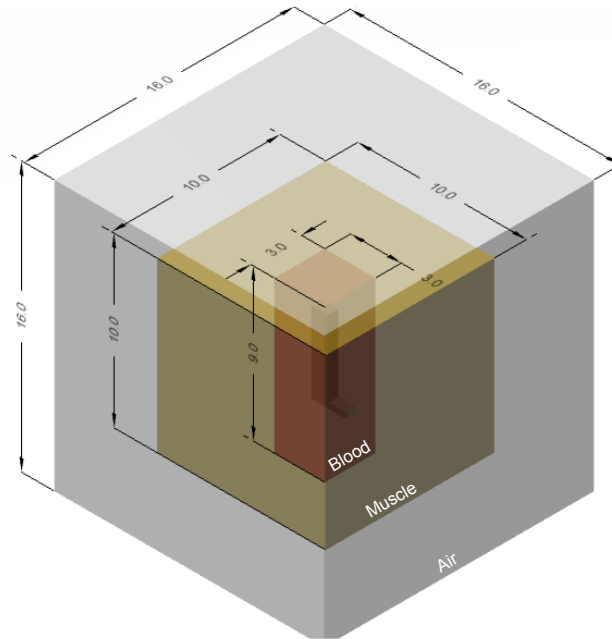


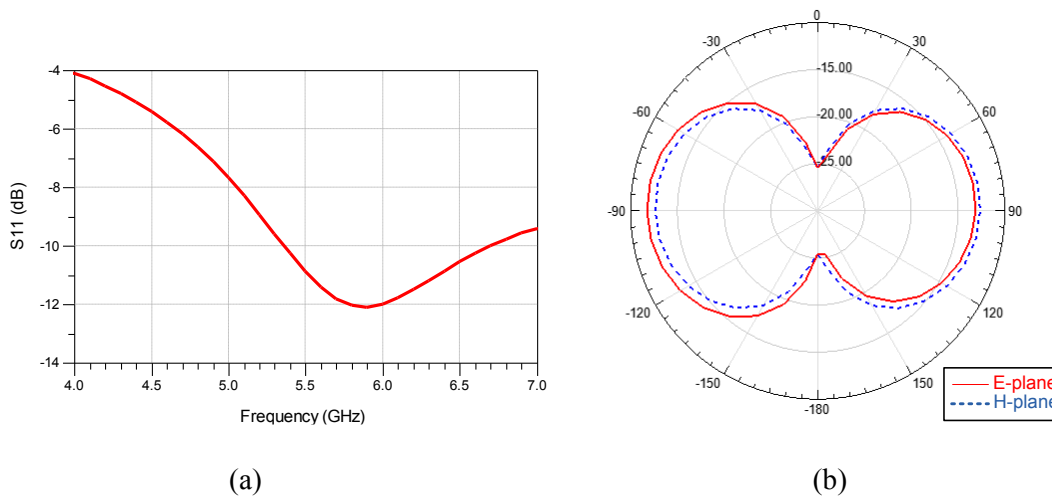
Fig. 93 The on-chip antenna placed inside the carotid artery

The simulation model setup is shown in Fig. 94. The on-chip antenna is placed in a  $3 \times 3 \times 9$  mm<sup>3</sup> blood ( $\tan\delta = 0.384$ ,  $\epsilon_r = 52.54$ ,  $\rho = 6.5057$  S/m) box and the blood box is inside a  $10 \times 10 \times 10$  mm<sup>3</sup> muscle ( $\tan\delta = 0.32$ ,  $\epsilon_r = 48.4$ ,  $\rho = 4.962$  S/m) box. The air box is  $16 \times 16 \times 16$  mm<sup>3</sup>. Fig. 95 shows the simulation result of the return loss and radiation pattern, and other detail results are

listed in the table 8. As can be seen, due to the high loss of blood and human muscle, the efficiency is 10% and the peak gain is -11.7 dB. However, it still works for a short communication distance.



**Fig. 94 Simulation model for the on-chip antenna placed inside a blood vessel and Muscle box**



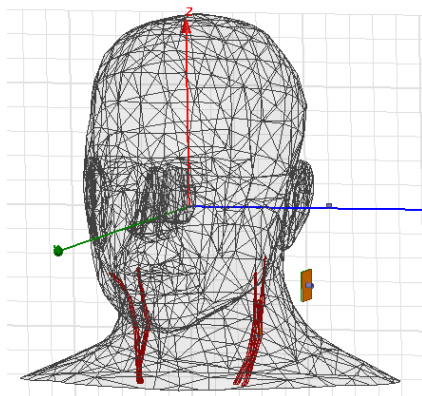
**Fig. 95 (a) Return loss and (b) radiation pattern of the proposed on-chip antenna for blood pressure monitor**

**Table 8 Parameters of the designed on-chip antenna for blood pressure monitor**

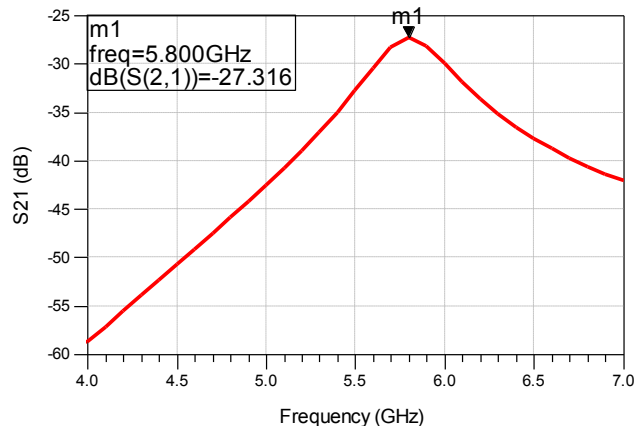
Parameter	Value at 5.8GHz
S11 (dB)	-12
Peak Gain (dBi)	-11.7
Efficiency	10%

### 6.3 Wireless system Global Blood Pressure Monitoring

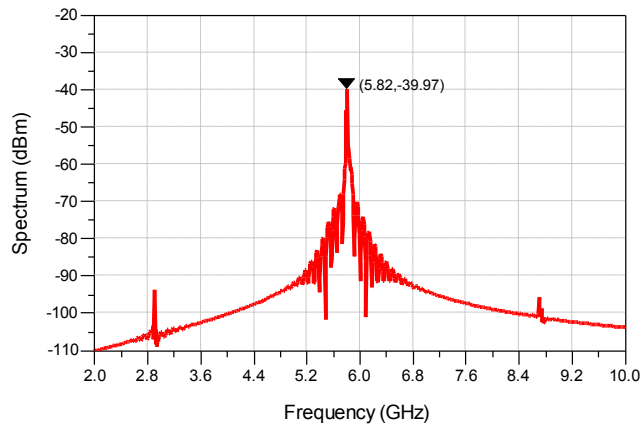
Similar to the Fig. 85 in chapter five, the external patch antenna is placed 5 cm away from the implanted chip to power up the system and receiving the data. A simulation model setup is the same as Fig. 86. The propagation loss between the two antennas is 27 dB. Once we have this S-parameter, we can import .S2P files into the rectenna and transmitter system shown in Fig. 88 in chapter five to evaluate the overall performance. Fig. 98 shows the receiving power at the external device. The receiving power level is -40 dBm which is roughly 2.5 dB less than the eye pressure monitor system because of lower antenna gain. -40 dBm is higher enough for the receiver to demodulate. Therefore the wireless system for cardiovascular pressure could still work properly.



**Fig. 96 External antenna is placed 5-cm away from the human neck to communicate with the implanted on-chip antenna in carotid artery**



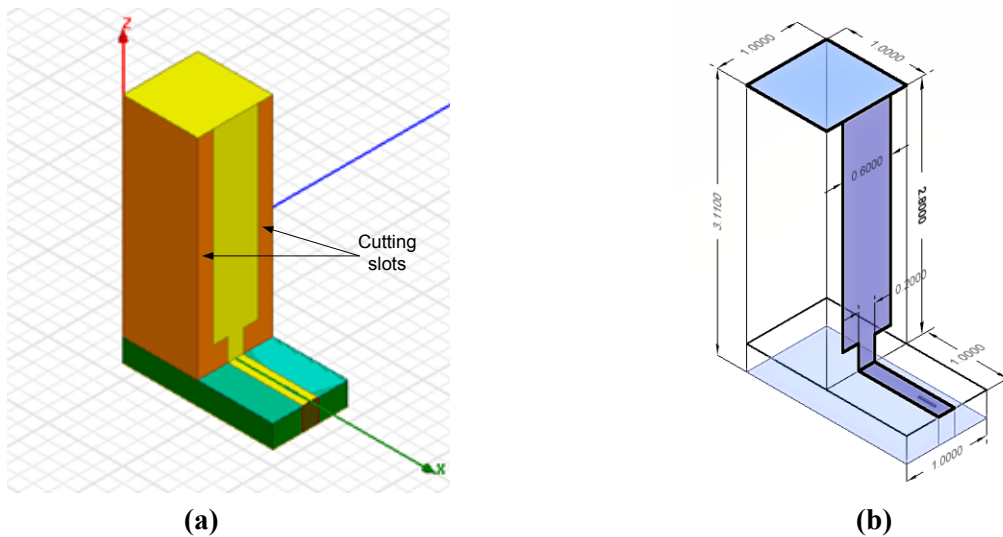
**Fig. 97 Propagation loss from the external patch antenna to the implanted on-chip antenna**



**Fig. 98 Output frequency spectrum at external receiver of the cardiac monitor system**

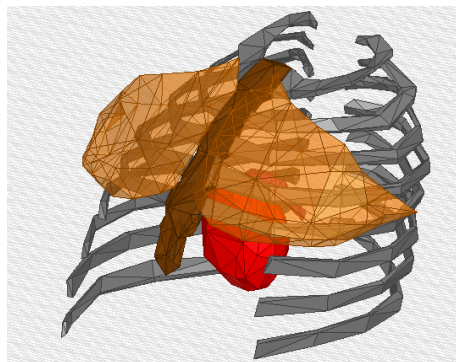
## **6.4 On-chip Antenna for Local Cardiovascular Pressure Monitoring**

Similar to 6.2, for more accurate local blood pressure information, we put the monitoring system directly inside the pulmonary artery which is right next to the heart. The volume of pulmonary artery is larger than the carotid artery. Therefore we have more room to place the designed on-chip system.



**Fig. 99** 3D-view of the proposed on-chip antenna for placing in pulmonary artery. (a) HSS model (b) Detail dimensions (Unit: mm)

Fig. 99 shows the modified 3D on-chip antenna for placing in pulmonary artery to monitor local blood pressure. The dimension of the antenna is  $1 \times 1 \times 3.1$  mm<sup>3</sup> with a  $1 \times 0.6$  mm<sup>2</sup> on-chip circuits. The cutting slots on the side wall of the antenna are used for impedance match to 50-Ω.



**Fig. 100** Human chest model

Fig. 100 shows the model of human chest structure. The pulmonary artery locates in front of heart. In front of pulmonary artery, there are also sternum, ribs and chest muscle around. Therefore the simulation model is quite complicated compared to section 6.2. The model setup is

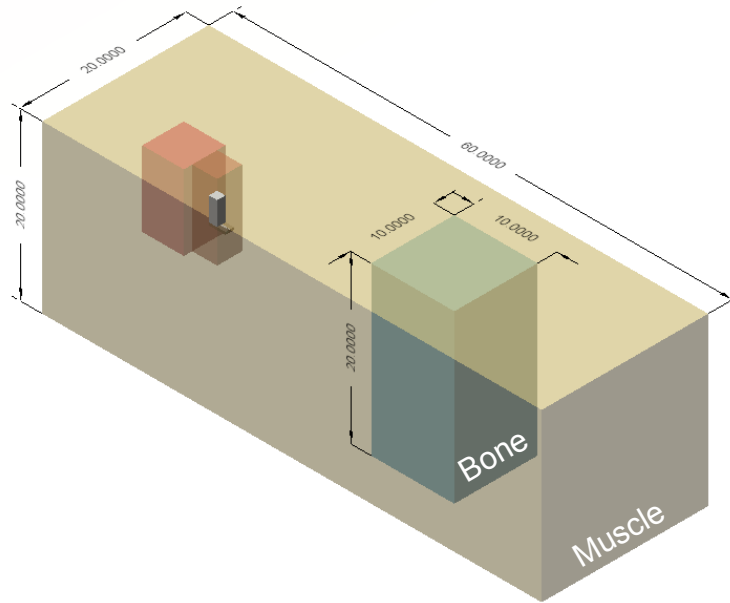
shown in Fig. 101. The on-chip antenna is placed in a  $3 \times 3 \times 9 \text{ mm}^3$  blood box and the blood box is inside a  $20 \times 60 \times 20 \text{ mm}^3$  muscle box. All the material properties of human organs are shown in Table 9.

**Table 9 Material properties of human organs**

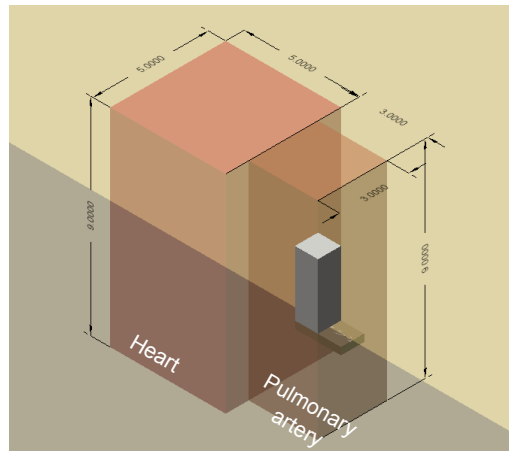
Frequency : 5.8 GHz			
Human organ	Relative permittivity	Loss tangent	Conductivity (S/m)
Muscle	48.49	0.317	4.96
Bone	9.67	0.369	1.154
Heart	48.95	0.371	5.86
blood	52.53	0.384	6.57
Aqueous humor	68	0.2677	6.67

Fig. 102 shows the simulation result of the return loss and radiation pattern, and other detail results are listed in the table 10. As can be seen, the efficiency is 10% and the peak gain is -10 dB, which meets our spec.



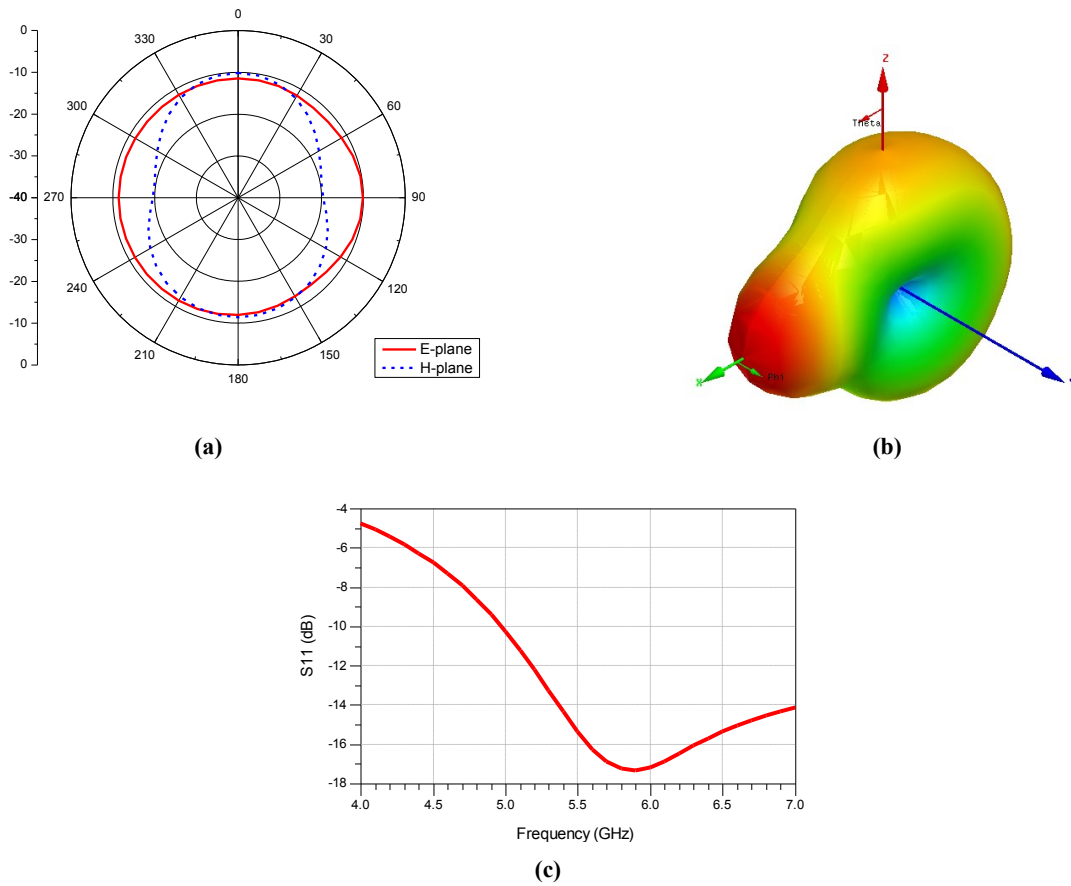


(a)



(b)

**Fig. 101 (a) Simulation model for the on-chip antenna placed in blood with muscle and bone around (b) Close view of simulated pulmonary which is right next to the heart**



**Fig. 102 (a) Radiation pattern (b) 3-D polar plot (c) return loss of the proposed on-chip antenna for local blood pressure monitor**

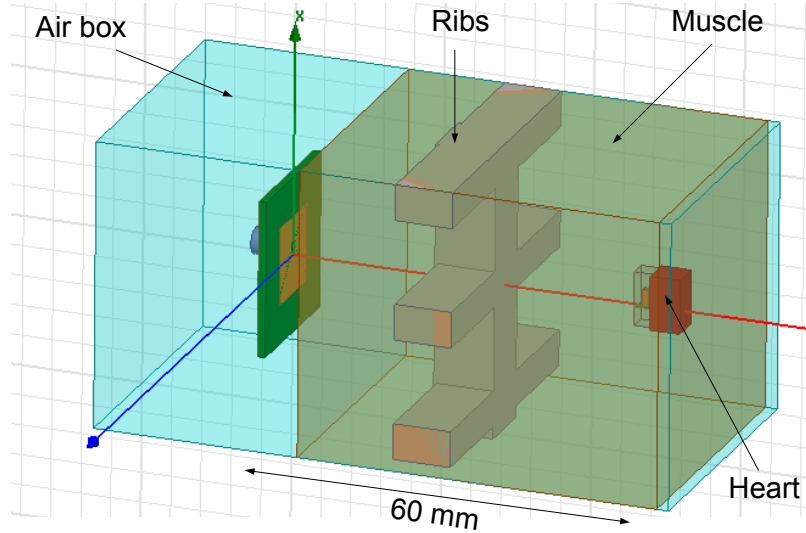
**Table 10 Parameters of the designed on-chip antenna in pulmonary artery**

Parameter	Value at 5.8GHz
S11 (dB)	-17
Peak Gain (dBi)	-10.1
Efficiency	9.3%

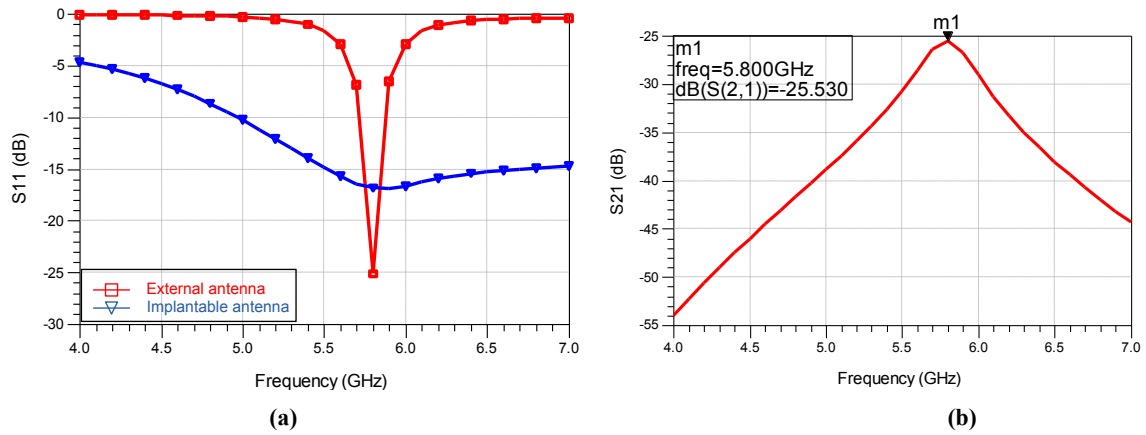
## 6.5 Wireless system for Local Cardiovascular Pressure Monitoring

The wireless system model for the local blood pressure monitoring is shown in Fig. 103. There are ribs and muscle between the external antenna and implanted antenna. The distance between the two antennas is 6-cm. For a person with thicker chest muscle might enlarge the distance. The simulation results of return loss and insertion loss are shown in Fig. 104. The

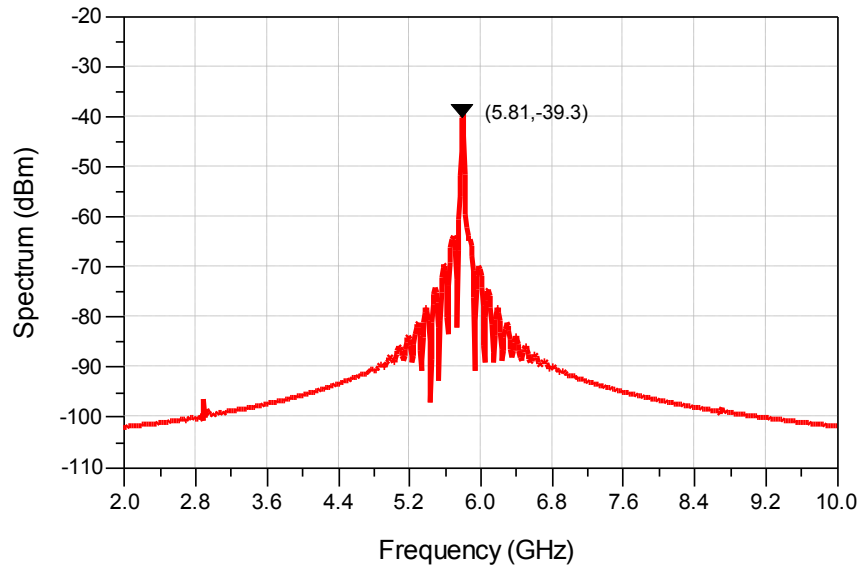
overall system performance is shown in Fig.105. The receiving power from the external device is -39.3 dBm which is still higher than -40 dBm and therefore it demonstrated this receiving signal is able to be demodulated by the high sensitivity communication technology.



**Fig. 103** External antenna is placed 6-cm away from the heart to communicate with the implanted on-chip antenna in pulmonary artery



**Fig. 104** Simulation result of (a) Return loss of external and implanted antenna (b) insertion loss from the external to the internal antenna to the implanted on-chip antenna



**Fig. 105** Output power at external receiver of the cardiac monitor system

## 6.6 Conclusion

Review chapter five and chapter six, the proposed biomedical wireless system can either work on eye or heart pressure monitoring application without any battery supply. Based on different application environment, the shape of the compact on-chip antenna may need to be modified in order to fit in the allowable space. Both the receiving power level at the external device is higher than -40 dBm at 36-dBm input from the external signal generator at 5.8 GHz. For the high sensitivity receiver such as Zigbee with sensitivity lower than -60 dBm, data with -40-dBm power level is able to be processed.

## **CHAPTER SEVEN: CONCLUSION**

### **7.1 Accomplishments**

In this thesis, a fully implantable wireless system analysis and design including on-chip rectenna and low power RF transmitter for the biomedical application of cardiovascular and Glaucoma intraocular pressure monitor have been presented. The designed harvesting circuit of Native NMOS rectifier is able to drive a 1-k $\Omega$  load with 1-V and 1-mA by utilizing RF energy within a short distance, which makes the battery-less function possible.

Second, A new idea for the 5.8-GHz on-chip antenna solution to fit in a miniature environment such as human eye and vessel with 10% efficiency and -10 dBi gain has been proposed and co-designed with TSMC 0.18 $\mu$ m CMOS ICs.

Finally, based on the built-up environment model for imitating human heart and eye, the system simulation results shows at least -40-dBm receiving power can be utilized within 5-cm distance at external device, which demonstrates the feasibility of future on-demand easy-to-design implantable SoC.

### **7.2 Future Work**

With all those contributions mentioned above, this work is not fully completed yet, more effort should be made by the following researchers. There are three topics should be focused on: RF energy harvesting ability of the rectifier, fabrication possibility of the on-chip antenna and the overall system optimization

First of all, the power inputs to the rectifier dramatically affects its efficiency and output voltage, which determined by the antennas and external power generator. According to the FCC rule 36-dBm RF power fed into antenna at ISM 5.8 GHz band, this constraint is based on the

average power which is greater than the 10% duty cycle. Therefore, one way to increase the generated power from external source is to transmit RF pulse in a pretty short duty cycle. However, the challenge is how the rectifier storage the energy between the time of two pulses. Large value and high Q capacitors may need to solve this issue. Also the switching speed of the diode-connected Native NMOS has to be taken into account.

Second, the fabrication of the 3D on-chip antenna is a critical issue and needed to be studied. Taller dielectric substrate upon Silicon dioxide consumes more time to be deposited on silicon wafer process. The dielectric to support antenna must have high dielectric constant and low loss tangent which depends on the materials. Polymer ceramic is the good candidate to have such a property. Seeking other high permittivity, for example Titanium dioxide, will be another research area.

Based on the link budget analysis, the specification should be optimized depends on the loaded circuits after rectifier, application environment and signal processing technology. For example, the state-of- art low power MEMS sensing circuits for pressure detecting can consume as low as 0.5 V. That means the rectifier 1-V output voltage can be relaxed. Moreover, the sensitivity of the external receiver can also go lower than -60 dBm or even -90 dBm nowadays, and thus the output power of VCO/PA can be reduced, and the size of antenna as well. Searching for the high sensitivity technology for the entire system optimization is the third area of further study.

Beyond the topologies to improve the system performance, the simulation model also need to be improved to achieve more realistic result before turning into the fabrication level. For example, the surrounding of the human eye also includes skull, muscle and skin around. Furthermore, these materials are actually frequency dependent and vary in the entire bandwidth.

In order to have more accurate result, building more completed model is necessary but the trade-off between simulation time may occur.

Last but not least, the goal of shrinking the on-chip antenna size must be keeping in progress. For the implantable IC, the size of antenna has to be reduced below 1 mm or even smaller because the package size will enlarge the overall dimension while in the production level. The packaging needs to provide a hermetic seal to prevent leakage of body fluids into the electronics and also protect the tissue from electronic materials. The package material should also be biocompatible over its lifetime inside the body. Therefore, the package effects on on-chip antenna size and performance should be included in the design. 3D structure is the good starting solution. Beside dipole and patch, different type of antenna such as PIFA, IFA or slot applied in this idea can be in the future research.

## **APPENDIX: DERIVATION OF EQUATION OF INPUT VOLTAGE TO A RF RECTIFIER**



The purpose of this appendix is to drive the equation (3) in section 2.5.2.2, which indicates the input voltage ( $V_{in}$ ) to the rectifier is square root proportion to the source resistance ( $R_s$ ). For a given simplified circuit shown in Fig. 106, the input terminal has a source resistance of  $R_s$  and source voltage of  $V_s$ . The source power,  $P_s$ , is given by (A.1).

$$P_s = \frac{1}{2} |V_s| |I_s| = \frac{|V_s|^2}{2R_s} \quad (\text{A.1})$$

At the node A,  $R_{rec}$  is the input resistance of the rectifier with input voltage  $V_{in}$ , which is given by (A.2)

$$V_{in} = V_s (I + \Gamma) \quad (\text{A.2})$$

Where  $\Gamma$  is the reflection coefficient which is given by (A.3)

$$\Gamma = \frac{R_{rec} - R_s}{R_{rec} + R_s} \quad (\text{A.3})$$

After substituting  $V_s$  in (A.1) by (A.2) we can get  $V_{in}$  given by (A.4)

$$|V_{in}| = (I + \Gamma) \sqrt{2P_s R_s} \quad (\text{A.4})$$

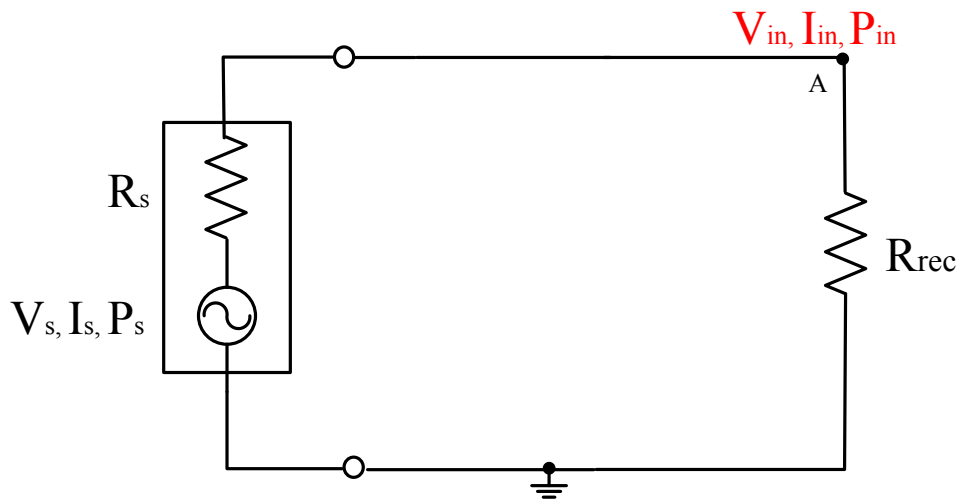


Fig. 106 Simplified circuit with a source terminal and a load of rectifier

It can be noticed by (A.4), the amplitude of the input voltage to the rectifier is determined by the source resistance and the reflection coefficient with a known source power. In order to better understand (A.4), we assume  $P_S$  is 1 W and then to see the results of different cases.

*Case 1:  $R_S = R_{rec} = 50 \Omega$ ,  $\Gamma = 0$*

$$|V_{in}| = \sqrt{2 * I * 50} = 10 \text{ V}$$

*Case 2:  $R_S = R_{rec} = 5 \Omega$ ,  $\Gamma = 0$*

$$|V_{in}| = \sqrt{2 * I * 5} = 3.62 \text{ V}$$

*Case 3:  $R_S = 50 \Omega$ ,  $R_{rec} = 25 \Omega$ ,  $\Gamma = -0.33$*

$$|V_{in}| = (1 - 0.33) \sqrt{2 * I * 50} = 6.67 \text{ V}$$

Case 1 and case 2 are based on the matching condition and in case 3, 30% mismatching occurred. As can be noticed in case 1 and case 2, the input voltage decreases while the matching resistance gets lower. From case 3, we can know the mismatching causes the input voltage degrades as well. Therefore, in summary, higher input voltage for the rectifier requires two conditions, first is the matching between the rectifier and the input terminal, and second, the matching resistance has to be as higher as possible.

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